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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SaTCR LNBs and Switchers
Core Processor	STM8
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	DiSEqC, I²C
Number of I/O	-
Voltage - Supply	2.95V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8splnb1p6

Contents

1.1.1 Pins description

Figure 3. TSSOP20/SO20W pinout

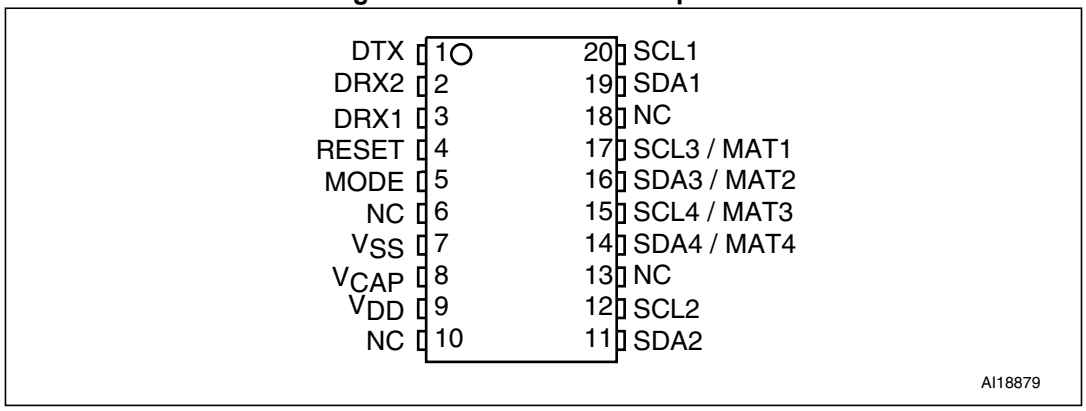


Figure 4. UFQFPN20 pinout

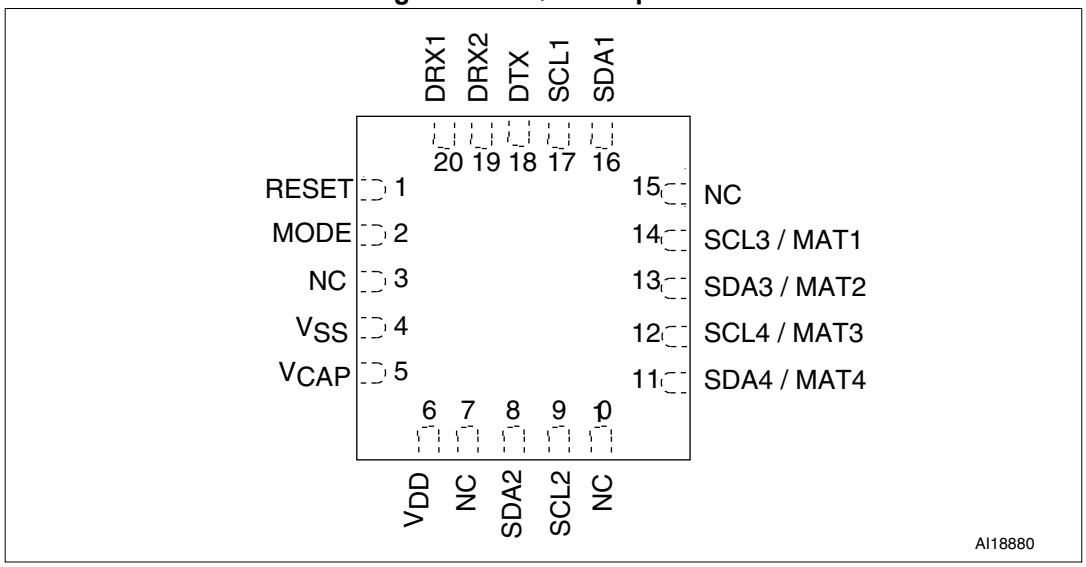


Table 1. STM8SPLNB1 pins description

pin no. TSSOP20 /SO20W	pin no. UFQFPN20	pin name	description	note
9	6	V_{DD}	+5 V power supply	+/- 10 % tolerance
7	4	V_{SS}	ground	_
4	1	RESET	device reset	0.1 µF capacitor to ground (active low)
8	5	V_{CAP}	filtering capacitor	1 µF capacitor to ground
3	20	DRX1	DiSEqC receive data input 2	HF signal after low pass filtering
2	19	DRX2	DiSEqC receive data input 2	HF signal after low pass filtering - secondary channel (less priority - see later description)

2 STM8SPLNB1 operation

STM8SPLNB1 has 8 output pins which can work as 4 I^2C master channels. Each I^2C channel can address 2 LNB devices (2 different I^2C addresses: 0xC8 and 0xCA) - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode* and *Table 3: SaTCRs implementation - incremental order mode* for assignment of given SaTCR to given I^2C bus and address.

Assignment depends from *I^2C addressing mode* EEPROM parameter - see *Table 14: STM8SPLNB1 EEPROM parameters*. As a convention, SaTCR1 must be associated to the BPF having the lowest center frequency of the application, SaTCR2 to the BPF having the next higher center frequency and so on.

Table 2. SaTCRs implementation - ST7LNB1 compatible mode

SatCR number	SaTCR(1)	SaTCR address	I^2C number
0	SaTCR1	0xC8	I^2C1
1	SaTCR2	0xCA	
2	SaTCR3	0xC8	I^2C2
3	SaTCR4	0xCA	
4	SaTCR5	0xC8	I^2C3
5	SaTCR6	0xCA	
6	SaTCR7	0xC8	I^2C4
7	SaTCR8/ legacy SaTCR (for wide RF band applications)	0xCA	

1. Selection of ST7LNB1 compatible mode: *pin MODE* (see *Table 1: STM8SPLNB1 pins description*) must be grounded and I2C addressing mode EEPROM parameter (see *Table 14: STM8SPLNB1 EEPROM parameters*) must be set to 0. Otherwise (e.g. pin MODE is left open or I2C addressing mode EEPROM parameter is set to 1) is used incremental order mode.

Table 3. SaTCRs implementation - incremental order mode

SatCR number	SaTCR(1)	SaTCR address	I^2C number
0	SaTCR1	0xC8	I^2C1
1	SaTCR2	0xCA	I^2C2
2	SaTCR3	0xC8	I^2C3
3	SaTCR4	0xCA	I^2C4
4	SaTCR5	0xCA	I^2C1
5	SaTCR6	0xC8	I^2C2
6	SaTCR7	0xCA	I^2C3
7	SaTCR8/ legacy SaTCR (for wide RF band applications)	0xC8	I^2C4

1. Selection of incremental order mode: *pin MODE* (see *Table 1: STM8SPLNB1 pins description*) is left open or I2C addressing mode EEPROM parameter (see *Table 14: STM8SPLNB1 EEPROM parameters*) is set to 1.

Another option is to decrease number of I^2C channels and use the remaining pins for legacy matrix LNB control - e.g. to have 2 I^2C channels (4 pins) and 4 legacy matrix output pins - see *Table 16: Application types*.

Operation mode and device behavior depends from final hardware configuration. This behavior is selected through configuration parameters - see *Table 14: STM8SPLNB1 EEPROM parameters*.

Note: Advantage of using incremental order mode is in applications with up to 4 SaTCRs - which is common in practice. Then each SaTCR owns one I^2C bus. I2C communication with another SaTCRs is running on different I^2C bus - so it does not disturb HF signal on given SaTCR (SaTCR is sensitive to I^2C bus signal transients).
Advantage of using ST7LNB1 compatible mode is in applications where is used SaTCRs control together with legacy matrix outputs (MAT1-MAT4) - see Section 1.1.1: Pins description. In this case there remains free only 2 I^2C buses for SaTCRs control (MAT1-MAT4 pins occupy I^2C3 and I^2C4 bus). In ST7LNB1 compatible mode 2 I^2C buses can address up to 4 SaTCRs - 2 SaTCRs per I^2C bus. Disadvantage is the I^2C bus disturbance to SaTCR which is not addressed - shared I^2C bus (HF filters on I^2C buses is recommended).

2.1 Supported DiSEqC commands

In the following *Table 4: STM8SPLNB1 DiSEqC™ supported commands* are listed DiSEqC commands supported by STM8SPLNB1. For more details about commands, refer to the *DiSEqC™ slave microcontroller specifications* at www.eutelsat.com.

Table 4. STM8SPLNB1 DiSEqC™ supported commands

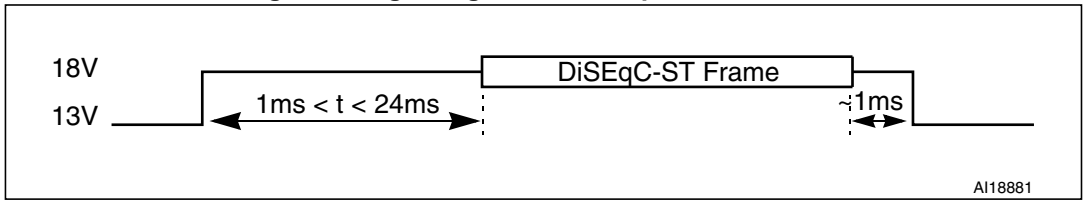
command number	command name	function
0x00	RESET	Reset DiSEqC™ microcontroller
0x0D	config read	Read configuration parameters from EEPROM
0x0F	config write	Write configuration parameters to EEPROM
0x38	write to port	DiSEqC 1.0: Write to port group command - Legacy commands
0x5A	operation command	DiSEqC-ST normal operation commands: ODU_Changechannel or ODU_SatCROFF
0x5B	installation command	DiSEqC-ST installation commands: ODU_Config, ODU_EEPvar.LOFREQ or ODU_SatCRxON

2.2 DiSEqC commands details

2.2.1 Command signaling

To be detected, the DiSEqC-ST commands must be sent after a voltage change from 13 to 18 V. A delay time between 4 ms and 24 ms must be respected before sending the DiSEqC-ST commands (see *Figure 5: Signaling of the DiSEqC-ST command*).

Figure 5. Signaling of the DiSEqC-ST command



2.2.2 Command 0x0F

STM8SPLNB1 devices are shipped to customers with a default parameter values. These parameters can be updated using a dedicated 0x0F DiSEqC command. This command has the following format where “[data]” is the parameter value to be programmed at the “[index]” location as described in *Table 14: STM8SPLNB1 EEPROM parameters*.

Table 5. Command 0x0F format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x0F	[index]	[data]

Note: The special command E0 xx 0F FF FF protects the EEPROM data from any subsequent write access (where xx is the corresponding DiSEqC slave address).

2.2.3 Command 0x0D

This command is dedicated for reading configuration parameters. This command has the following format where the “[index]” is location to be read as shown in *Table 14: STM8SPLNB1 EEPROM parameters*.

Table 6. Command 0x0D format

frame	DiSEqC™ address	command	data1
0xE2	[device address]	0x0D	[index]

The format of the reply frame from slave has format according *Table 7: Reply to command 0x0D format* where “[data]” is the byte read from EEPROM.

Table 7. Reply to command 0x0D format

frame	data1
0xE4	[data]

Table 11. Feeds(1)

Feed	RF input		
	Band	Polarization	Satellite
0	Low	Vertical	A
1	High	Vertical	A
2	Low	Horizontal	A
3	High	Horizontal	A
4	Low	Vertical	B
5	High	Vertical	B
6	Low	Horizontal	B
7	High	Horizontal	B

1. Applications supporting legacy are limited to one satellite only (satellite A - see *Table 8: Command 0x38 format*).

2.2.6 Command 0x5B

This command is used only during LNB (or switched) installation/configuration. Command 0x5B is DiSEqC command (see *Table 12: Command 0x5B format*) with two data bytes. In dependence from those data bytes are performed three subcommands which descriptions are in *Table 13: Subcommands 0x5B format - ODU_SaTCR_Inst*.

Table 12. Command 0x5B format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x5B	[data1](1)	[data2](1)

1. See *Table 13.: Subcommands 0x5B format - ODU_SaTCR_Inst* for details.

Table 13. Subcommands 0x5B format - ODU_SaTCR_Inst

Subcommand	data1			data2	description
	[7:5]	[4:2]	[1:0]	[7:0]	
ODU_Config	SaTCR(1)	0	1	AppliNum(2)	This command is sent by the STB in order to set the STM8SPLNB1 application number. If the data2 value corresponds to the STM8SPLNB1 AppliNum, then the STM8SPLNB1 commands SaTCR indicated in data1 to send a tone having frequency: F = BPF(4), else: F = (BPF + 20 MHz).
ODU_Lofreq	SaTCR(1)	0	2	LOfreqNum(3)	This command is sent by the STB in order to set the L.O. frequencies present in the LNB. If the data2 value corresponds to the STM8SPLNB1 LOfreqNum, then the STM8SPLNB1 commands SaTCR indicated in data1 to send a tone having frequency: F = BPF(4), else: F = (BPF + 20 MHz).
ODU_SaTCRxSignalOn	xxh	0		xxh	When receiving this command the STM8SPLNB1 commands all connected SaTCRs to send a tone in order to indicate their respective BPF(4) center frequencies.

1. SaTCR number - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode*
2. See *Table 17: DiSEqC Applications* for details.
3. See *Table 18: Local oscillator frequencies* for details.
4. BPF is bandpass center frequency for a given SaTCR - see *Table 14: STM8SPLNB1 EEPROM parameters* for details.

3 Configuration parameters

STM8SPLNB1 devices are compliant with the Eutelsat DiSEqC slave microcontroller specifications version 1.0, but they are not scanning the control pins to determine the slave configuration. Instead this are the slave configuration parameters stored in EEPROM memory and must be programmed for each specific application through programming parameters in STM8SPLNB1 data EEPROM memory.

The EEPROM parameters described are the default configurations in our firmware. Custom configurations can be programmed at factory on request according customer requirements (FastROM process available). Customer can reprogram all EEPROM parameters through DiSEqC command - see *Section 2.2.2: Command 0x0F*.

3.1 Configuration parameters

The slave configuration parameters for STM8SPLNB1 are listed in *Table 14: STM8SPLNB1 EEPROM parameters*:

Table 14. STM8SPLNB1 EEPROM parameters

index	parameter	description	default value
00	Slave Address	DiSEqC slave address(1)	0x11
01	SaTCR1 BPF (lsb)	(2)	0x5D
02	SaTCR1 BPF (msb)		0x02
03	SaTCR2 BPF (lsb)		0xC6
04	SaTCR2BPF (msb)		0x02
05	SaTCR3 BPF (lsb)		0x48
06	SaTCR3 BPF (msb)		0x03
07	SaTCR4 BPF (lsb)		0xFC
08	SaTCR4 BPF (msb)		0x03
09	SaTCR5 BPF (lsb)		0xFF
0A	SaTCR5BPF (msb)		0xFF
0B	SaTCR6 BPF (lsb)		0xFF
0C	SaTCR6 BPF (msb)		0xFF
0D	SaTCR7 BPF(lsb) / legacy SaTCR Low band (msb)	(3)	0xFF
0E	SaTCR7 BPF(msb) / legacy SaTCR Low band (lsb)		0xFF
0F	SaTCR8 BPF(lsb) / legacy SaTCR High band (msb)		0xFF
10	SaTCR8 BPF(msb) / legacy SaTCR High band (lsb)		0xFF
11	Applitype	Application type number (refer to *Table 16.*)	0x00

Table 16. Application types (continued)

number	application type	description
1	SaTCR and legacy (standard RF band) (see *Figure 7: SaTCR control and legacy configuration (standard RF band)*)	– Control through I^2C up to 4 SaTCRs – Control of a legacy matrix using up to 4 pins
2	SaTCR and legacy (wide RF band) (see *Figure 8: SaTCR control and legacy configuration (wide RF band)*)	– Control though I^2C of up to 6 SaTCRs + legacy – Control of a dedicated SaTCR for the legacy support

1. This application could support up to 8 RF feeds. (applications 1 and 2 are limited to 4 RF feeds).

Figure 6. SaTCR control configuration

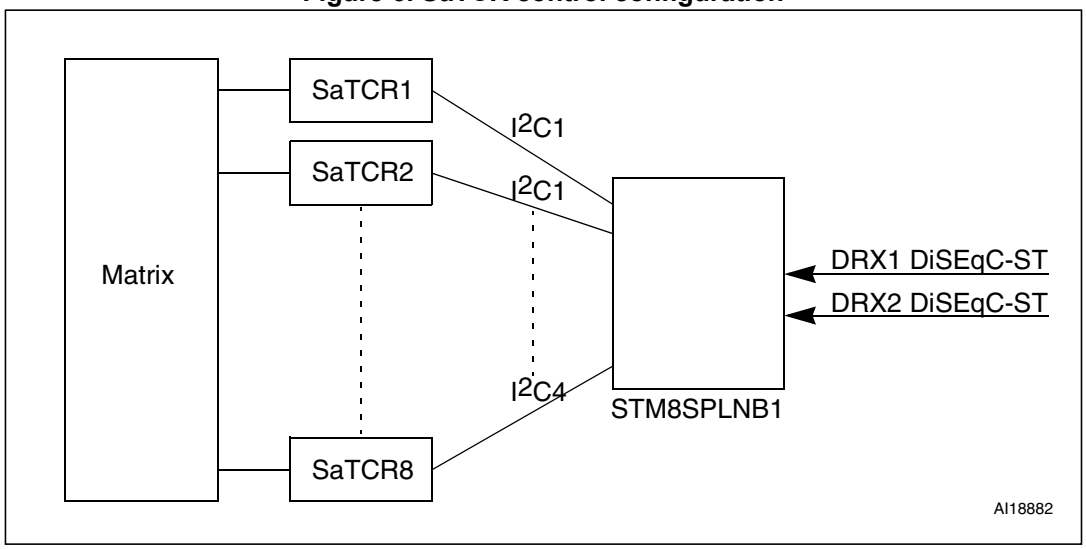


Figure 7. SaTCR control and legacy configuration (standard RF band)

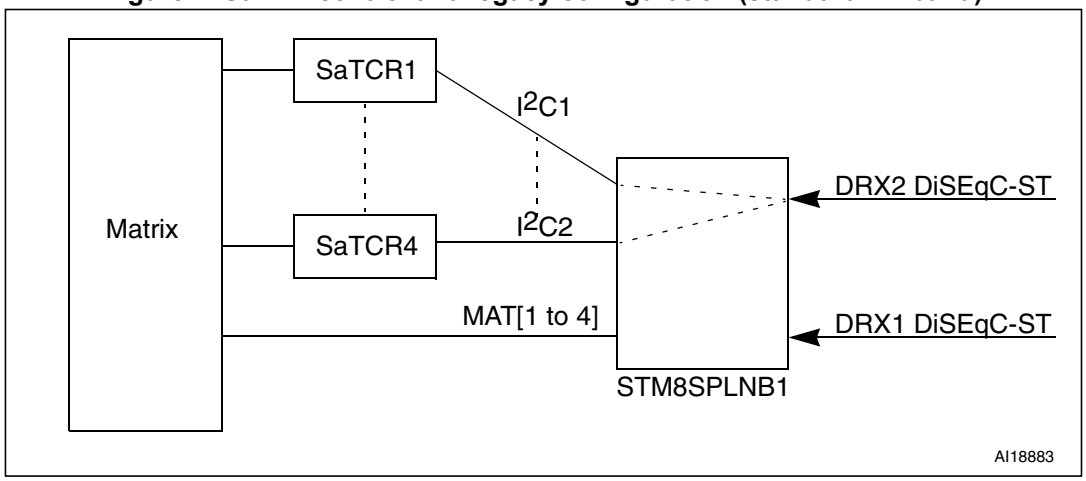


Table 18. Local oscillator frequencies

LofreqNum (hex)		Local oscillator frequency
Standard RF band	0x00	none
	0x01	not known
	0x02	9.750 GHz
	0x03	10.000 GHz
	0x04	10.600 GHz
	0x05	10.750 GHz
	0x06	11.000 GHz
	0x07	11.250 GHz
	0x08	11.475 GHz
	0x09	20.250 GHz
	0x0A	5.150 GHz
	0x0B	1.585 GHz
	0x0C	13.850 GHz
	0x0D	not allocated
	0x0E	not allocated
	0x0F	not allocated
Wide RF band	0x10	not allocated
	0x11	10.000 GHz
	0x12	10.200 GHz
	0x13	13.250 GHz
	0x14	13.450 GHz
	0x15 - 0x1F	not allocated

4.3 Operating conditions

4.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85 °C	TSSOP20	-	238	mW
		SO20W	-	220	
		UFQFPN20	-	220	
T_A	Ambient temperature	Maximum power dissipation	-40	85	°C
T_J	Junction temperature range	-	-40	105	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *5.3: Thermal characteristics*)

Table 23. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	-	µs/V
	V_{DD} fall time rate(1)	-	2	-	-	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min.) when the t_{TEMP} delay has elapsed.

4.3.4 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

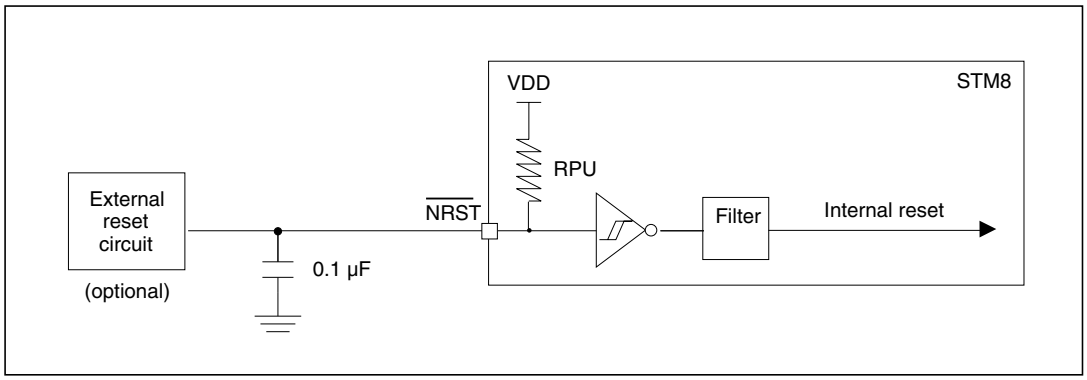
Table 26. RESET pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(RST)}$	RESET Input low level voltage (1)	-	-0.3 V		0.3 x V_{DD}	V
$V_{IH(RST)}$	RESET Input high level voltage (1)	-	0.7 x V_{DD}		V_{DD} + 0.3	
$R_{PU(RST)}$	RESET Pull-up resistor (2)	-	30	55	80	kΩ

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.

The reset network shown in the following *Figure 12.* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in the *Table 26.: RESET pin characteristics*. Otherwise the reset is not taken into account internally.

Figure 12. Recommended reset pin protection



Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 28. EMI data

Symbol	Parameter	Conditions			Unit
		General conditions	Monitored frequency band	f_{CPU}(1)	
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP32 package Conforming to SAE J 1752/3	0.1 MHz to 30 MHz	3	dBµV
			30 MHz to 130 MHz	10	
			130 MHz to 1 GHz	7	
	SAE EMI level		SAE EMI level	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU, and DLU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 29. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25 °C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A LQFP32 package = 25 °C, conforming to SD22-C101	IV	1000	

1. Data based on characterization results, not tested in production

5.2 Package mechanical data

5.2.1 TSSOP package mechanical data

Figure 13. 20-pin, 4.40 mm body, 0.65 mm pitch

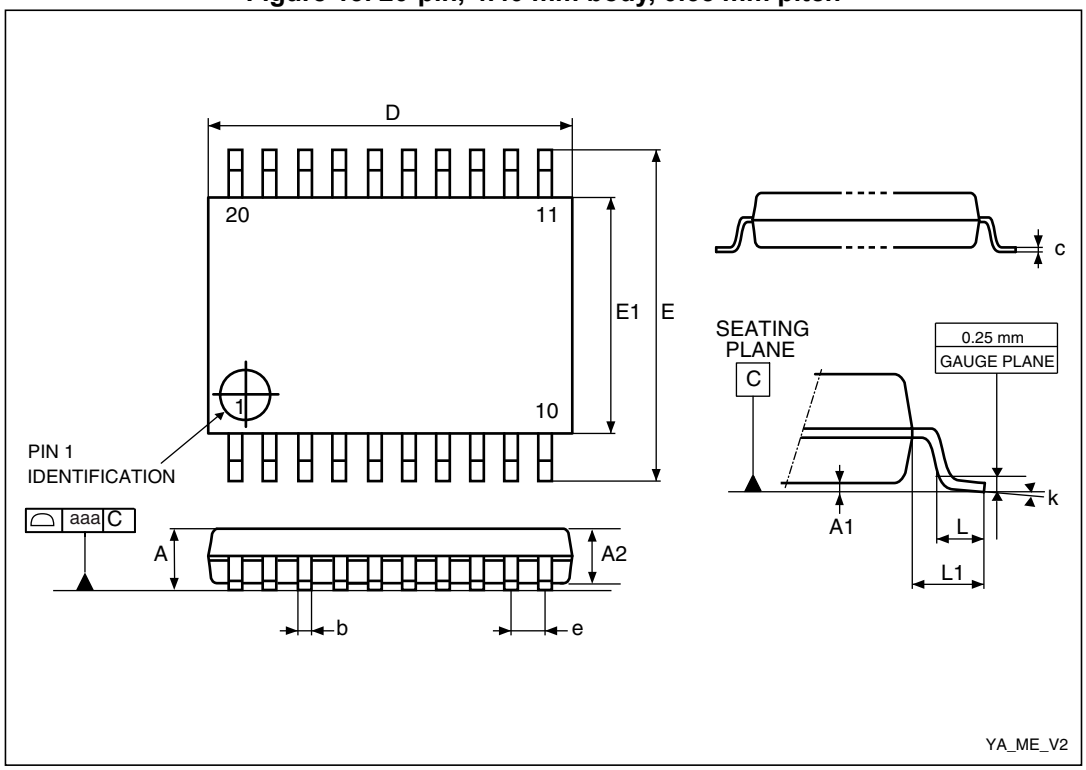


Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data

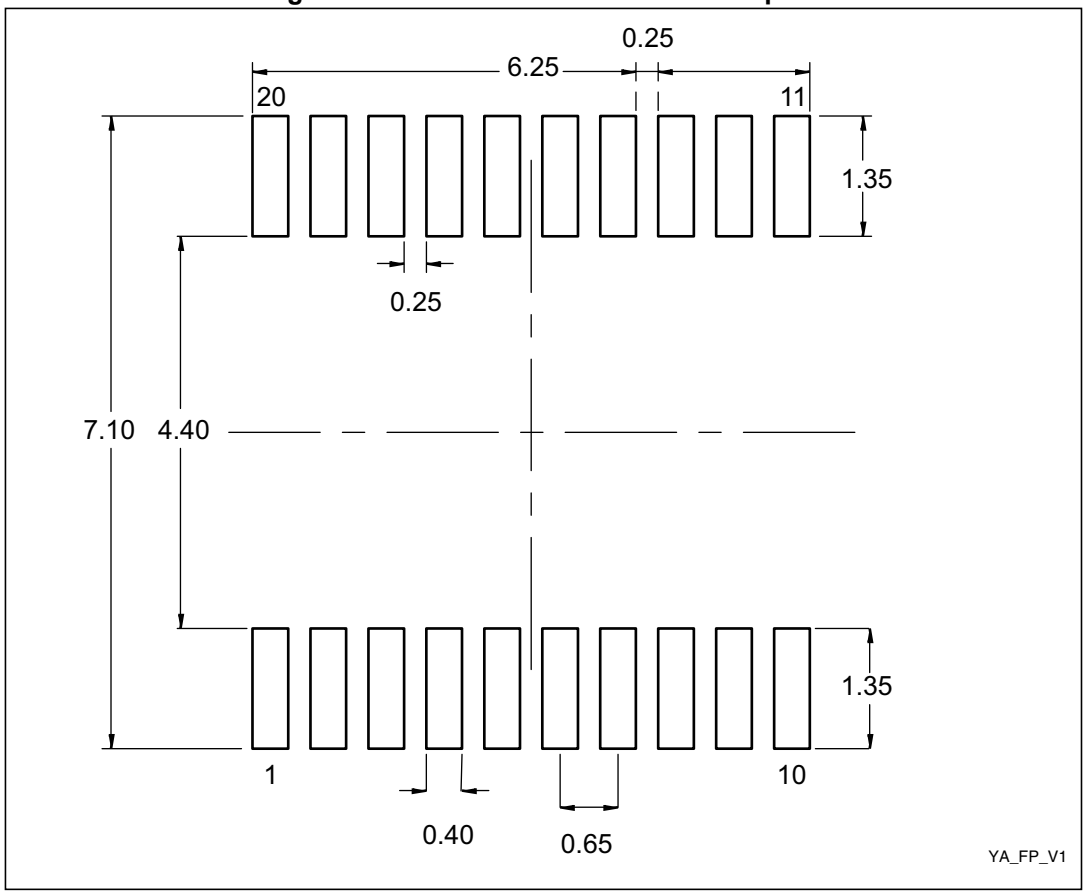
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	0.100			0.0039		

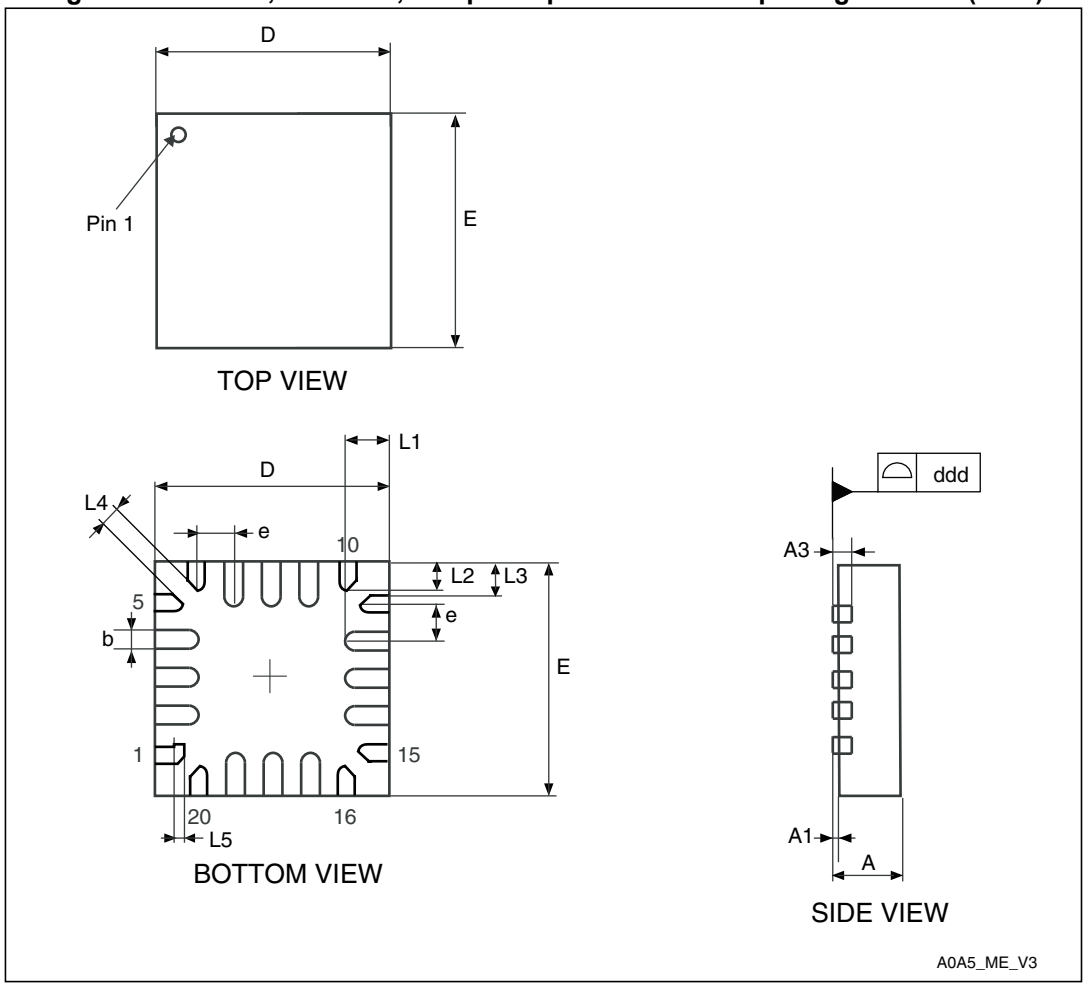
1. Values in inches are converted from mm and rounded to 4 decimal digits
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 14. TSSOP20 recommended footprint



5.2.3 UFQFPN package mechanical data

Figure 16. 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)



1. Drawing is not to scale

Table 33. 20-lead, ultra thin, fine pitch quad flat no-lead package (3 x 3) package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

10	SaTCR8 BPF(msb)/Legacy, SaTCR High band (lsb)	FFh	[h]
11	Applitype	00h	[h]
12	AppliNum	04h	[h]
13	High L.O freq Number	04h	[h]
14	Low L.O freq Number	02h	[h]
15	SaTCR1 matrix truth table	ACh	[h]
16		35h	[h]
17	SaTCR2 matrix truth table	59h	[h]
18		6Ah	[h]
19	SaTCR3 matrix truth table	56h	[h]
1A		9Ah	[h]
1B	SaTCR4 matrix truth table	95h	[h]
1C		A6h	[h]
1D	SaTCR5 matrix truth table	FFh	[h]
1E		FFh	[h]
1F	SaTCR6 matrix truth table	FFh	[h]
20		FFh	[h]
21	SaTCR7 matrix truth table	FFh	[h]
22		FFh	[h]
23	SaTCR8 matrix truth table	FFh	[h]
24	Legacy matrix	FFh	[h]
25	SaTCRs GAIN	FFh	[h]
26		FFh	[h]
27	SaTCRs number	04h	[h]
28	I2C addressing mode	00h	[h]
29	Software version	15h	[h]

(Please refer to *Table 14: STM8SPLNB1 EEPROM parameters* in the datasheet for full descriptions and notes of EEPROM Parameters)

Comments	.....
Notes	.....
Date	.....
Signature	.....

Optional data bytes are data for given command. Data in answer (from slave) specify required information. There is specified data byte format only for 3 required bytes from slave:

- Status byte (bus collision, reset status, standby status, supply voltage)
- Configuration byte (more detailed information about current slave configuration)
- Switches byte (describes status of the committed switches)

For more information about format of those 3 data bytes refer to *DiSEqC™ slave microcontroller specifications* available at www.eutelsat.com (and *Table 4: STM8SPLNB1 DiSEqC™ supported commands*).

7 Revision history

Table 36. Document revision history

Date	Revision	Changes
28-Jul-2011	1	Initial release.
08-Sep-2011	2	Updated RESET capacitor value in *Figure 2: STM8SPLNB1 typical configuration*. Updated AppliNum and SaTCRs number parameters. Added note on V_{CAP} parameter in *Table 22: General operating conditions*.
03-Nov-2011	3	Updated datasheet description. Updated conditions and notes related to V_{CAP} parameter in *Table 22: General operating conditions*.
11-Jun-2012	4	Updated typical and maximum values of R_{PU} in *Table 26: RESET pin characteristics*. Modified *Figure 16: 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)* to add package top view.
18-Dec-2014	5	Updated: – *Section 5.2.1: TSSOP package mechanical data*, – *Section 5.2.2: SO20W package mechanical data*, – *Section 5.2.3: UFQFPN package mechanical data*.