Infineon Technologies - MB96F623RBPMC1-GS-UJE2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

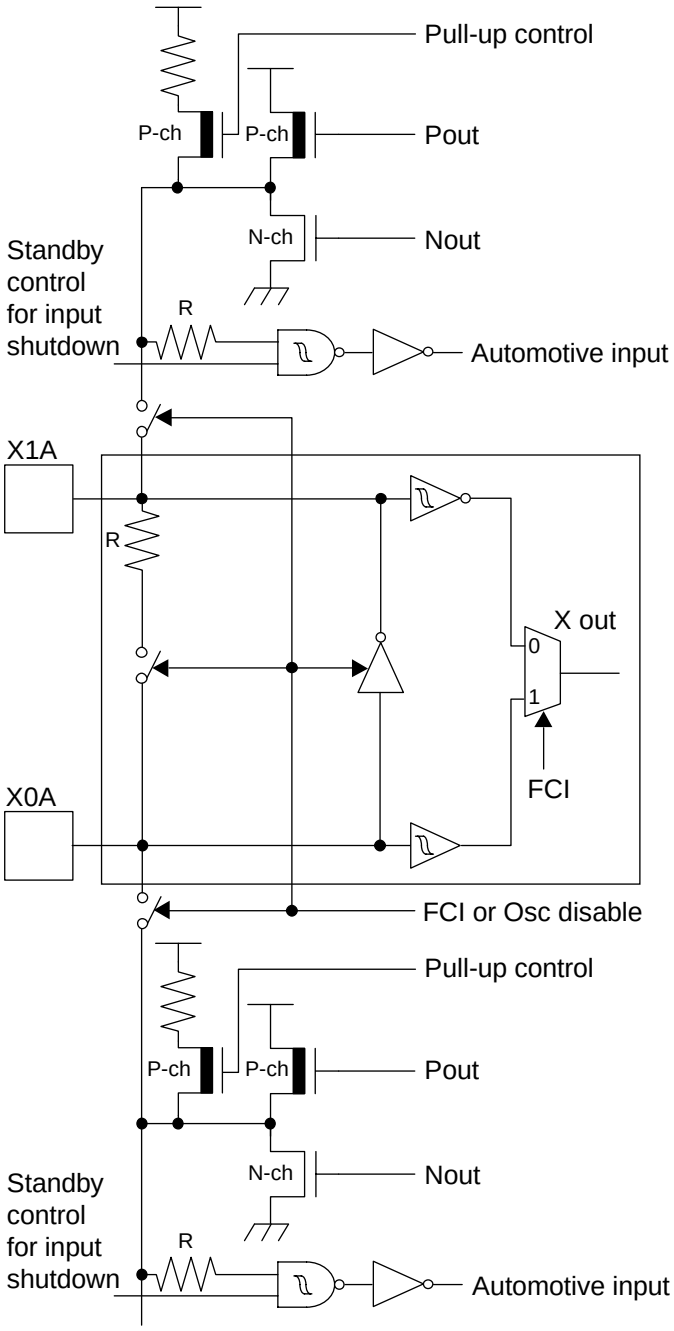
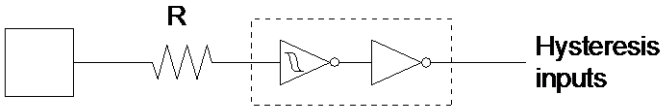
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f623rbpmc1-gs-uje2

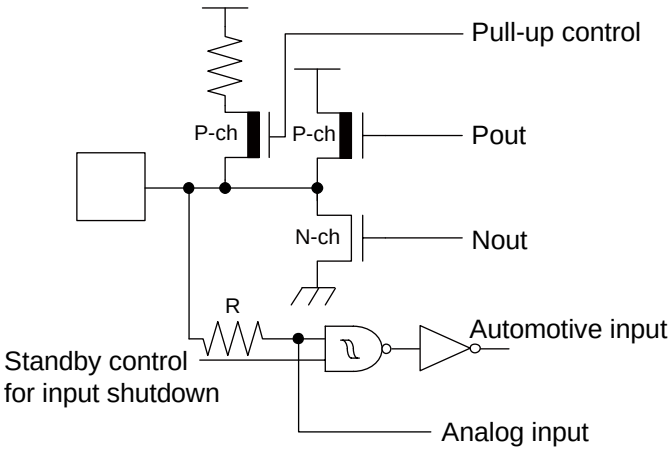
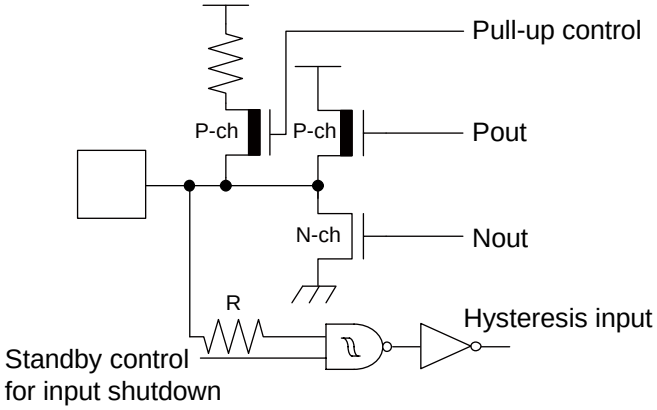
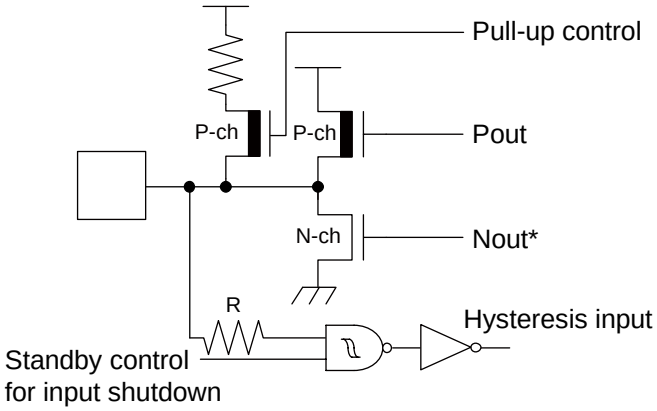
- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I^2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor
- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase or write

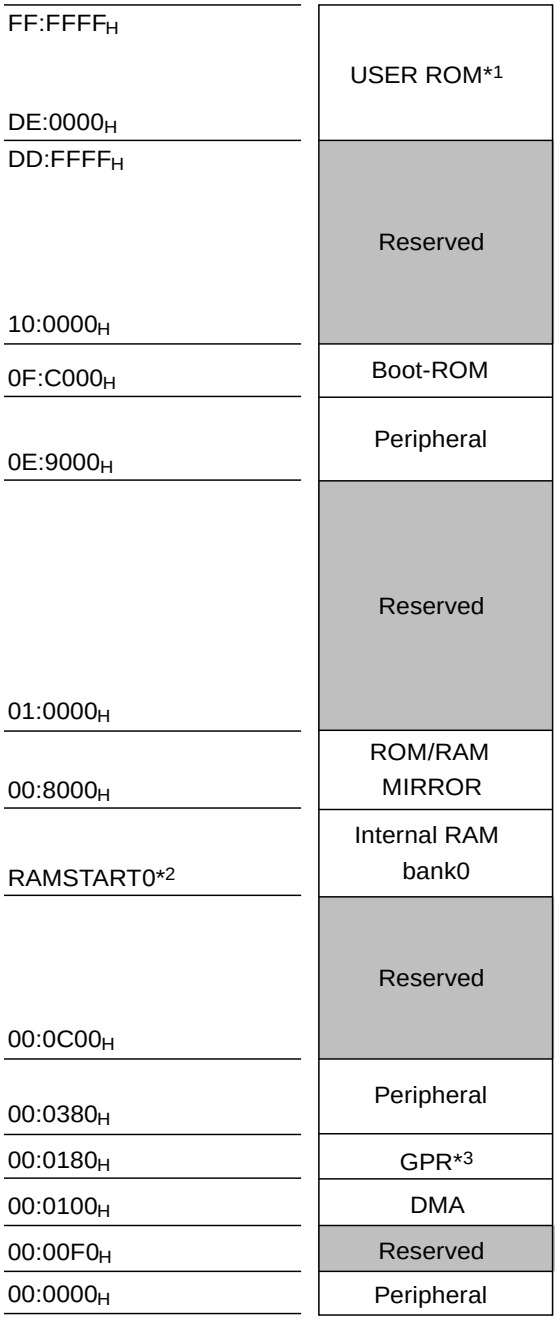
Pin No.	I/O Circuit Type*	Pin Name
33	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
34	H	P01_2 / INT11_R
35	H	P01_3
36	H	P01_4 / PPG4_B
37	M	P01_5 / SIN2_R / INT7_R
38	H	P01_6 / SOT2_R / PPG6_B
39	M	P01_7 / SCK2_R / PPG7_B
40	H	P02_0 / PPG12 / CKOT1_R
41	H	P02_1
42	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
43	H	P02_3
44	H	P02_4 / AIN0 / IN0 / TTG0
45	C	RSTX
46	A	X1
47	A	X0
48	Supply	Vss
49	Supply	Vcc
50	F	C
51	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
52	N	P04_4 / SDA0 / FRCK0
53	N	P04_5 / SCL0 / FRCK1
54	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
55	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
56	M	P03_2 / INT10_R / RX2
57	H	P03_3 / TX2
58	K	P03_4 / OUT4 / AN28
59	K	P03_5 / OUT5 / AN29
60	K	P03_6 / ZIN1 / OUT6 / AN30
61	K	P03_7 / OUT7 / AN31
62	K	P06_0 / AN0 / PPG0
63	K	P06_1 / AN1 / PPG1
64	Supply	AVcc

*: See “I/O Circuit Type” for details on the I/O circuit types.

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

7. Memory Map



*1: For details about USER ROM area, see “USER ROM MEMORY MAP FOR FLASH DEVICES” on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

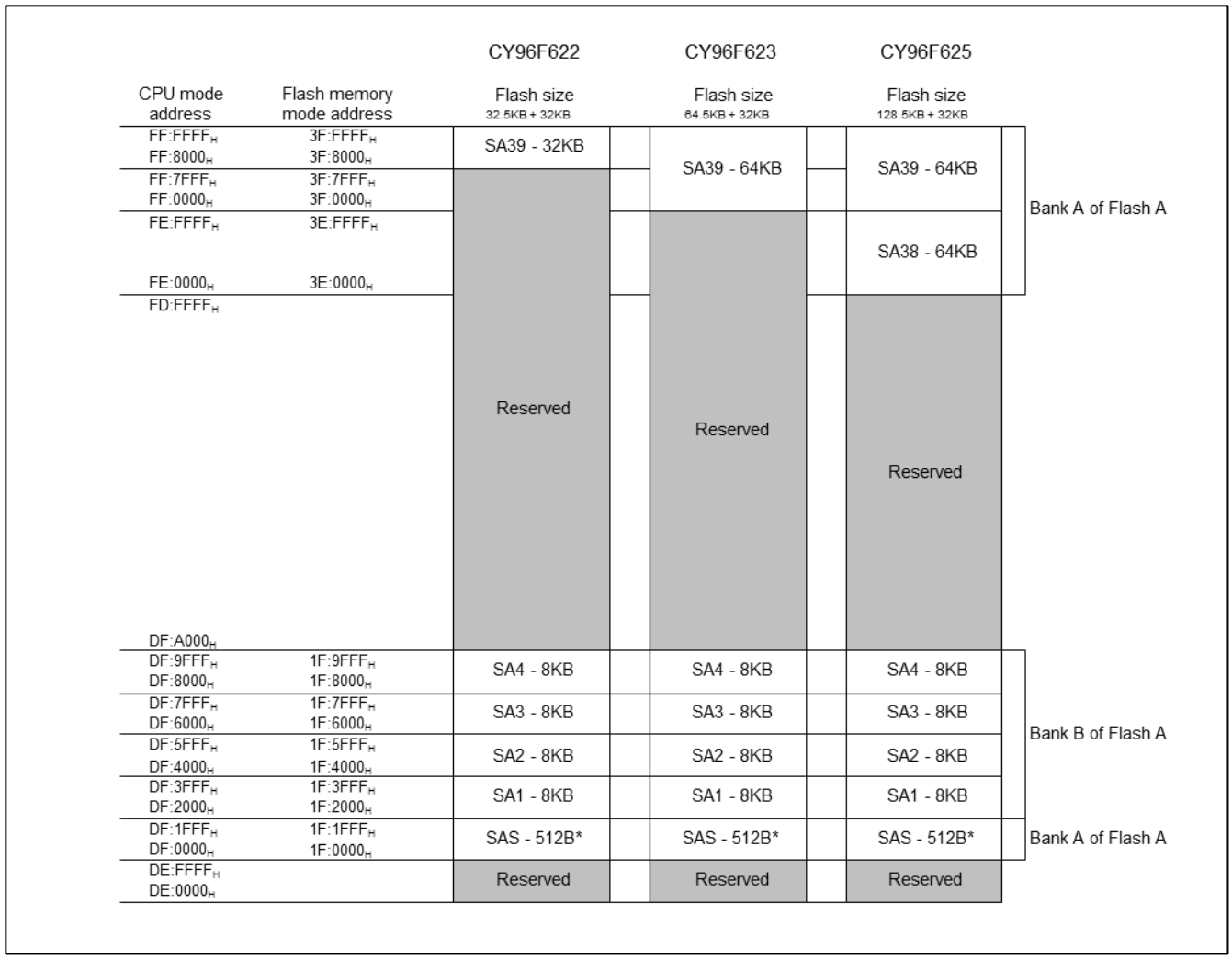
*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

9. User ROM Memory Map For Flash Devices



*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^{2}PROM emulation.

11. Interrupt Vector Table

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	-	-	18	Reserved
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	-	-	22	Reserved
23	$3A0_H$	-	-	23	Reserved
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	-	-	33	Reserved
34	374_H	-	-	34	Reserved
35	370_H	CAN2	No	35	CAN Controller 2
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
81	$2B8_H$	OCU4	Yes	81	Output Compare Unit 4
82	$2B4_H$	OCU5	Yes	82	Output Compare Unit 5
83	$2B0_H$	OCU6	Yes	83	Output Compare Unit 6
84	$2AC_H$	OCU7	Yes	84	Output Compare Unit 7
85	$2A8_H$	-	-	85	Reserved
86	$2A4_H$	-	-	86	Reserved
87	$2A0_H$	-	-	87	Reserved
88	$29C_H$	-	-	88	Reserved
89	298_H	FRT0	Yes	89	Free-Running Timer 0
90	294_H	FRT1	Yes	90	Free-Running Timer 1
91	290_H	FRT2	Yes	91	Free-Running Timer 2
92	$28C_H$	FRT3	Yes	92	Free-Running Timer 3
93	288_H	RTC0	No	93	Real Time Clock
94	284_H	CAL0	No	94	Clock Calibration Unit
95	280_H	-	-	95	Reserved
96	$27C_H$	IIC0	Yes	96	I^2C interface 0
97	278_H	-	-	97	Reserved
98	274_H	ADC0	Yes	98	A/D Converter 0
99	270_H	-	-	99	Reserved
100	$26C_H$	-	-	100	Reserved
101	268_H	-	-	101	Reserved
102	264_H	-	-	102	Reserved
103	260_H	-	-	103	Reserved
104	$25C_H$	-	-	104	Reserved
105	258_H	LINR2	Yes	105	LIN USART 2 RX
106	254_H	LINT2	Yes	106	LIN USART 2 TX
107	250_H	-	-	107	Reserved
108	$24C_H$	-	-	108	Reserved
109	248_H	-	-	109	Reserved
110	244_H	-	-	110	Reserved
111	240_H	-	-	111	Reserved
112	$23C_H$	-	-	112	Reserved
113	238_H	-	-	113	Reserved
114	234_H	-	-	114	Reserved
115	230_H	LINR7	Yes	115	LIN USART 7 RX
116	$22C_H$	LINT7	Yes	116	LIN USART 7 TX
117	228_H	LINR8	Yes	117	LIN USART 8 RX
118	224_H	LINT8	Yes	118	LIN USART 8 TX
119	220_H	-	-	119	Reserved
120	$21C_H$	-	-	120	Reserved
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
				-	-	35	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
				-	-	8.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
				-	-	6.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
				-	-	4.2	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

14.3.2 Pin Characteristics

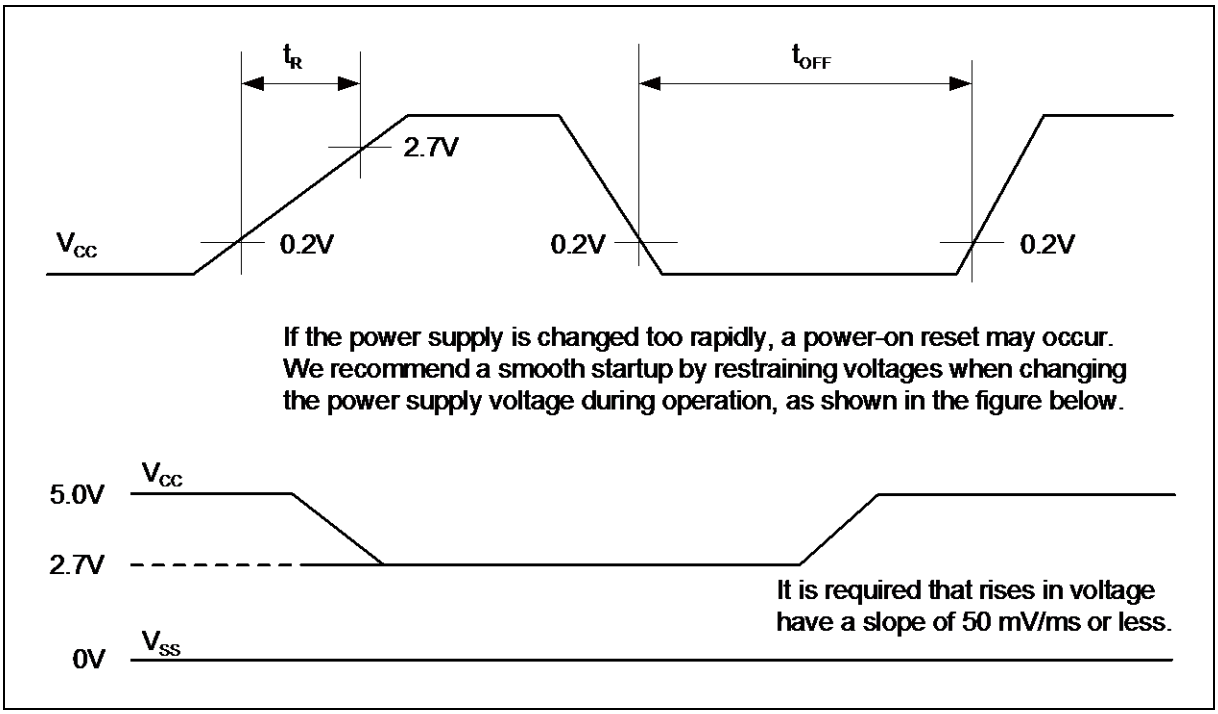
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC} + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS} - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	V_{SS} - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS} - 0.3	-	0.8	V	TTL Input

14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



14.4.8 USART Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C, C_L=50pF)

Parameter	Symbol	Pin Name	Conditions	4.5V ≤ Vcc < 5.5V		2.7V ≤ Vcc < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1}$ – 20*	-	$N \times t_{CLKP1}$ – 30*	-	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1}$ + 45	-	$2t_{CLKP1}$ + 55	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2$ + 10	-	$t_{CLKP1}/2$ + 10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

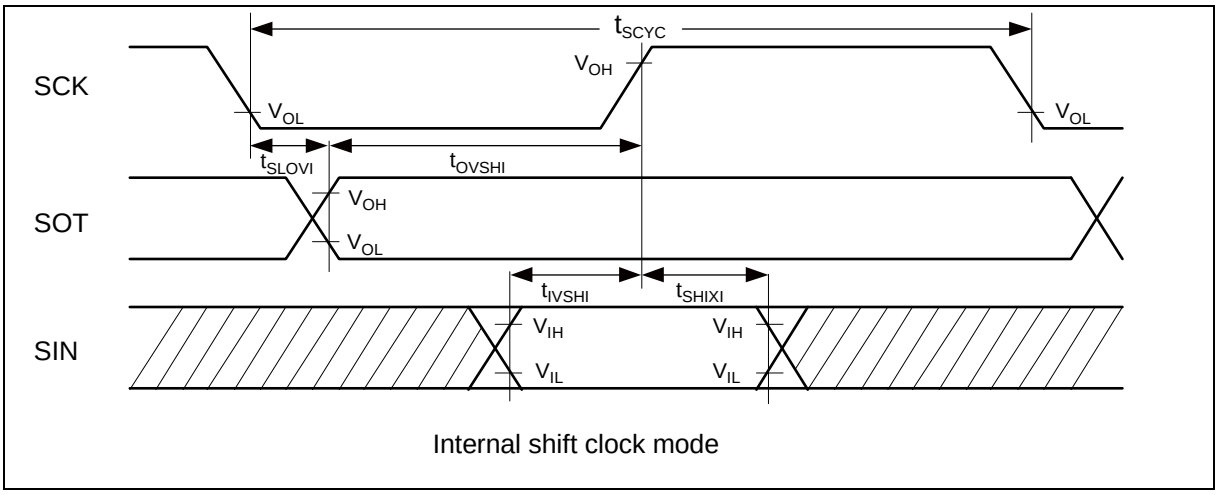
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “CY96600 series HARDWARE MANUAL”.
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number. For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

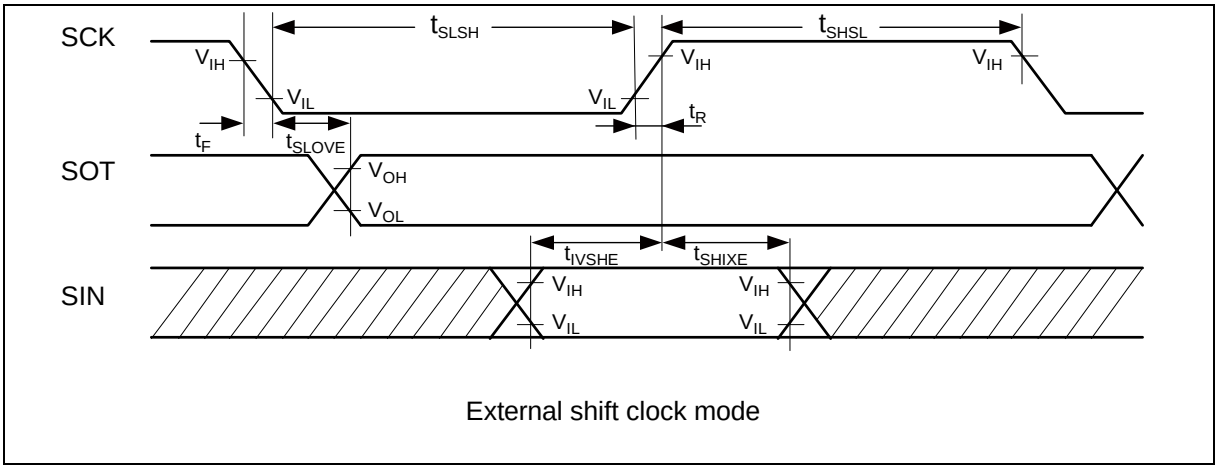
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
…	…



Internal shift clock mode



External shift clock mode

14.5 A/D Converter

14.5.1 Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS} + 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN8, 9, 12, 13	-	-	15.5	pF	Normal outputs
		AN16 to 23	-	-	17.4	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	1450	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	2700	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	AN8, 9, 12, 13	- 1.0	-	+ 1.0	µA	AV_{SS} < V_{AIN} < AV_{CC}, AVRH
		AN16 to 23	- 3.0	-	+ 3.0	µA	
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq$ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq$ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		$T_A \leq$ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [*2]
10,000	10 [*2]
100,000	5 [*2]

[*1]: See "Low Voltage Detection Function Characteristics".

[*2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

16. Ordering Information

MCU with CAN Controller

Part Number	Flash Memory	Package*
CY96F622RBPMC-GS-UJE1	Flash A (64.5KB)	64-pin plastic LQFP (LQG064)
CY96F622RBPMC-GS-UJE2		
CY96F622RBPMC1-GS-UJE1		64-pin plastic LQFP (LQD064)
CY96F622RBPMC1-GS-UJE2		
CY96F623RBPMC-GS-UJE1	Flash A (96.5KB)	64-pin plastic LQFP (LQG064)
CY96F623RBPMC-GS-UJE2		
CY96F623RBPMC1-GS-UJE2		64-pin plastic LQFP (LQD064)
CY96F625RBPMC-GS-UJE1	Flash A (160.5KB)	64-pin plastic LQFP (LQG064)
CY96F625RBPMC-GS-UJE2		
CY96F625RBPMC1-GS-UJE1		64-pin plastic LQFP (LQD064)
CY96F625RBPMC1-GS-UJE2		

*: For details about package, see "PACKAGE DIMENSION".

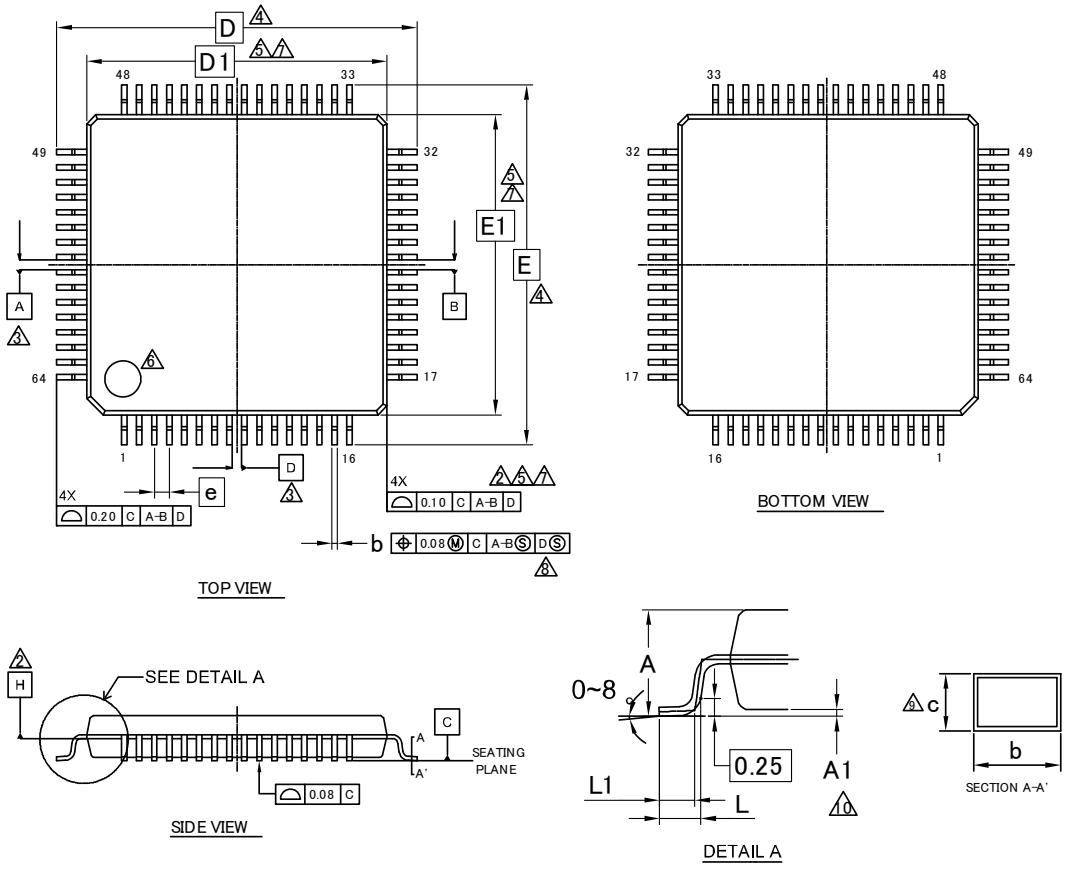
MCU without CAN Controller

Part Number	Flash Memory	Package*
CY96F622ABPMC-GS-UJE1	Flash A (64.5KB)	64-pin plastic LQFP (LQG064)
CY96F622ABPMC-GS-UJE2		
CY96F622ABPMC1-GS-UJE1		64-pin plastic LQFP (LQD064)
CY96F622ABPMC1-GS-UJE2		
CY96F622ABPMC1-GS-UJERE2		
CY96F623ABPMC-GS-UJE1	Flash A (96.5KB)	64-pin plastic LQFP (LQG064)
CY96F623ABPMC-GS-UJE2		
CY96F623ABPMC1-GS-UJE1		64-pin plastic LQFP (LQD064)
CY96F623ABPMC1-GS-UJE2		
CY96F625ABPMC-GS-UJE2	Flash A (160.5KB)	64-pin plastic LQFP (LQG064)
CY96F625ABPMC1-GS-UJE1		64-pin plastic LQFP (LQD064)
CY96F625ABPMC1-GS-UJE2		

*: For details about package, see "PACKAGE DIMENSION".

LQD064, 64 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 64pin	LQD064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Page	Section	Change Results
56	Electrical Characteristics 7. Flash Memory Write/Erase Characteristics	Changed the Note While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing, be sure to turn the power off by using an external voltage detector. → While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
60	Ordering Information	Deleted the Part number MCU with CAN controller MB96F622RBPMC-GTE2 MB96F622RBPMC1-GTE2 MB96F623RBPMC-GTE2 MB96F623RBPMC1-GTE2 MB96F625RBPMC-GTE2 MB96F625RBPMC1-GTE2 MCU without CAN controller MB96F622ABPMC-GTE2 MB96F622ABPMC1-GTE2 MB96F623ABPMC-GTE2 MB96F623ABPMC1-GTE2 MB96F625ABPMC-GTE2 MB96F625ABPMC1-GTE2
Revision 2.1		
-	-	Company name and layout design change
Rev.*B		
5, 7, 59, 60, 61, 62	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-64P-M23 → LQG064 FPT-64P-M24 → LQD064
59	16. Ordering Information	Added the following part number. MB96F622RBPMC-GS-UJE1 MB96F622RBPMC-GS-UJE2 MB96F622RBPMC1-GS-UJE1 MB96F622RBPMC1-GS-UJE2 MB96F623RBPMC-GS-UJE1 MB96F623RBPMC-GS-UJE2 MB96F623RBPMC1-GS-UJE1 MB96F623RBPMC1-GS-UJE2 MB96F625RBPMC-GS-UJE1 MB96F625RBPMC-GS-UJE2 MB96F625RBPMC1-GS-UJE1 MB96F625RBPMC1-GS-UJE2 MB96F622ABPMC-GS-UJE1 MB96F622ABPMC-GS-UJE2 MB96F622ABPMC1-GS-UJE1 MB96F622ABPMC1-GS-UJE2 MB96F623ABPMC-GS-UJE1 MB96F623ABPMC-GS-UJE2 MB96F623ABPMC1-GS-UJE1 MB96F623ABPMC1-GS-UJE2 MB96F625ABPMC-GS-UJE1 MB96F625ABPMC-GS-UJE2 MB96F625ABPMC1-GS-UJE1 MB96F625ABPMC1-GS-UJE2

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>Rev.*C</td><td></td><td></td></tr>
<tr><td>11</td><td>5. Pin Circuit Type</td><td>The shading parts below revised I/O circuit type and Pin name.

Error)
<table>
<tr><th>Pin No.</th><th>I/O Circuit Type*</th><th>Pin Name</th></tr>
<tr><td>33</td><td>N</td><td>P04_5 / SCL0</td></tr>
<tr><td>34</td><td>O</td><td>DEBUG I/F</td></tr>
<tr><td>35</td><td>H</td><td>P17_0</td></tr>
<tr><td>36</td><td>C</td><td>MD</td></tr>
<tr><td>37</td><td>A</td><td>X0</td></tr>
<tr><td>38</td><td>A</td><td>X1</td></tr>
<tr><td>39</td><td>Supply</td><td>Vss</td></tr>
<tr><td>40</td><td>B</td><td>P04_0 / X0A</td></tr>
<tr><td>41</td><td>B</td><td>P04_1 / X1A</td></tr>
<tr><td>42</td><td>C</td><td>RSTX</td></tr>
<tr><td>43</td><td>J</td><td>P11_7 / SEG3 / IN0_R</td></tr>
<tr><td>44</td><td>J</td><td>P11_0 / COM0</td></tr>
<tr><td>45</td><td>J</td><td>P11_1 / COM1 / PPG0_R</td></tr>
<tr><td>46</td><td>J</td><td>P11_2 / COM2 / PPG1_R</td></tr>
<tr><td>47</td><td>J</td><td>P11_3 / COM3 / PPG2_R</td></tr>
<tr><td>48</td><td>J</td><td>P12_0 / SEG4 / IN1_R</td></tr>
<tr><td>49</td><td>J</td><td>P12_1 / SEG5 / TIN1_R / PPG0_B</td></tr>
<tr><td>50</td><td>J</td><td>P12_2 / SEG6 / TOT1_R / PPG1_B</td></tr>
<tr><td>51</td><td>J</td><td>P12_4 / SEG8</td></tr>
<tr><td>52</td><td>J</td><td>P12_5 / SEG9 / TIN2_R / PPG2_B</td></tr>
<tr><td>53</td><td>J</td><td>P12_6 / SEG10 / TOT2_R / PPG3_B</td></tr>
<tr><td>54</td><td>J</td><td>P12_7 / SEG11 / INT1_R</td></tr>
<tr><td>55</td><td>J</td><td>P01_1 / SEG21 / CKOT1</td></tr>
<tr><td>56</td><td>J</td><td>P01_3 / SEG23</td></tr>
<tr><td>57</td><td>L</td><td>P03_0 / SEG36 / V0</td></tr>
<tr><td>58</td><td>L</td><td>P03_1 / SEG37 / V1</td></tr>
<tr><td>59</td><td>L</td><td>P03_2 / SEG38 / V2</td></tr>
<tr><td>60</td><td>L</td><td>P03_3 / SEG39 / V3</td></tr>
<tr><td>61</td><td>M</td><td>P03_4 / RX0 / INT4</td></tr>
<tr><td>62</td><td>H</td><td>P03_5 / TX0</td></tr>
<tr><td>63</td><td>H</td><td>P03_6 / INT0 / NMI</td></tr>
<tr><td>64</td><td>Supply</td><td>Vcc</td></tr>
</table></td></tr>
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Document History

Document Title: CY96620 Series F²MC-16FX 16-Bit Microcontroller
Document Number: 002-04712

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04712. No change to document contents or format.
*A	5137624	KSUN	02/17/2016	Updated to Cypress format.
*B	5735123	KUME	05/15/2017	Updated the Ordering Information and the Package Dimension For details, please see 18. Major Changes.
*C	5749379	MIYH	05/25/2017	Updated the I/O circuit type and Pin name of 5.Pin Circuit Type For details, please see 18. Major Changes.
*D	5809040	MIYH	07/11/2017	Updated the Ordering Information For details, please see 18. Major Changes.
*E	5978310	MIYH	11/30/2017	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 16. Ordering Information For details, please see 18. Major Changes.