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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	124
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f6416madfd-ua

1.1.2 Performance Overview

Tables 1.1 to 1.4 show the performance overview of the R32C/116A Group.

Table 1.1 Performance Overview for the 176 pin-Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 15.625 ns (f(CPU) = 64 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 512 Kbytes to 1 Mbyte RAM: 96 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	• Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16/32 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 9, key input × 4 Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output) • Automatic timer start function is available
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 61 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 156 CMOS I/O ports • 52 ports are 5 V tolerant • A pull-up resistor is selectable for every 4 input ports (except 5 V tolerant inputs)

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.10 Pin Characteristics for the 176-pin Package (5/5)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
156		P15_6			CLK6	IIO0_6	AN15_6	
157		P15_5			RXD6/SCL6/STXD6	IIO0_5	AN15_5	
158		P15_4			TXD6/SDA6/SRXD6	IIO0_4	AN15_4	
159		P15_3			$\overline{\text{CTS7}}/\overline{\text{RTS7}}$	IIO0_3	AN15_3	
160		P15_2			RXD7	IIO0_2	AN15_2	
161		P15_1			CLK7	IIO0_1	AN15_1	
162	VSS							
163		P15_0			TXD7	IIO0_0	AN15_0	
164	VCC							
165		P10_7	$\overline{\text{KI3}}$				AN_7	
166		P10_6	$\overline{\text{KI2}}$				AN_6	
167		P10_5	$\overline{\text{KI1}}$				AN_5	
168		P10_4	$\overline{\text{KI0}}$				AN_4	
169		P10_3					AN_3	
170		P10_2					AN_2	
171		P10_1					AN_1	
172	AVSS							
173		P10_0					AN_0	
174	VREF							
175	AVCC							
176		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$	

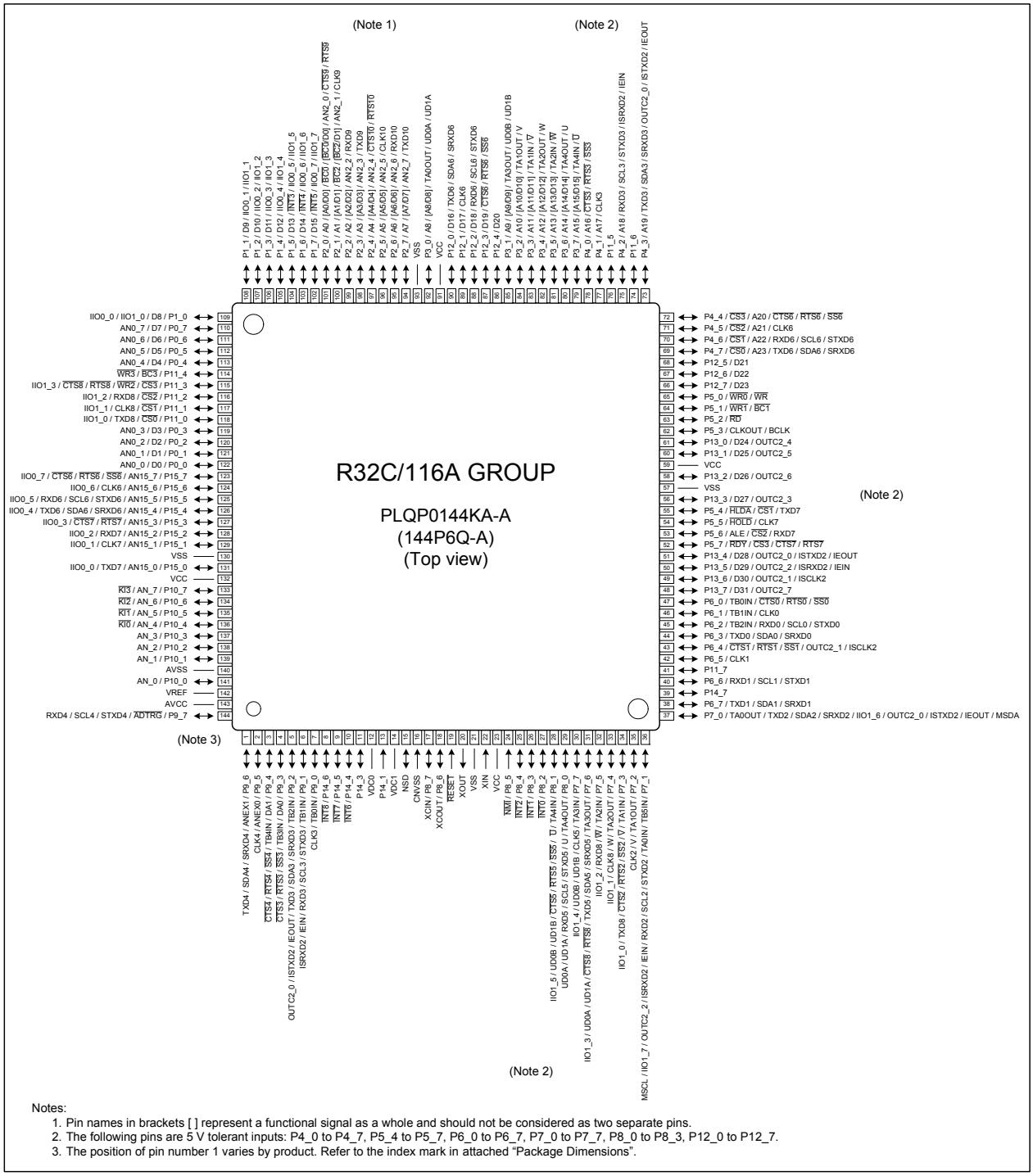


Figure 1.4 Pin Assignment for the 144-pin Package (top view)

Table 1.12 Pin Characteristics for the 144-pin Package (2/4)

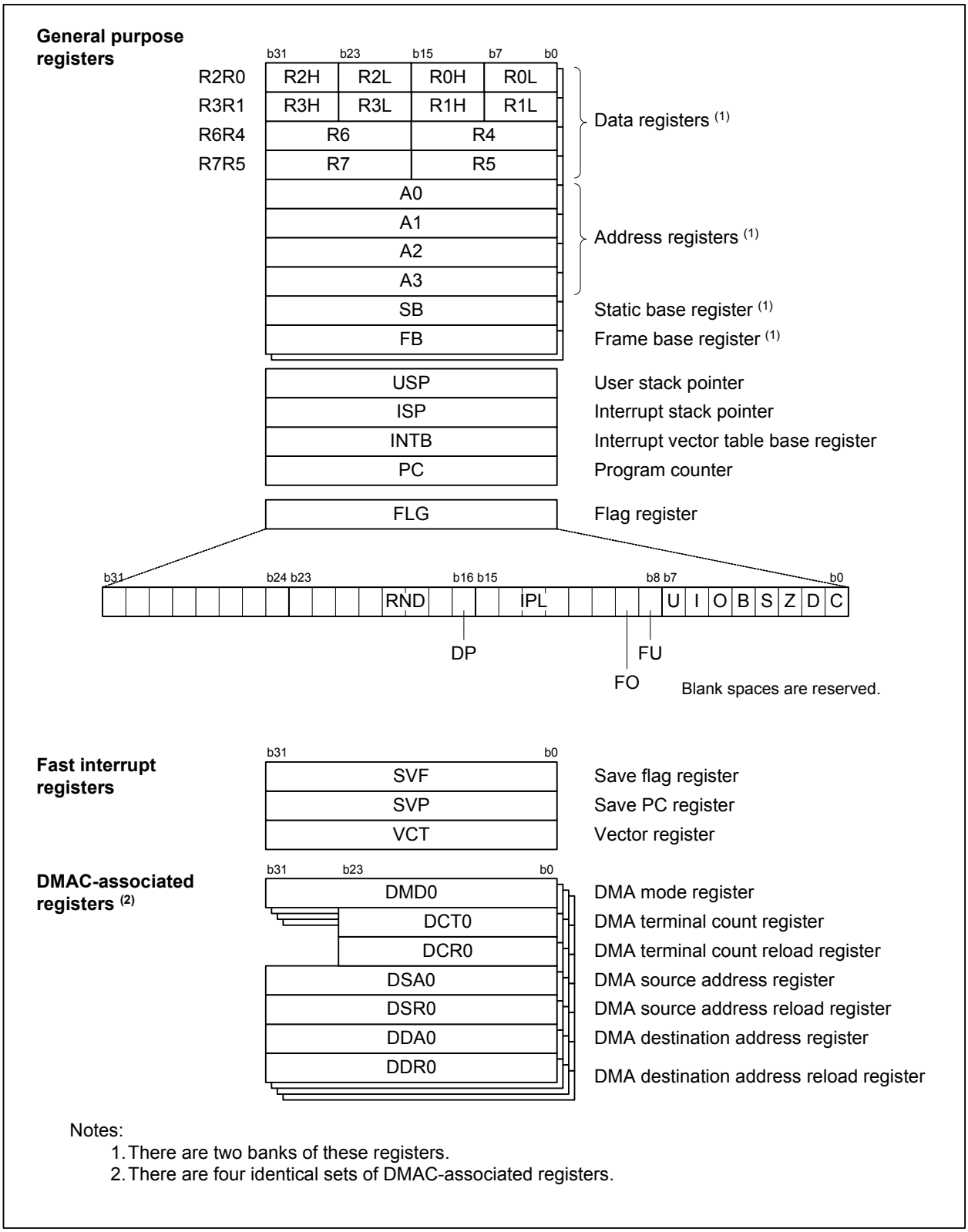
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
37		P7_0		TA0OUT	TXD2/SDA2/SRXD2/ MSDA	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39		P14_7						
40		P6_6			RXD1/SCL1/STXD1			
41		P11_7						
42		P6_5			CLK1			
43		P6_4			$\overline{\text{CTS1}}/\overline{\text{RTS1}}/\overline{\text{SS1}}$	OUTC2_1/ISCLK2		
44		P6_3			TXD0/SDA0/SRXD0			
45		P6_2		TB2IN	RXD0/SCL0/STXD0			
46		P6_1		TB1IN	CLK0			
47		P6_0		TB0IN	$\overline{\text{CTS0}}/\overline{\text{RTS0}}/\overline{\text{SS0}}$			
48		P13_7				OUTC2_7		D31
49		P13_6				OUTC2_1/ISCLK2		D30
50		P13_5				OUTC2_2/ISRXD2/ IEIN		D29
51		P13_4				OUTC2_0/ISTXD2/ IEOUT		D28
52		P5_7			$\overline{\text{CTS7}}/\overline{\text{RTS7}}$			$\overline{\text{RDY}}/\overline{\text{CS3}}$
53		P5_6			RXD7			ALE/$\overline{\text{CS2}}$
54		P5_5			CLK7			$\overline{\text{HOLD}}$
55		P5_4			TXD7			$\overline{\text{HLDA}}/\overline{\text{CS1}}$
56		P13_3				OUTC2_3		D27
57	VSS							
58		P13_2				OUTC2_6		D26
59	VCC							
60		P13_1				OUTC2_5		D25
61		P13_0				OUTC2_4		D24
62		P5_3						CLKOUT/ BCLK
63		P5_2						$\overline{\text{RD}}$
64		P5_1						$\overline{\text{WR1}}/\overline{\text{BC1}}$
65		P5_0						$\overline{\text{WR0}}/\overline{\text{WR}}$
66		P12_7						D23
67		P12_6						D22
68		P12_5						D21
69		P4_7			TXD6/SDA6/SRXD6			$\overline{\text{CS0}}$/A23
70		P4_6			RXD6/SCL6/STXD6			$\overline{\text{CS1}}$/A22
71		P4_5			CLK6			$\overline{\text{CS2}}$/A21
72		P4_4			$\overline{\text{CTS6}}/\overline{\text{RTS6}}/\overline{\text{SS6}}$			$\overline{\text{CS3}}$/A20
73		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
74		P11_6						

Table 1.18 Pin Definitions and Functions (4/4)

Function	Symbol	I/O	Description
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7	I	Analog input for the A/D converter
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_7	O	Output for OC (output compare) of Intelligent I/O group 2
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface
Multi-master I^2C-bus	MSDA	I/O	Serial data input/output
	MSCL	I/O	Transmit/receive clock input/output

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.



Notes:
1. There are two banks of these registers.
2. There are four identical sets of DMAC-associated registers.

Figure 2.1 CPU Registers

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
000141h			
000142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
000143h			
000144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
000145h			
000146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
000147h			
000148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
000149h			
00014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 0000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0000 0000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0000 0000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0000 0000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0000 0000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0000 0000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0000 0000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0000 0000b
000158h			
000159h			
00015Ah			
00015Bh			
00015Ch			
00015Dh			
00015Eh			
00015Fh			
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	0000 0000b
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Base Timer Start Register	BTSR	XXXX 0000b
000165h			
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 RTP Output Buffer Register	G2RTP	00h
000168h			
000169h			
00016Ah	Group 2 Serial Interface Mode Register	G2MR	00XX X000b
00016Bh	Group 2 Serial Interface Control Register	G2CR	0000 X110b
00016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
00016Dh			
00016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
00016Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h	Port P16 Register	P16	XXh
0003E1h	Port P17 Register	P17	XXh
0003E2h	Port P16 Direction Register	PD16	0000 0000b
0003E3h	Port P17 Direction Register	PD17	0000 0000b
0003E4h	Port P18 Register	P18	XXh
0003E5h	Port P19 Register	P19	XXh
0003E6h	Port P18 Direction Register	PD18	0000 0000b
0003E7h	Port P19 Direction Register	PD19	0000 0000b
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX X0XXb
0003F2h	Pull-up Control Register 2	PUR2	X00X XXXXb
0003F3h	Pull-up Control Register 3	PUR3	00XX 0000b
0003F4h	Pull-up Control Register 4	PUR4	0XXX 0000b
0003F5h	Pull-up Control Register 5	PUR5	XXXX 0000b
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	?0XX 0XX0b (1)

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The bit 7 is 0 in the 144-pin package and 1 in the 176-pin package.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0001 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ????b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ????b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h	Block Protect Bit Monitor Register 2	FBPM2	???? ????b (1)
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h			
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The reset value reflects the value of the protect bit for each block in the flash memory.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

Symbol	Characteristic		Condition	Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
V_I	Input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, V_{REF}, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (2)		-0.3 to V_{CC} + 0.3	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3, P12_0 to P12_7, P16_0 to P16_7, P17_0 to P17_3 (2)		-0.3 to 6.0	V
V_O	Output voltage	XOUT, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (2)		-0.3 to V_{CC} + 0.3	V
P_d	Power consumption		T_a = 25°C	500	mW
—	Operating temperature range			-40 to 85	°C
T_{stg}	Storage temperature range			-65 to 150	°C

Notes:
1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Ports P16 to P19 are available in the 176-pin package only.

Table 5.2 Operating Conditions (1/5) (1)

Symbol	Characteristic			Value			Unit
				Min.	Typ.	Max.	
V_{CC}	Digital supply voltage			3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage				V_{CC}		V
V_{REF}	Reference voltage			3.0		V_{CC}	V
V_{SS}	Digital ground voltage				0		V
AV_{SS}	Analog ground voltage				0		V
dV_{CC}/dt	V_{CC} ramp up rate (V_{CC} < 2.0 V)			0.05			V/ms
V_{IH}	High level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)		0.8 × V_{CC}		V_{CC}	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3, P16_0 to P16_7, P17_0 to P17_3 (3)		0.8 × V_{CC}		6.0	V
		P0_0 to P0_7, P1_0 to P1_7, P13_0 to P13_7	in single-chip mode	0.8 × V_{CC}		V_{CC}	V
			in memory expansion mode or microprocessor mode	0.5 × V_{CC}		V_{CC}	V
		P12_0 to P12_7	in single-chip mode	0.8 × V_{CC}		6.0	V
			in memory expansion mode or microprocessor mode	0.5 × V_{CC}		6.0	V
V_{IL}	Low level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)		0		0.2 × V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P12_0 to P12_7, P13_0 to P13_7	in single-chip mode	0		0.2 × V_{CC}	V
			in memory expansion mode or microprocessor mode	0		0.16 × V_{CC}	V
T_{opr}	Operating temperature range	D version		-40		85	°C
		P version		-40		85	°C

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.
3. Ports P16 to P19 are available in the 176-pin package only.

Table 5.4 Operating Conditions (3/5)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	High level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)			-10.0	mA
$I_{OH(avg)}$	High level average output current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)			-5.0	mA
$I_{OL(peak)}$	Low level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)			10.0	mA
$I_{OL(avg)}$	Low level average output current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (3)			5.0	mA

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. The following conditions should be satisfied:
   - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, P10, P11_0 to P11_4, P14_3 to P14_6, P15, P18_2 to P18_7, P19_0, P19_1, P19_6, and P19_7 is 80 mA or less.
   - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, P8_0 to P8_4, P11_5 to P11_7, P12, P13, P14_7, P16, P17, P18_0, P18_1, and P19_2 to P19_5 is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P0, P1, P2, P11_0 to P11_4, P18_2 to P18_7, P19_0, and P19_1 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, P10, P14_3 to P14_6, P15, P19_6, and P19_7 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P3, P4, P5, P11_5, P11_6, P12, P13, P16, P17_0 to P17_3, and P19_2 to P19_5 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P6, P7, P8_0 to P8_4, P11_7, P14_7, P17_4 to P17_7, P18_0, and P18_1 is -40 mA or less.
3. Ports P16 to P19 are available in the 176-pin package only.
4. Average value within 100 ms.

V_{CC} = 5 V

Table 5.15 Electrical Characteristics (1/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	I_{OH} = -5 mA	V_{CC} - 2.0		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	I_{OH} = -200 µA	V_{CC} - 0.3		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	I_{OL} = 200 µA			0.45	V

Note:
1. Ports P16 to P19 are available in the 176-pin package only.

V_{CC} = 5 V

Table 5.16 Electrical Characteristics (2/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $\overline{NMI}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{KI0}$ to $\overline{KI3}$, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{CTS0}$ to $\overline{CTS10}$, CLK0 to CLK10, RXD0 to RXD10, SCL0 to SCL6, SDA0 to SDA6, $\overline{SS0}$ to $\overline{SS6}$, SRXD0 to SRXD6, $\overline{ADTRG}$, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, MSCL, MSDA		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	High level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	V_I = 5 V			5.0	µA
I_{IL}	Low level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P16_0 to P16_7, P17_0 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	V_I = 0 V			-5.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P13_0 to P13_7, P14_1, P14_3 to P14_7, P15_0 to P15_7, P17_4 to P17_7, P18_0 to P18_7, P19_0 to P19_7 (1)	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Note:
1. Ports P16 to P19 are available in the 176-pin package only.

V_{CC} = 3.3 V

Table 5.44 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	V_{REF} = V_{CC} = 3.3 V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		10	MHz
		With sample and hold function		1		10	MHz
$R_{PU(AST)}$	Pull-up resistor for open-circuit detection			5	10	15	kΩ
$R_{PD(AST)}$	Pull-down resistor for open-circuit detection			5	10	15	kΩ

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.48 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.49 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.50 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.51 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.52 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.60 Multi-master I²C-bus Interface

Symbol	Characteristic	Value				Unit
		Standard-mode		Fast-mode		
		Min.	Max.	Min.	Max.	
$t_{w(SCLH)}$	MSCL input high level pulse width	600		600		ns
$t_{w(SCLL)}$	MSCL input low level pulse width	600		600		ns
$t_{r(SCL)}$	MSCL input rise time		1000		300	ns
$t_{f(SCL)}$	MSCL input fall time		300		300	ns
$t_{r(SDA)}$	MSDA input rise time		1000		300	ns
$t_{f(SDA)}$	MSDA input fall time		300		300	ns
$t_{h(SDA-SCL)S}$	MSCL high level hold time after START condition/repeated START condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SCL-SDA)P}$	MSCL high level setup time for repeated START condition/STOP condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{w(SDAH)P}$	MSDA high level pulse width after STOP condition	(1)		4 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SDA-SCL)}$	MSDA input setup time	100		100		ns
$t_{h(SCL-SDA)}$	MSDA input hold time	0		0		ns

Note:

1. The value is calculated using the formulas below based on a value SSC set by bits SSC4 to SSC0 in the I2CSSCR register:

   $t_{h(SDA-SCL)S}$ = SSC ÷ 2 × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{su(SCL-SDA)P}$ = (SSC ÷ 2 + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{w(SDAH)P}$ = (SSC + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

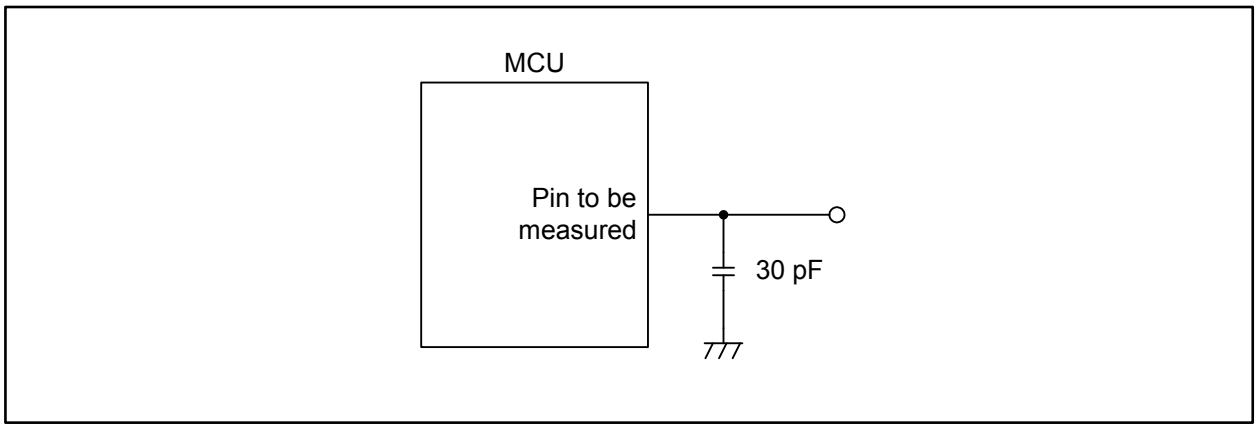


Figure 5.6 Switching Characteristic Measurement Circuit

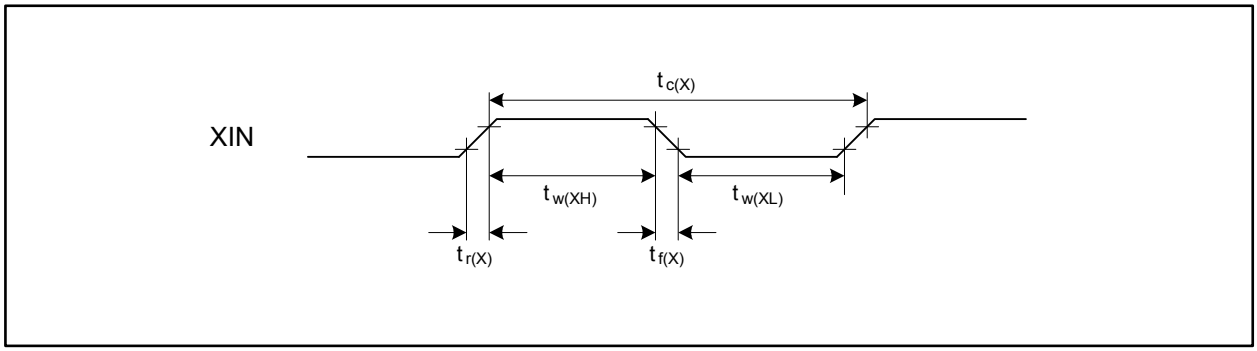
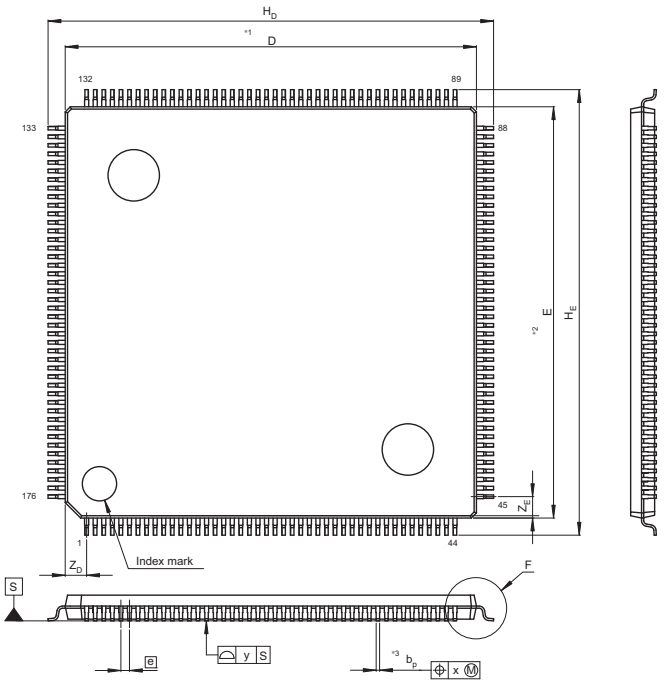
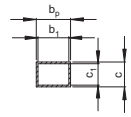


Figure 5.7 External Clock Input Timing

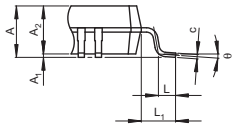
Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—