Microchip Technology - PIC24FJ128GA702T-I/SS Datasheet

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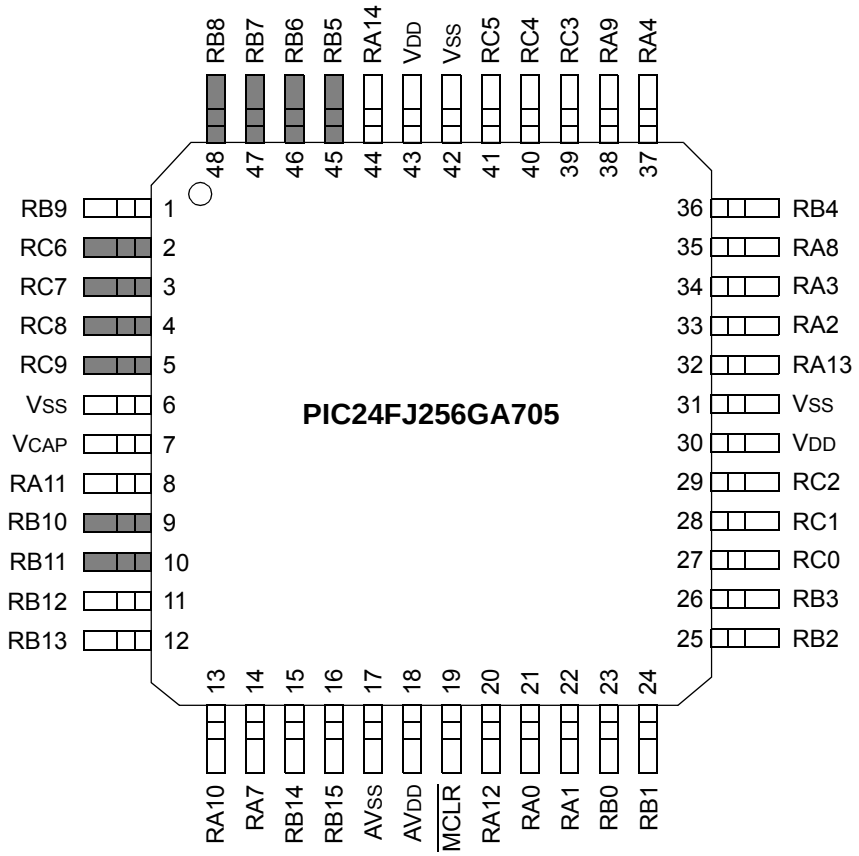
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga702t-i-ss

Pin Diagrams (PIC24FJ256GA705 Devices)

48-Pin TQFP



Legend: See Table 5 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
PGC1	5	2	22	24	I	ST	ICSP™ Programming Clock
PGC2	22	19	9	10	I	ST	
PGC3	15	12	42	46	I	ST	
PGD1	4	1	21	23	I/O	DIG/ST	ICSP Programming Data
PGD2	21	18	8	9	I/O	DIG/ST	
PGD3	14	11	41	45	I/O	DIG/ST	
PMA0	—	—	3	3	I/O	DIG/ST/ TTL	Parallel Master Port Address<0>/ Address Latch Low
PMA1	—	—	2	2	I/O	DIG/ST/ TTL	Parallel Master Port Address<1>/ Address Latch High
PMA2	—	—	12	13	I/O	DIG/ST/ TTL	Parallel Master Port Address<2>
PMA3	—	—	38	41	I/O	DIG/ST/ TTL	Parallel Master Port Address<3>
PMA4	—	—	37	40	I/O	DIG/ST/ TTL	Parallel Master Port Address<4>
PMA5	—	—	4	4	I/O	DIG/ST/ TTL	Parallel Master Port Address<5>
PMA6	—	—	5	5	I/O	DIG/ST/ TTL	Parallel Master Port Address<6>
PMA7	—	—	13	14	I/O	DIG/ST/ TTL	Parallel Master Port Address<7>
PMA8	—	—	32	35	I/O	DIG/ST/ TTL	Parallel Master Port Address<8>
PMA9	—	—	35	38	I/O	DIG/ST/ TTL	Parallel Master Port Address<9>
PMA14/PMCS/ PMCS1	—	—	15	16	I/O	DIG/ST/ TTL	Parallel Master Port Address<14>/ Slave Chip Select/Chip Select 1 Strobe

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

TABLE 4-8: SFR MAP: 0400h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
SPI (CONTINUED)			**I²C (CONTINUED)**	0498	0000
SPI1BUFL	0400	0000	I2C1BRG	0498	0000
SPI1BUFH	0402	0000	I2C1CONL	049A	1000
SPI1BRGL	0404	xxxx	I2C1CONH	049C	0000
SPI1IMSKL	0408	0000	I2C1STAT	049E	0000
SPI1IMSKH	040A	0000	I2C1ADD	04A0	0000
SPI1URDTL	040C	0000	I2C1MSK	04A2	0000
SPI1URDTH	040E	0000	I2C2RCV	04A4	0000
SPI2CON1L	0410	0x00	I2C2TRN	04A6	00FF
SPI2CON1H	0412	0000	I2C2BRG	04A8	0000
SPI2CON2L	0414	0000	I2C2CONL	04AA	1000
SPI2STATL	0418	0028	I2C2CONH	04AC	0000
SPI2STATH	041A	0000	I2C2STAT	04AE	0000
SPI2BUFL	041C	0000	I2C2ADD	04B0	0000
SPI2BUFH	041E	0000	I2C2MSK	04B2	0000
SPI2BRGL	0420	xxxx	**DMA**		
SPI2IMSKL	0424	0000	DMACON	04C4	0000
SPI2IMSKH	0426	0000	DMABUF	04C6	0000
SPI2URDTL	0428	0000	DMAL	04C8	0000
SPI2URDTH	042A	0000	DMAH	04CA	0000
SPI3CON1L	042C	0x00	DMACH0	04CC	0000
SPI3CON1H	042E	0000	DMAINT0	04CE	0000
SPI3CON2L	0430	0000	DMASRC0	04D0	0000
SPI3STATL	0434	0028	DMADST0	04D2	0000
SPI3STATH	0436	0000	DMACNT0	04D4	0001
SPI3BUFL	0438	0000	DMACH1	04D6	0000
SPI3BUFH	043A	0000	DMAINT1	04D8	0000
SPI3BRGL	043C	xxxx	DMASRC1	04DA	0000
SPI3IMSKL	0440	0000	DMADST1	04DC	0000
SPI3IMSKH	0442	0000	DMACNT1	04DE	0001
SPI3URDTL	0444	0000	DMACH2	04E0	0000
SPI3URDTH	0446	0000	DMAINT2	04E2	0000
CONFIGURABLE LOGIC CELL (CLC)			DMASRC2	04E4	0000
CLC1CONL	0464	0000	DMADST2	04E6	0000
CLC1CONH	0466	0000	DMACNT2	04E8	0001
CLC1SEL	0468	0000	DMACH3	04EA	0000
CLC1GLSL	046C	0000	DMAINT3	04EC	0000
CLC1GLSH	046E	0000	DMASRC3	04EE	0000
CLC2CONL	0470	0000	DMADST3	04F0	0000
CLC2CONH	0472	0000	DMACNT3	04F2	0001
CLC2SEL	0474	0000	DMACH4	04F4	0000
CLC2GLSL	0478	0000	DMAINT4	04F6	0000
CLC2GLSH	047A	0000	DMASRC4	04F8	0000
I²C			DMADST4	04FA	0000
I2C1RCV	0494	0000	DMACNT4	04FC	0001
I2C1TRN	0496	00FF	DMACH5	04FE	0000

Legend: x = undefined. Reset values are shown in hexadecimal.

REGISTER 5-1: DMACON: DMA ENGINE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMAEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PRSSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DMAEN:** DMA Module Enable bit
1 = Enables module
0 = Disables module and terminates all active DMA operation(s)

bit 14-1 **Unimplemented:** Read as ‘0’

bit 0 **PRSSEL:** Channel Priority Scheme Selection bit
1 = Round-robin scheme
0 = Fixed priority scheme

EXAMPLE 6-2: INITIATING A PROGRAMMING SEQUENCE

```
        DISI    #5                      ; Block all interrupts with priority <7
                                        ; for next 5 instructions
        MOV.B   #0x55, W0
        MOV     W0, NVMKEY              ; Write the 0x55 key
        MOV.B   #0xAA, W1               ;
        MOV     W1, NVMKEY              ; Write the 0xAA key
        BSET    NVMCON, #WR             ; Start the programming sequence
        NOP                             ; Required delays
        NOP
        BTSC    NVMCON, #15             ; and wait for it to be
        BRA     $-2                     ; completed
```

REGISTER 9-8: REFOTRIML: REFERENCE OSCILLATOR TRIM REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<0:7>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ROTRIM8	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **ROTRIM<0:8>:** REFO Trim bits

These bits provide a fractional additive to the RODIVx value for the 1/2 period of the REFO clock.
000000000 = 0/512 (0.0 divisor added to the RODIVx value)
000000001 = 1/512 (0.001953125 divisor added to the RODIVx value)
000000010 = 2/512 (0.00390625 divisor added to the RODIVx value)
•
•
•
100000000 = 256/512 (0.5000 divisor added to the RODIVx value)
•
•
•
111111110 = 510/512 (0.99609375 divisor added to the RODIVx value)
111111111 = 511/512 (0.998046875 divisor added to the RODIVx value)

bit 6-0 **Unimplemented:** Read as ‘0’

TABLE 11-3: PORTA PIN AND ANSELx AVAILABILITY

Device	PORTA I/O Pins															
	RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
PIC24FJXXXGA705	—	X	X	X	X	X	X	X	X	—	—	X	X	X	X	X
PIC24FJXXXGA704	—	—	—	—	—	X	X	X	X	—	—	X	X	X	X	X
PIC24FJXXXGA702	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X
ANSELA bit present	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X

TABLE 11-4: PORTB PIN AND ANSELx AVAILABILITY

Device	PORTB I/O Pins															
	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
PIC24FJXXXGA705	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PIC24FJXXXGA704	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PIC24FJXXXGA702	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ANSELB bit present	X	X	X	X	—	—	X	—	—	—	—	—	X	X	X	X

TABLE 11-5: PORTC PIN AND ANSELx AVAILABILITY

Device	PORTC I/O Pins															
	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
PIC24FJXXXGA705	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X
PIC24FJXXXGA704	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X
PIC24FJXXXGA702	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ANSELC bit present	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X

REGISTER 11-34: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP5R5	RP5R4	RP5R3	RP5R2	RP5R1	RP5R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP5R<5:0>:** RP5 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP5 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP4R<5:0>:** RP4 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP4 (see Table 11-7 for peripheral function numbers).

REGISTER 11-35: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP7R<5:0>:** RP7 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP7 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP6R<5:0>:** RP6 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP6 (see Table 11-7 for peripheral function numbers).

REGISTER 11-38: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP13R5	RP13R4	RP13R3	RP13R2	RP13R1	RP13R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP12R5	RP12R4	RP12R3	RP12R2	RP12R1	RP12R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP13R<5:0>:** RP13 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP13 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP12R<5:0>:** RP12 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP12 (see Table 11-7 for peripheral function numbers).

REGISTER 11-39: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP15R5	RP15R4	RP15R3	RP15R2	RP15R1	RP15R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP14R5	RP14R4	RP14R3	RP14R2	RP14R1	RP14R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP15R<5:0>:** RP15 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP15 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP14R<5:0>:** RP14 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP14 (see Table 11-7 for peripheral function numbers).

REGISTER 11-46: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0
bit 7							bit 0

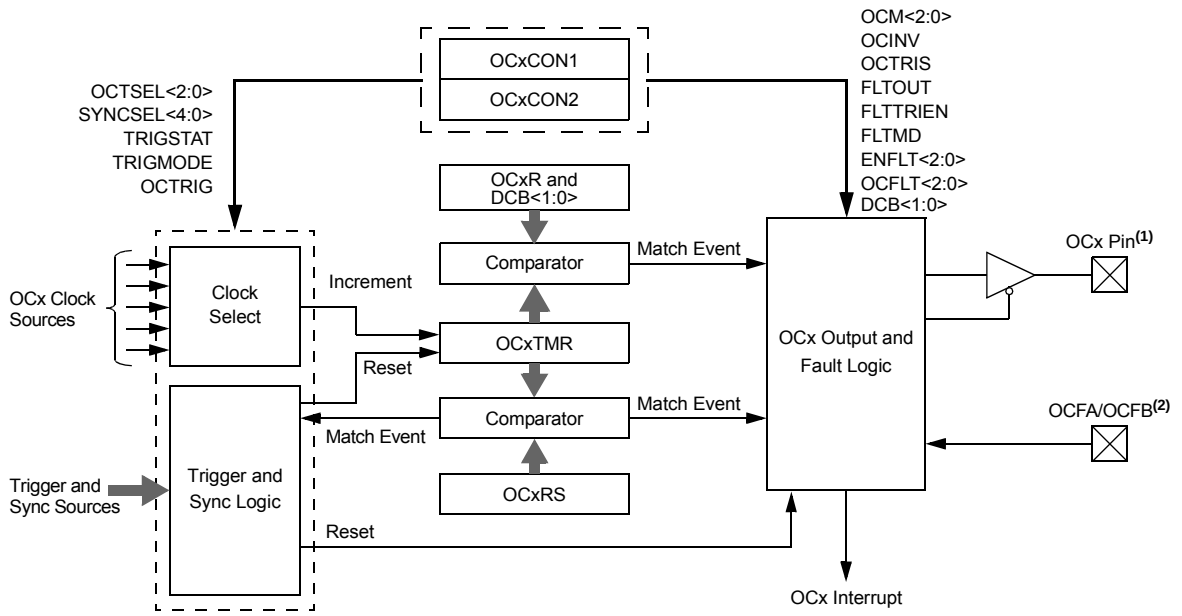
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP28R<5:0>:** RP28 Output Pin Mapping bits

Peripheral Output Number n is assigned to pin, RP28 (see Table 11-7 for peripheral function numbers).

FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

15.2 Compare Operations

In Compare mode (Figure 15-1), the output compare module can be configured for Single-Shot or Continuous mode pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins if available on the OCx module you are using. Otherwise, configure the dedicated OCx output pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate the time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= `0xx`).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure Trigger mode operation and TRIGSTAT to select a hardware or software trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the Trigger or Sync source. If free-running timer operation is required, set the SYNCSELx bits to '`00000`' (no Sync/Trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bit for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a Trigger source event occurs.

REGISTER 16-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT<5:0>:** CCPx Dead-Time Select bits(1)

111111 = Inserts 63 dead-time delay periods between complementary output signals
111110 = Inserts 62 dead-time delay periods between complementary output signals
...
000010 = Inserts 2 dead-time delay periods between complementary output signals
000001 = Inserts 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in the MCCP1 module only.

REGISTER 17-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

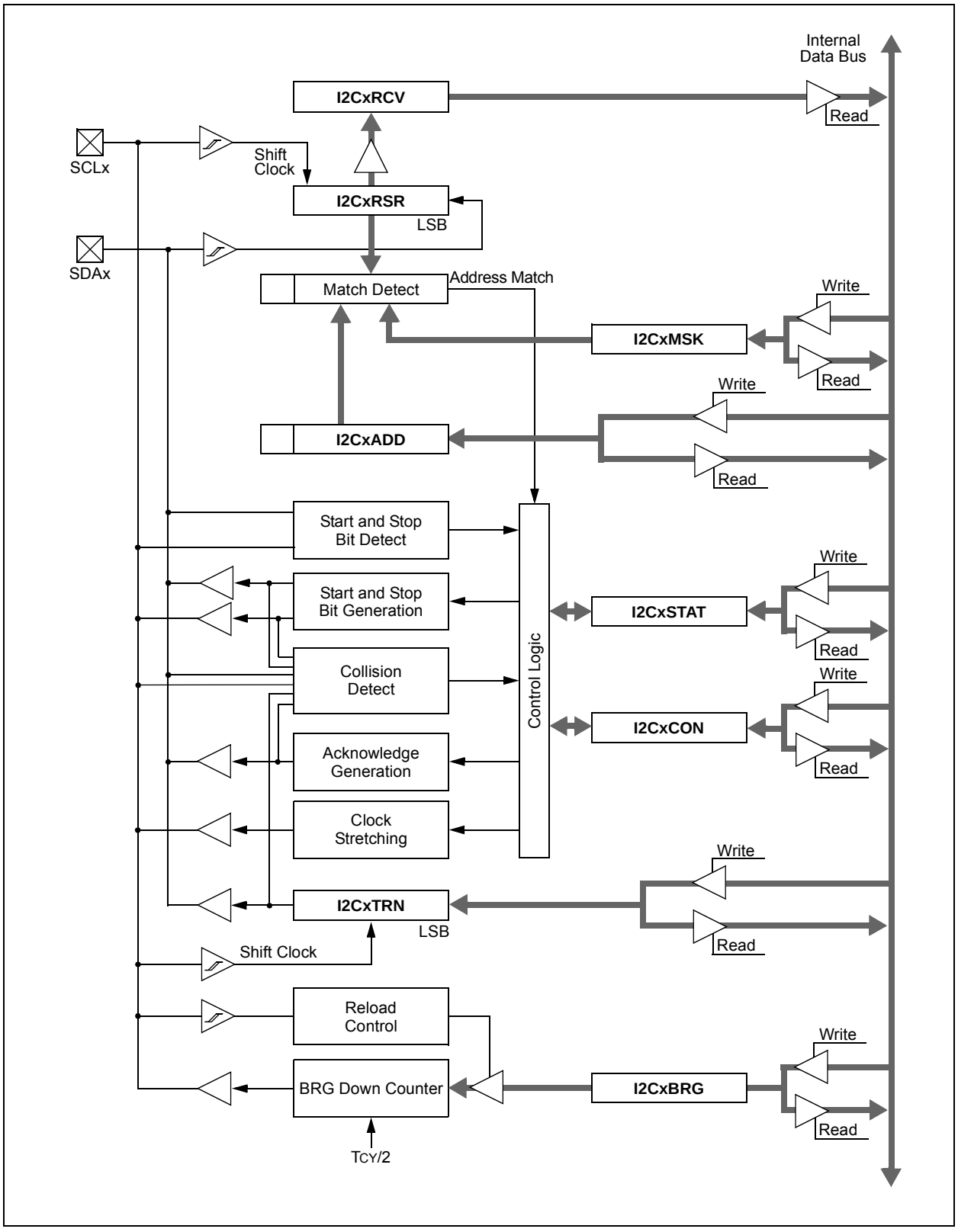
bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.
2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

FIGURE 18-1: I2Cx BLOCK DIAGRAM



REGISTER 25-1: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 THROUGH 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0, HS	R-0, HSC
CEN	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CEN:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	2	None
TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK		Unlink Frame Pointer	1	1	None
XOR	XOR	f	f = f .XOR. WREG	1	1	N, Z
	XOR	f,WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

NOTES:

TABLE 32-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.0	—	3.6	V	BOR is disabled
			VBOR	—	3.6	V	BOR is enabled
DC12	VDR	**RAM Data Retention Voltage(1)**	Greater of: VPORREL or VBOR	—	—	V	VBOR is used only if BOR is enabled (BOREN = 1)
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	—	V	**(Note 2)**
DC17A	SVDD	**Recommended VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1V/20 ms	—	1V/10 µS	sec	**(Note 2, Note 4)**
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	2.1	2.2	V	**(Note 3)**

Note 1: This is the limit to which VDD may be lowered and the RAM contents will always be retained.

2: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

3: On a rising VDD power-up sequence, application firmware execution begins at the higher of the VPORREL or VBOR level (when BOREN = 1).

4: VDD rise times outside this window may not internally reset the processor and are not parametrically tested.

TABLE 32-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR	TVREG	Voltage Regulator Start-up Time	—	10	—	μs	VREGS = 0 with any POR or BOR
DVR10	VBG	Internal Band Gap Reference	1.14	1.2	1.26	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	1.6	1.8	2.0	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	10	—	—	μF	Series resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

TABLE 32-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0100(1)	3.45	—	3.73	V	
			HLVDL<3:0> = 0101	3.25	—	3.58	V	
			HLVDL<3:0> = 0110	2.95	—	3.25	V	
			HLVDL<3:0> = 0111	2.75	—	3.04	V	
			HLVDL<3:0> = 1000	2.65	—	2.92	V	
			HLVDL<3:0> = 1001	2.45	—	2.70	V	
			HLVDL<3:0> = 1010	2.35	—	2.60	V	
			HLVDL<3:0> = 1011	2.25	—	2.49	V	
			HLVDL<3:0> = 1100	2.15	—	2.39	V	
			HLVDL<3:0> = 1101	2.08	—	2.28	V	
			HLVDL<3:0> = 1110	2.00	—	2.15	V	
DC101	VTHL	HLVD Voltage on HLVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.20	—	V	
DC105	TONLVD	HLVD Module Enable Time		—	5	—	μS	From POR or HLVDEN = 1

Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0011', are not implemented.

TABLE 32-24: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 2.2	—	Lesser of: VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
Analog Inputs							
AD10	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	**(Note 2)**
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/3	V	
AD13		Leakage Current	—	±1.0	±610	nA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V, Source Impedance = 2.5 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	2.5K	Ω	10-bit
A/D Accuracy							
AD20B	Nr	Resolution	—	12	—	bits	
AD21B	INL	Integral Nonlinearity	—	±1	< ±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD22B	DNL	Differential Nonlinearity	—	—	< ±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD23B	GERR	Gain Error	—	±1	±4	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD24B	EOFF	Offset Error	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD25B		Monotonicity(1)	—	—	—	—	Guaranteed

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

2: Measurements are taken with the external VREF+ and VREF- used as the A/D voltage reference.