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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga704-i-pt

PIC24FJ256GA705 FAMILY

TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator				I/O	Input Buffer	Description
	28-Pin SOIC, SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
PGC1	5	2	22	24	I	ST	ICSP™ Programming Clock
PGC2	22	19	9	10	I	ST	
PGC3	15	12	42	46	I	ST	
PGD1	4	1	21	23	I/O	DIG/ST	ICSP Programming Data
PGD2	21	18	8	9	I/O	DIG/ST	
PGD3	14	11	41	45	I/O	DIG/ST	
PMA0	—	—	3	3	I/O	DIG/ST/TTL	Parallel Master Port Address<0>/Address Latch Low
PMA1	—	—	2	2	I/O	DIG/ST/TTL	Parallel Master Port Address<1>/Address Latch High
PMA2	—	—	12	13	I/O	DIG/ST/TTL	Parallel Master Port Address<2>
PMA3	—	—	38	41	I/O	DIG/ST/TTL	Parallel Master Port Address<3>
PMA4	—	—	37	40	I/O	DIG/ST/TTL	Parallel Master Port Address<4>
PMA5	—	—	4	4	I/O	DIG/ST/TTL	Parallel Master Port Address<5>
PMA6	—	—	5	5	I/O	DIG/ST/TTL	Parallel Master Port Address<6>
PMA7	—	—	13	14	I/O	DIG/ST/TTL	Parallel Master Port Address<7>
PMA8	—	—	32	35	I/O	DIG/ST/TTL	Parallel Master Port Address<8>
PMA9	—	—	35	38	I/O	DIG/ST/TTL	Parallel Master Port Address<9>
PMA14/PMCS/PMCS1	—	—	15	16	I/O	DIG/ST/TTL	Parallel Master Port Address<14>/Slave Chip Select/Chip Select 1 Strobe

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I²C = I²C/SMBus input buffer
XCVR = Dedicated Transceiver

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FJ256GA705 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 “Power Supply Pins”**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used (see **Section 2.2 “Power Supply Pins”**)
- MCLR pin (see **Section 2.3 “Master Clear (MCLR) Pin”**)
- VCAP pin (see **Section 2.4 “Voltage Regulator Pin (VCAP)”**)

These pins must also be connected if they are being used in the end application:

- PGCx/PGDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 “ICSP Pins”**)
- OSCI and OSCO pins when an external oscillator source is used (see **Section 2.6 “External Oscillator Pins”**)

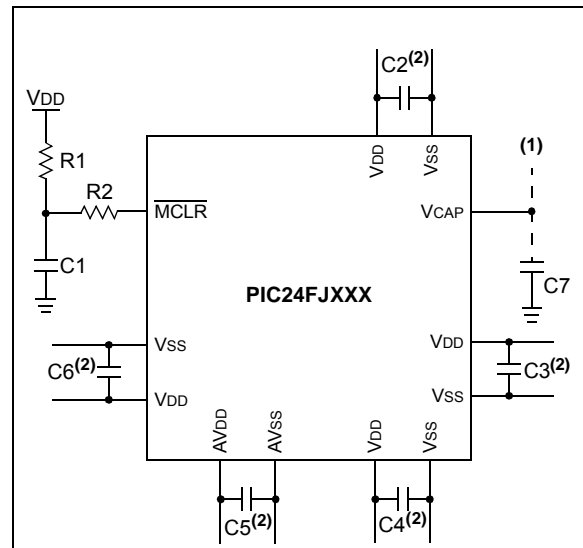
Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for analog modules is implemented

Note: The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 μ F, 50V ceramic

C7: 10 μ F, 16V or greater, ceramic

R1: 10 k Ω

R2: 100 Ω to 470 Ω

Note 1: See **Section 2.4 “Voltage Regulator Pin (VCAP)”** for an explanation of voltage regulator pin connections.

2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the “dsPIC33/PIC24 Family Reference Manual”, “**CPU with Extended Data Space (EDS)**” (DS39732), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the REPEAT instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The lower 32 Kbytes of the Data Space (DS) can be accessed linearly. The upper 32 Kbytes of the Data Space are referred to as Extended Data Space (EDS), to which the extended data RAM, EPMP memory space or program memory can be mapped.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct Addressing modes along with three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (that is, $A + B = C$) to be executed in a single cycle.

A high-speed, 17-bit x 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit x 16-bit or 8-bit x 8-bit, integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the REPEAT instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit, integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to 8 sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is shown in Figure 3-1.

3.1 Programmer's Model

The programmer's model for the PIC24F is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions.

A description of each register is provided in Table 3-1. All registers associated with the programmer's model are memory-mapped.

4.2.5.1 Data Read from EDS

In order to read the data from the EDS space, first, an Address Pointer is set up by loading the required EDS page number into the DSRPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, the EDS window is enabled by setting bit 15 of the Working register which is assigned with the offset address; then, the contents of the pointed EDS location can be read.

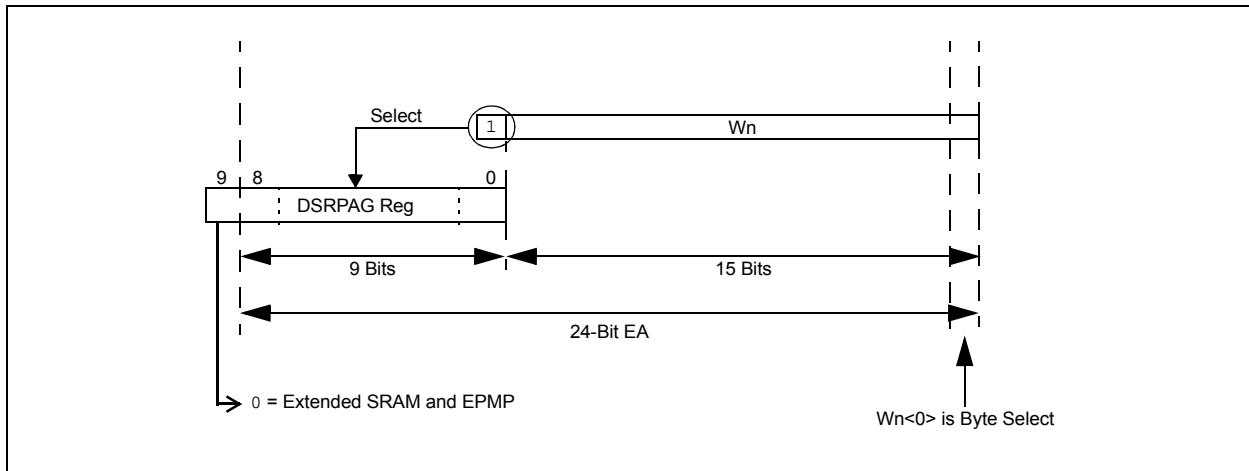
Figure 4-4 illustrates how the EDS space address is generated for read operations.

When the Most Significant bit (MSb) of EA is '1' and DSRPAG<9> = 0, the lower 9 bits of DSRPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS space address for read operations.

Example 4-1 shows how to read a byte, word and double word from EDS.

Note: All read operations from EDS space have an overhead of one instruction cycle. Therefore, a minimum of two instruction cycles are required to complete an EDS read. EDS reads under the `REPEAT` instruction; the first two accesses take three cycles and the subsequent accesses take one cycle.

FIGURE 4-4: EDS ADDRESS GENERATION FOR READ OPERATIONS



EXAMPLE 4-1: EDS READ CODE IN ASSEMBLY

```
; Set the EDS page from where the data to be read
mov    #0x0002, w0
mov    w0, DSRPAG    ;page 2 is selected for read
mov    #0x0800, w1    ;select the location (0x800) to be read
bset   w1, #15        ;set the MSB of the base address, enable EDS mode

;Read a byte from the selected location
mov.b  [w1++], w2     ;read Low byte
mov.b  [w1++], w3     ;read High byte

;Read a word from the selected location
mov    [w1], w2       ;

;Read Double - word from the selected location
mov.d  [w1], w2       ;two word read, stored in w2 and w3
```

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TABLE 8-2: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	IRQ #	IVT Address	Interrupt Bit Location		
			Flag	Enable	Priority
PMP – Parallel Master Port	45	00006Eh	IFS2<13>	IEC2<13>	PMPInterrupt
DMA4 – Direct Memory Access 4	46	000070h	IFS2<14>	IEC2<14>	DMA4Interrupt
—	47	—	—	—	—
—	48	—	—	—	—
SI2C2 – I2C2 Slave Events	49	000076h	IFS3<1>	IEC3<1>	SI2C2Interrupt
MI2C2 – I2C2 Master Events	50	000078h	IFS3<2>	IEC3<2>	MI2C2Interrupt
—	51	—	—	—	—
—	52	—	—	—	—
INT3 – External Interrupt 3	53	00007Eh	IFS3<5>	IEC3<5>	INT3Interrupt
INT4 – External Interrupt 4	54	000080h	IFS3<6>	IEC3<6>	INT4Interrupt
—	55	—	—	—	—
—	56	—	—	—	—
—	57	—	—	—	—
SPI1RX – SPI1 Receive Done	58	000088h	IFS3<10>	IEC3<10>	SPI1RXInterrupt
SPI2RX – SPI2 Receive Done	59	00008Ah	IFS3<11>	IEC3<11>	SPI2RXInterrupt
SPI3RX – SPI3 Receive Done	60	00008Ch	IFS3<12>	IEC3<12>	SPI3RXInterrupt
DMA5 – Direct Memory Access 5	61	00008Eh	IFS3<13>	IEC3<13>	DMA5Interrupt
RTCC – Real-Time Clock and Calendar	62	000090h	IFS3<14>	IEC3<14>	RTCCInterrupt
CCP1 – Capture/Compare 1	63	000092h	IFS3<15>	IEC3<15>	CCP1Interrupt
CCP2 – Capture/Compare 2	64	000094h	IFS4<0>	IEC4<0>	CCP2Interrupt
U1E – UART1 Error	65	000096h	IFS4<1>	IEC4<1>	U1EInterrupt
U2E – UART2 Error	66	000098h	IFS4<2>	IEC4<2>	U2EInterrupt
CRC – Cyclic Redundancy Check	67	00009Ah	IFS4<3>	IEC4<3>	CRCInterrupt
—	68	—	—	—	—
—	69	—	—	—	—
—	70	—	—	—	—
—	71	—	—	—	—
HLVD – High/Low-Voltage Detect	72	0000A4h	IFS4<8>	IEC4<8>	HLVDInterrupt
—	73	—	—	—	—
—	74	—	—	—	—
—	75	—	—	—	—
—	76	—	—	—	—
CTMU – Interrupt	77	0000AEh	IFS4<13>	IEC4<13>	CTMUInterrupt
—	78	—	—	—	—
—	79	—	—	—	—
—	80	—	—	—	—
—	81	—	—	—	—
—	82	—	—	—	—
—	83	—	—	—	—

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REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IC3MD	IC2MD	IC1MD
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	OC3MD	OC2MD	OC1MD
bit 7					bit 0		

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **IC3MD:** Input Capture 3 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled
- bit 9 **IC2MD:** Input Capture 2 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled
- bit 8 **IC1MD:** Input Capture 1 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled
- bit 7-3 **Unimplemented:** Read as '0'
- bit 2 **OC3MD:** Output Capture 3 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled
- bit 1 **OC2MD:** Output Capture 2 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled
- bit 0 **OC1MD:** Output Capture 1 Module Disable bit
 - 1 = Module is disabled
 - 0 = Module power and clock sources are enabled

PIC24FJ256GA705 FAMILY

REGISTER 11-10: IOCFx: INTERRUPT-ON-CHANGE FLAG x REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
IOCFx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCFx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **IOCFx<15:0>**: Interrupt-on-Change Flag x bits

1 = An enabled change was detected on the associated pin; set when IOCPx = 1 and a positive edge was detected on the IOCx pin, or when IOCNx = 1 and a negative edge was detected on the IOCx pin

0 = No change was detected or the user cleared the detected change

Note 1: It is not possible to set the IOCFx register bits with software writes (as this would require the addition of significant logic). To test IOC interrupts, it is recommended to enable the IOC functionality on one or more GPIO pins and then use the corresponding LATx register bit(s) to trigger an IOC interrupt.

2: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-11: IOCPUx: INTERRUPT-ON-CHANGE PULL-UP ENABLE x REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
IOCPUx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCPUx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **IOCPUx<15:0>**: Interrupt-on-Change Pull-up Enable x bits

1 = Pull-up is enabled

0 = Pull-up is disabled

Note 1: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

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REGISTER 11-17: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **ICM2R<5:0>:** Input Capture Mode 2 bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ICM1R<5:0>:** Input Capture Mode 1 bits

REGISTER 11-18: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ICM4R5	ICM4R4	ICM4R3	ICM4R2	ICM4R1	ICM4R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ICM3R5	ICM3R4	ICM3R3	ICM3R2	ICM3R1	ICM3R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **ICM4R<5:0>:** Input Capture Mode 4 bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ICM3R<5:0>:** Input Capture Mode 3 bits

16.2 General Purpose Timer

Timer mode is selected when CCSEL = 0 and MOD<3:0> = 0000. The timer can function as a 32-bit timer or a dual 16-bit timer, depending on the setting of the T32 bit (Table 16-1).

TABLE 16-1: TIMER OPERATION MODE

T32 (CCPxCON1L<5>)	Operating Mode
0	Dual Timer Mode (16-bit)
1	Timer Mode (32-bit)

Dual 16-Bit Timer mode provides a simple timer function with two independent 16-bit timer/counters. The primary timer uses the CCPxTMRL and CCPxPRL registers. Only the primary timer can interact with other modules on the device. It generates the MCCPx Sync out signals for use by other MCCPx modules. It can also use the SYNC<4:0> bits signal generated by other modules.

The secondary timer uses the CCPxTMRH and CCPxPRH registers. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an output Sync/Trigger signal like the primary time base. In Dual Timer mode, the Timer Period High register, CCPxPRH, generates the MCCPx compare event (CCPxIF) used by many other modules on the device.

The 32-Bit Timer mode uses the CCPxTMRL and CCPxTMRH registers, together, as a single 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments

by one. This mode provides a simple timer function when it is important to track long time periods. Note that the T32 bit (CCPxCON1L<5>) should be set before the CCPxTMRL or CCPxPRH registers are written to initialize the 32-bit timer.

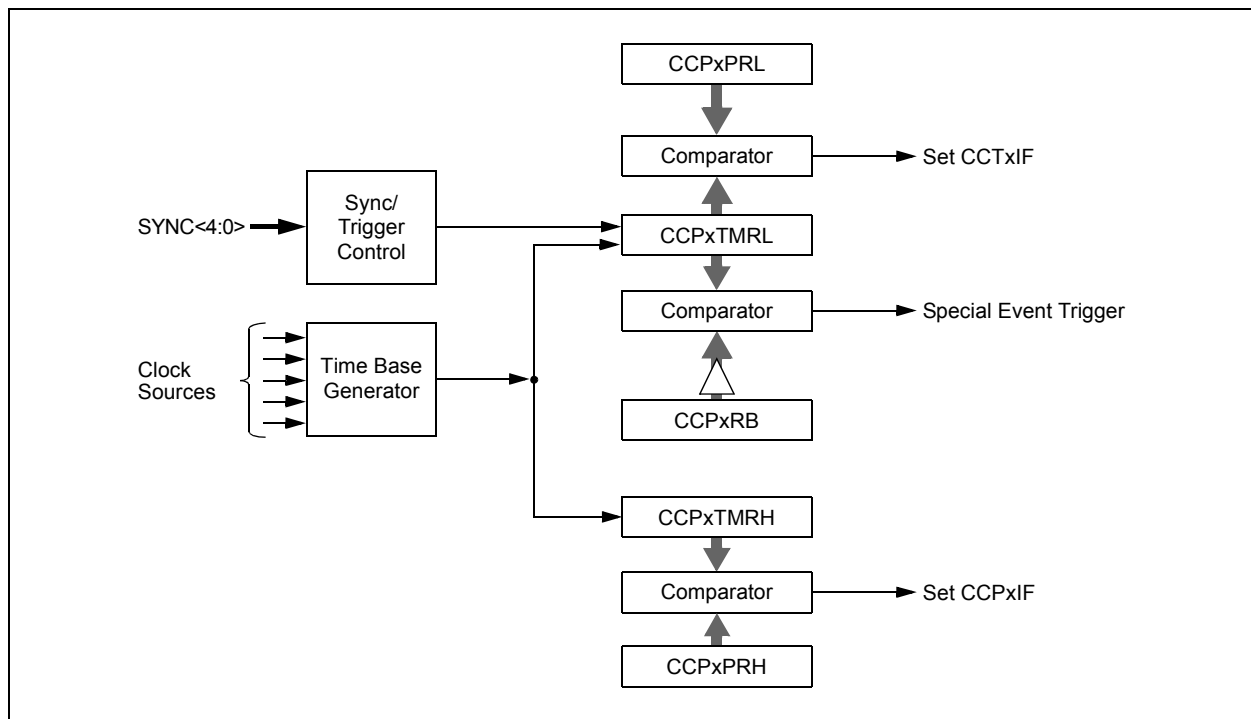
16.2.1 SYNC AND TRIGGER OPERATION

In both 16-bit and 32-bit modes, the timer can also function in either Synchronization ("Sync") or Trigger mode operation. Both use the SYNC<4:0> bits (CCPxCON1H<4:0>) to determine the input signal source. The difference is how that signal affects the timer.

In Sync operation, the Timer Reset or clear occurs when the input selected by SYNC<4:0> is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H<7>) is cleared. The SYNC<4:0> bits can have any value except '11111'.

In Trigger mode operation, the timer is held in Reset until the input selected by SYNC<4:0> is asserted; when it occurs, the timer starts counting. Trigger operation is used whenever the TRIGEN bit is set. In Trigger mode, the timer will continue running after a trigger event as long as the CCPTRIG bit (CCPxSTATL<7>) is set. To clear CCPTRIG, the TRCLR bit (CCPxSTATL<5>) must be set to clear the trigger event, reset the timer and hold it at zero until another trigger event occurs. On PIC24FJ256GA705 family devices, Trigger mode operation can only be used when the system clock is the time base source (CLKSEL<2:0> = 000).

FIGURE 16-3: DUAL 16-BIT TIMER MODE



REGISTER 18-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 8	SMEN: SMBus Input Levels Enable bit 1 = Enables input logic so thresholds are compliant with the SMBus specification 0 = Disables SMBus-specific inputs
bit 7	GCEN: General Call Enable bit (I ² C Slave mode only) 1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception 0 = General call address is disabled
bit 6	STREN: SCLx Clock Stretch Enable bit In I ² C Slave mode only; used in conjunction with the SCLREL bit. 1 = Enables clock stretching 0 = Disables clock stretching
bit 5	ACKDT: Acknowledge Data bit In I ² C Master mode during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive. In I ² C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception. 1 = NACK is sent 0 = ACK is sent
bit 4	ACKEN: Acknowledge Sequence Enable bit In I ² C Master mode only; applicable during Master Receive mode. 1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits the ACKDT data bit 0 = Acknowledge sequence is Idle
bit 3	RCEN: Receive Enable bit (I ² C Master mode only) 1 = Enables Receive mode for I ² C; automatically cleared by hardware at the end of the 8-bit receive data byte 0 = Receive sequence is not in progress
bit 2	PEN: Stop Condition Enable bit (I ² C Master mode only) 1 = Initiates Stop condition on the SDAx and SCLx pins 0 = Stop condition is Idle
bit 1	RSEN: Restart Condition Enable bit (I ² C Master mode only) 1 = Initiates Restart condition on the SDAx and SCLx pins 0 = Restart condition is Idle
bit 0	SEN: Start Condition Enable bit (I ² C Master mode only) 1 = Initiates Start condition on the SDAx and SCLx pins 0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception. The user software must provide a delay between writing to the transmit buffer and setting the SCLREL bit. This delay must be greater than the minimum setup time for slave transmissions, as specified in **Section 32.0 "Electrical Characteristics"**.

2: Automatically cleared to '0' at the beginning of slave transmission.

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REGISTER 20-9: PADCON: PAD CONFIGURATION CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
IOCON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PMPTTL
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **IOCON:** Used for Non-PMP functionality

bit 14-1 **Unimplemented:** Read as '0'

bit 0 **PMPTTL:** EPMP Module TTL Input Buffer Select bit

1 = EPMP module inputs (PMDx, PMCS1) use TTL input buffers

0 = EPMP module inputs use Schmitt Trigger input buffers

21.2 RTCC Module Registers

The RTCC module registers are organized into four categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers
- Timestamp Registers

21.2.1 REGISTER MAPPING

Previous RTCC implementations used a Register Pointer to access the RTCC Time and Date registers, as well as the Alarm Time and Date registers. These Registers are now mapped to memory and are individually addressable.

21.2.2 WRITE LOCK

To prevent spurious changes to the Time Control or Time Value registers, the WRLOCK bit (RTCCON1L<11>) must be cleared ('0'). The POR default state is when the WRLOCK bit is '0' and is cleared on any device Reset (POR, BOR, MCLR). It is recommended that the WRLOCK bit be set to '1' after the Date and Time registers are properly initialized, and after the RTCEN bit (RTCCON1L<15>) has been set.

Any attempt to write to the RTCEN bit, the RTCCON2L/H registers, or the Date or Time registers, will be ignored as long as WRLOCK is '1'. The Alarm, Power Control and Timestamp registers can be changed when WRLOCK is '1'.

Clearing the WRLOCK bit requires an unlock sequence after it has been written to a '1', writing two bytes consecutively to the NVMKEY register. A sample assembly sequence is shown in Example 21-1. If WRLOCK is already cleared, it can be set to '1' without using the unlock sequence.

Note: To avoid accidental writes to the timer, it is recommended that the WRLOCK bit (RTCCON1L<11>) is kept clear at any other time. For the WRLOCK bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of WRLOCK; therefore, it is recommended that code follow the procedure in Example 21-1.

21.2.3 SELECTING RTCC CLOCK SOURCE

The clock source for the RTCC module can be selected using the CLKSEL<1:0> bits in the RTCCON2L register. When the bits are set to '00', the Secondary Oscillator (SOSC) is used as the reference clock and when the bits are '01', LPRC is used as the reference clock. When CLKSEL<1:0> = 10, the external power-line (50 Hz and 60 Hz) is used as the clock source. When CLKSEL<1:0> = 11, the system clock is used as the clock source.

EXAMPLE 21-1: SETTING THE WRLOCK BIT

```
DISI    #6                      ;disable interrupts for 6 instructions
MOV     #NVMKEY, W1
MOV     #0x55, W2                ; first unlock code
MOV     W2, [W1]                 ; write first unlock code
MOV     #0xAA, W3                ; second unlock sequence
MOV     W3, [W1]                 ; write second unlock sequence
BCLR    RTCCON1L, #WRLOCK        ; clear the WRLOCK bit
```

FIGURE 23-3: CLCx INPUT SOURCE SELECTION DIAGRAM

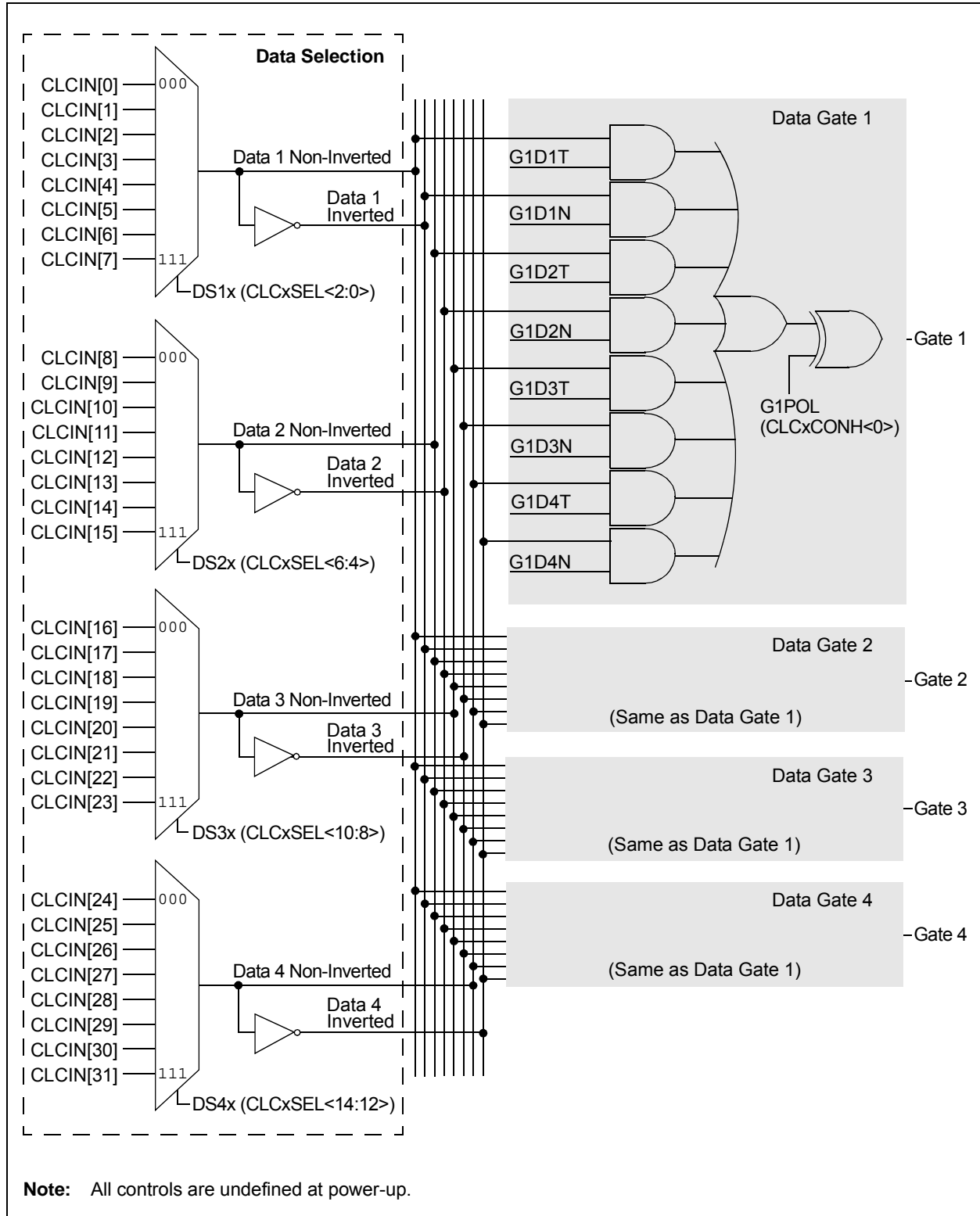
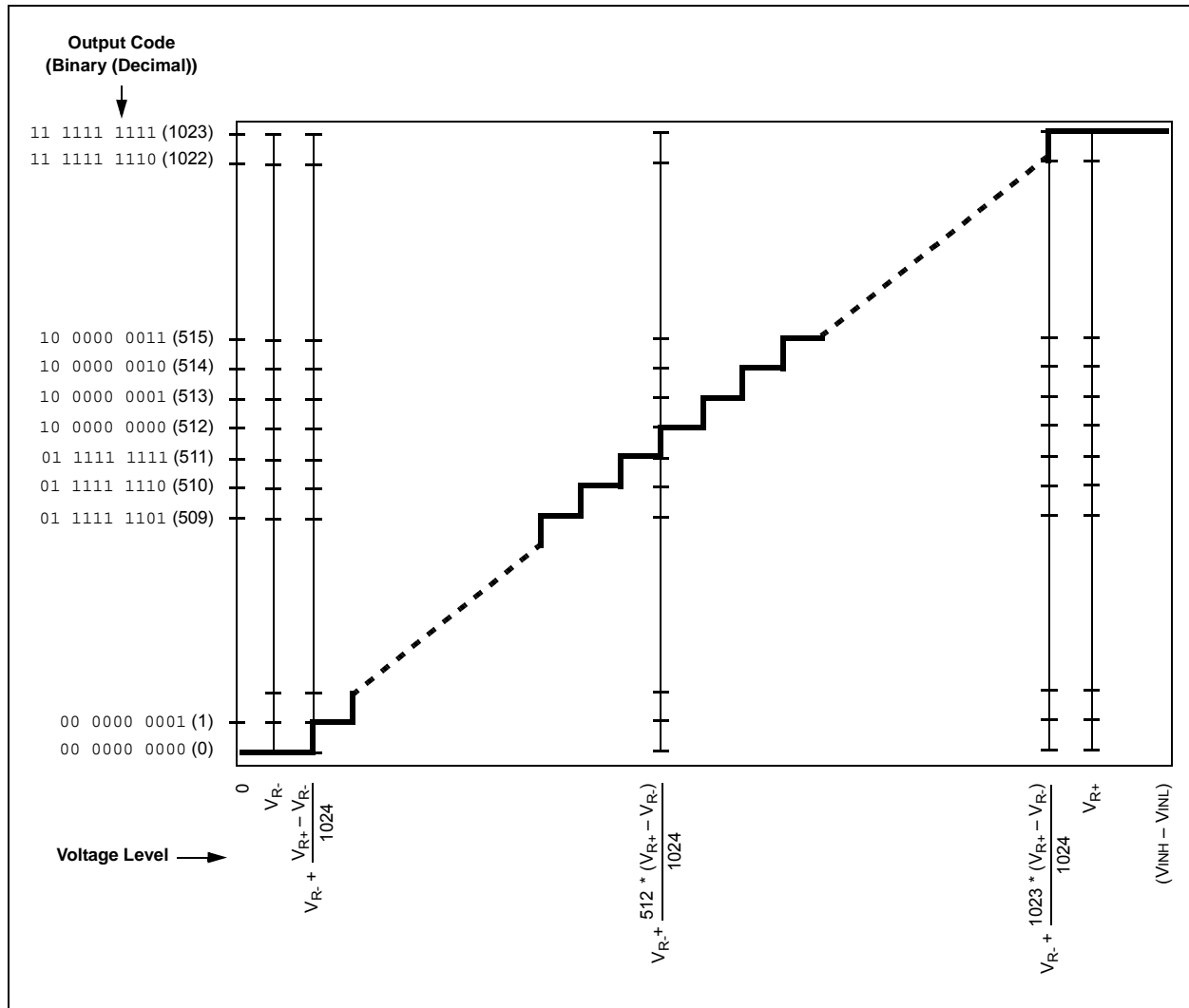


FIGURE 24-5: 10-BIT A/D TRANSFER FUNCTION



PIC24FJ256GA705 FAMILY

FIGURE 25-2: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 0

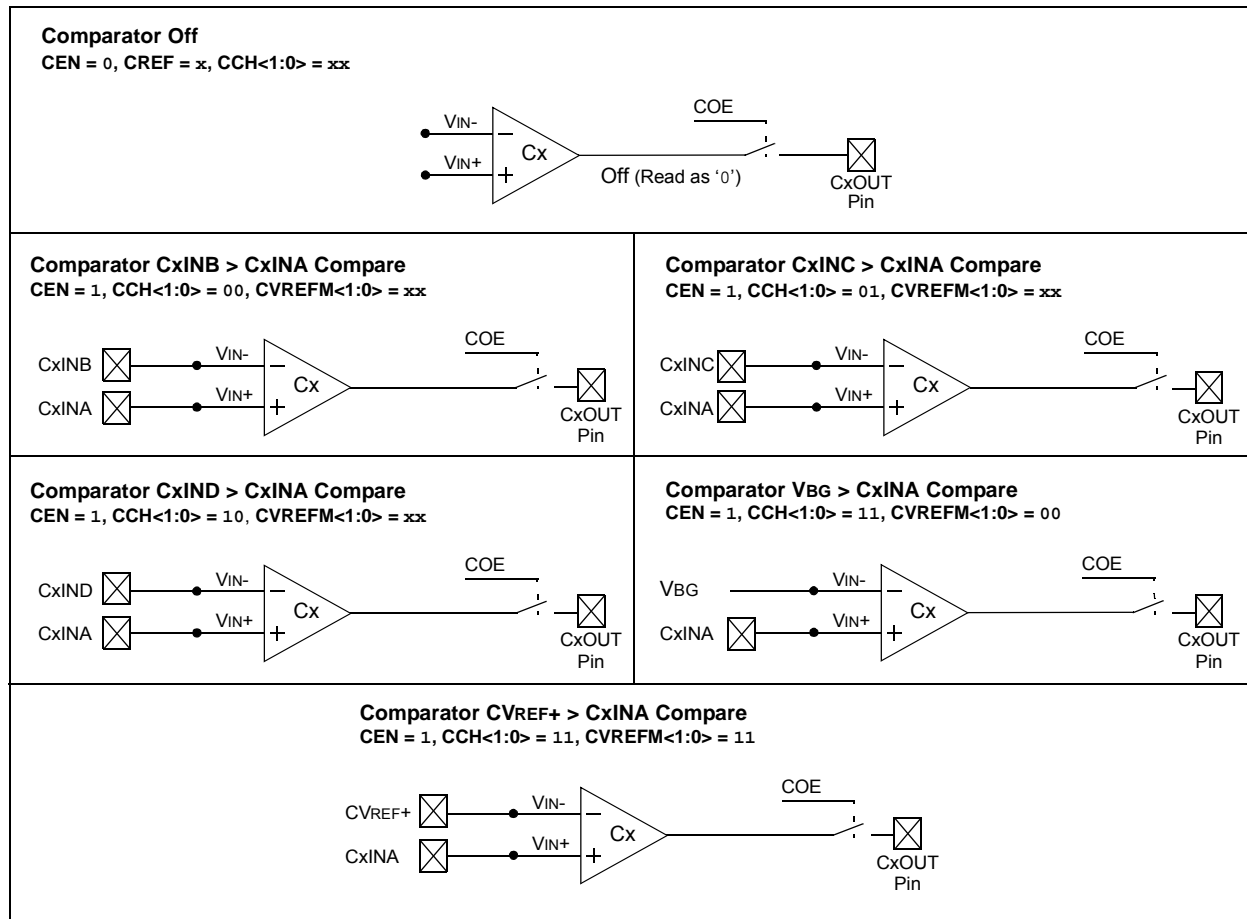
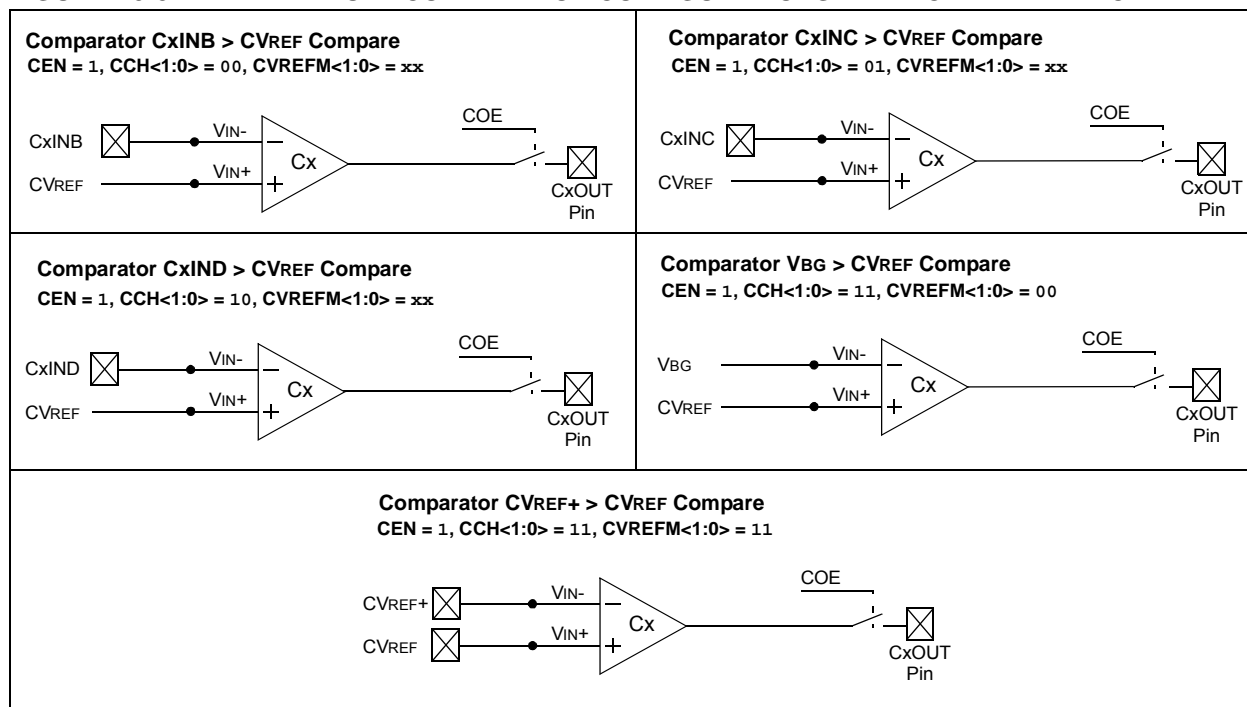


FIGURE 25-3: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 0



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REGISTER 27-1: CTMUCON1L: CTMU CONTROL REGISTER 1 LOW (CONTINUED)

bit 1-0 **IRNG<1:0>**: Current Source Range Select bits

If IRNGH = 0:

11 = 55 μ A range

10 = 5.5 μ A range

01 = 550 nA range

00 = 550 μ A range

If IRNGH = 1:

11 = Reserved

10 = Reserved

01 = 2.2 mA range

00 = 550 μ A range

REGISTER 27-3: CTMUCON2L: CTMU CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DSCHS2	DSCHS1	DSCHS0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **IRSTEN:** CTMU Current Source Reset Enable bit

1 = Signal selected by DSCHS<2:0> bits or IDISSEN control bit will reset CTMU edge detect logic

0 = CTMU edge detect logic will not occur

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DSCHS<2:0>:** Discharge Source Select Bits

111 = CLC2 out

110 = CLC1 out

101 = Disabled

100 = A/D end of conversion

011 = MCCP3 auxiliary output

010 = MCCP2 auxiliary output

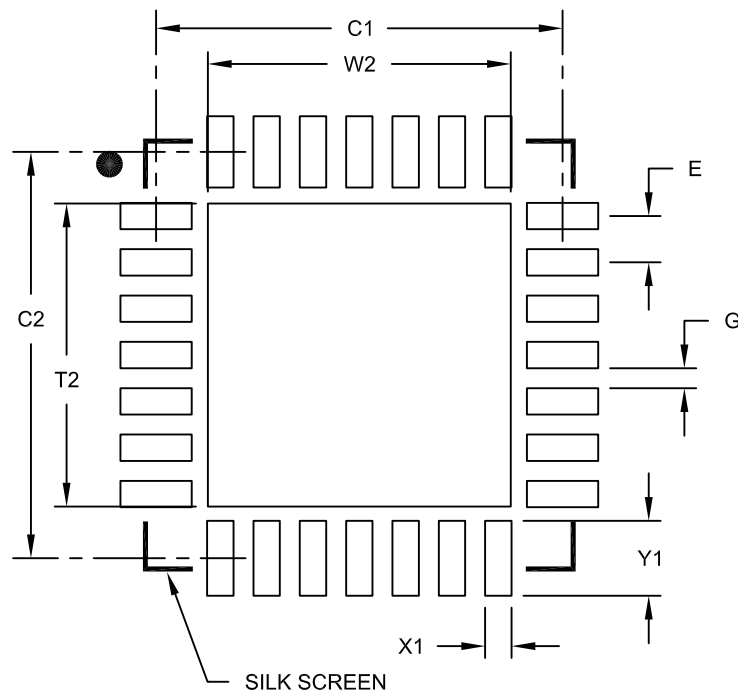
001 = MCCP1 auxiliary output

000 = Disabled

PIC24FJ256GA705 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

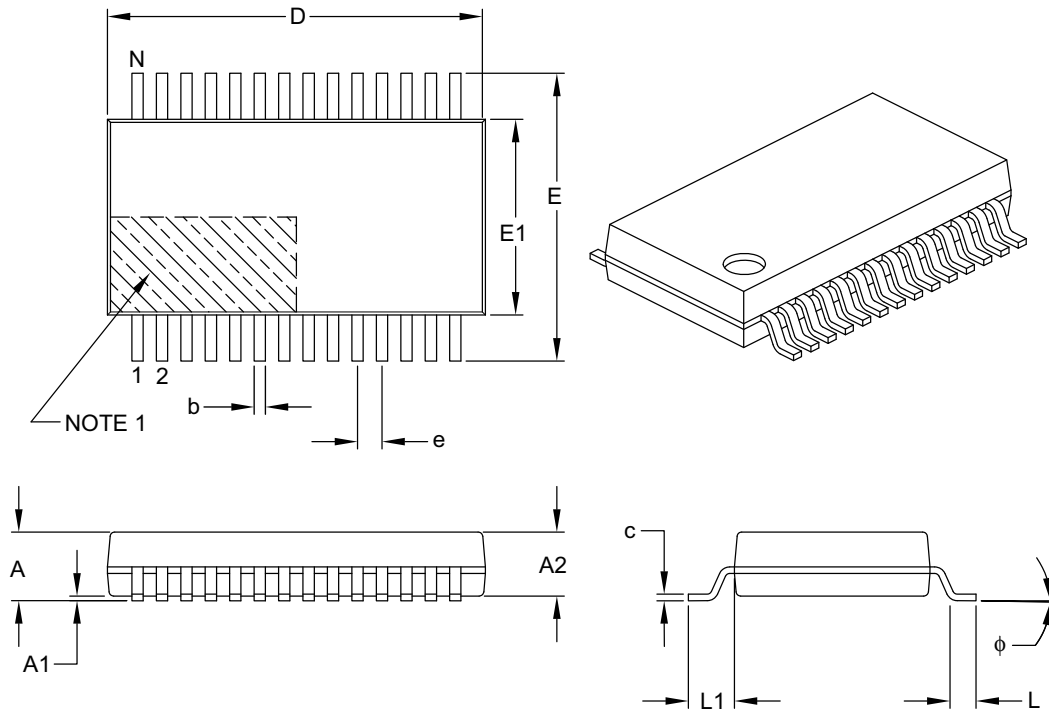
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC24FJ256GA705 FAMILY

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		0.65 BSC		
Overall Height	A		–	–	2.00
Molded Package Thickness	A2		1.65	1.75	1.85
Standoff	A1		0.05	–	–
Overall Width	E		7.40	7.80	8.20
Molded Package Width	E1		5.00	5.30	5.60
Overall Length	D		9.90	10.20	10.50
Foot Length	L		0.55	0.75	0.95
Footprint	L1		1.25 REF		
Lead Thickness	c		0.09	–	0.25
Foot Angle	φ		0°	4°	8°
Lead Width	b		0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC24FJ256GA705 FAMILY

NOTES: