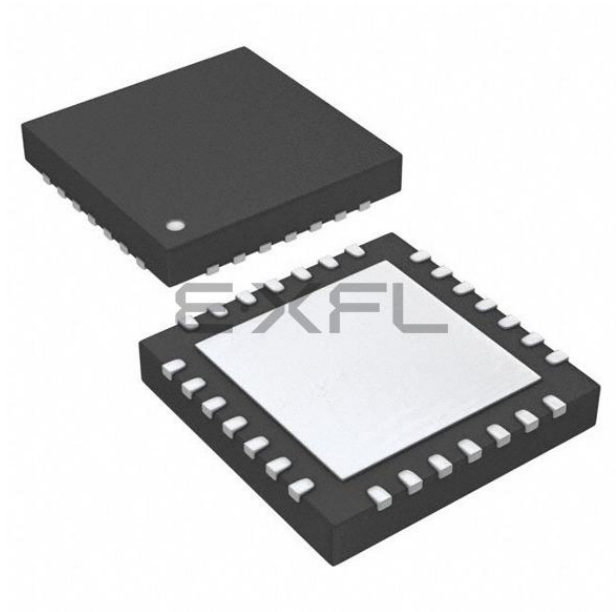

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga702-i-ml

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

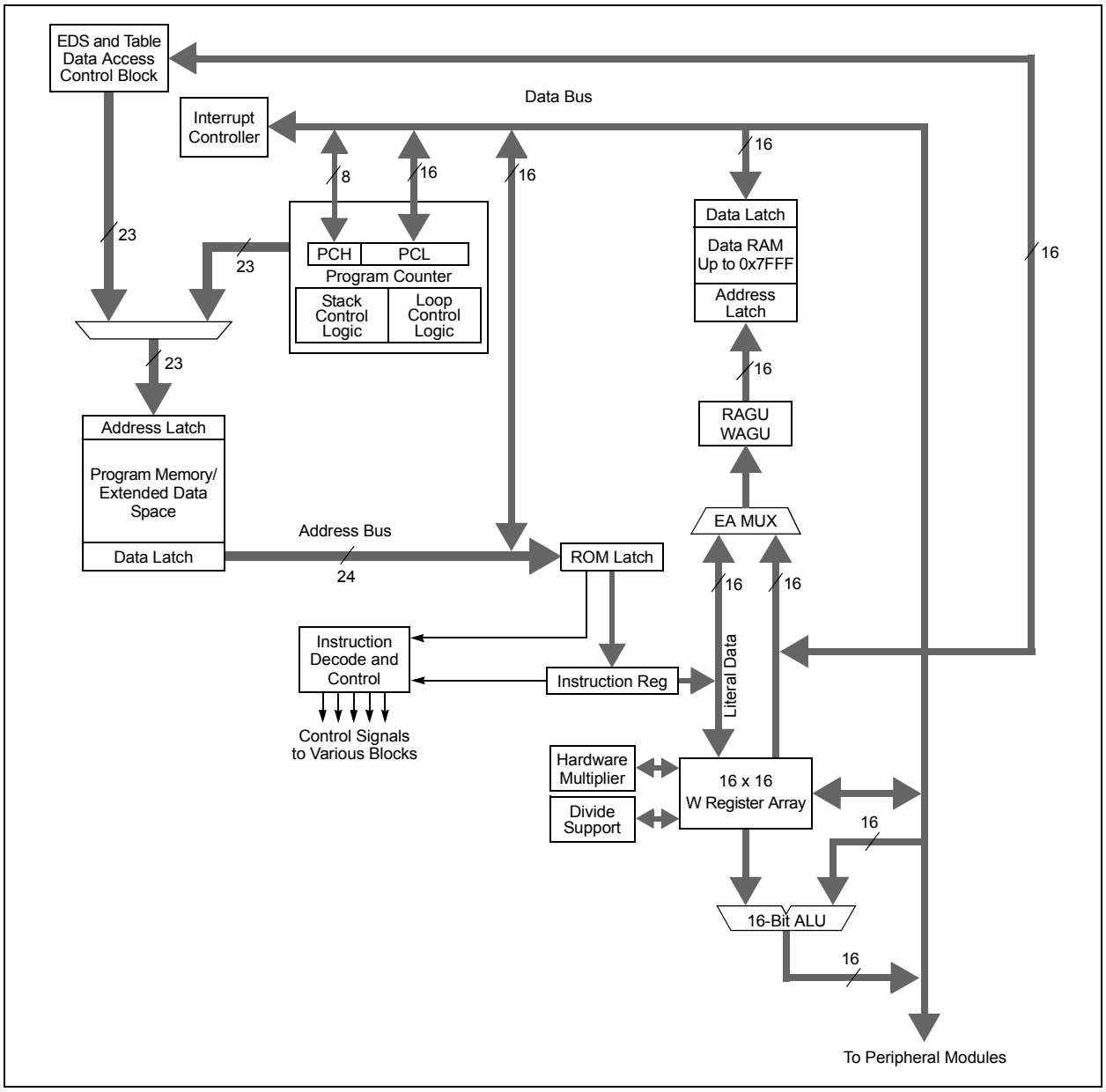


TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

4.2.5.1 Data Read from EDS

In order to read the data from the EDS space, first, an Address Pointer is set up by loading the required EDS page number into the DSRPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, the EDS window is enabled by setting bit 15 of the Working register which is assigned with the offset address; then, the contents of the pointed EDS location can be read.

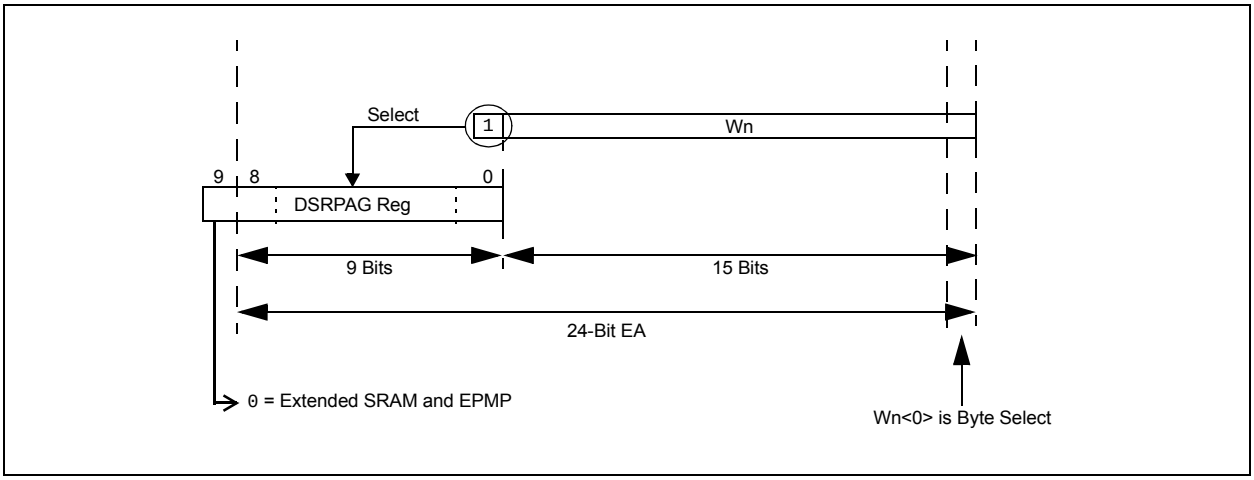
Figure 4-4 illustrates how the EDS space address is generated for read operations.

When the Most Significant bit (MSb) of EA is '1' and DSRPAG<9> = 0, the lower 9 bits of DSRPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS space address for read operations.

Example 4-1 shows how to read a byte, word and double word from EDS.

Note:	All read operations from EDS space have an overhead of one instruction cycle. Therefore, a minimum of two instruction cycles are required to complete an EDS read. EDS reads under the REPEAT instruction; the first two accesses take three cycles and the subsequent accesses take one cycle.

FIGURE 4-4: EDS ADDRESS GENERATION FOR READ OPERATIONS



EXAMPLE 4-1: EDS READ CODE IN ASSEMBLY

```
; Set the EDS page from where the data to be read
    mov     #0x0002, w0
    mov     w0, DSRPAG      ;page 2 is selected for read
    mov     #0x0800, w1     ;select the location (0x800) to be read
    bset    w1, #15         ;set the MSB of the base address, enable EDS mode

;Read a byte from the selected location
    mov.b   [w1++], w2      ;read Low byte
    mov.b   [w1++], w3      ;read High byte

;Read a word from the selected location
    mov     [w1], w2        ;

;Read Double - word from the selected location
    mov.d   [w1], w2        ;two word read, stored in w2 and w3
```

TABLE 8-2: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	IRQ #	IVT Address	Interrupt Bit Location		
			Flag	Enable	Priority
PMP – Parallel Master Port	45	00006Eh	IFS2<13>	IEC2<13>	PMPInterrupt
DMA4 – Direct Memory Access 4	46	000070h	IFS2<14>	IEC2<14>	DMA4Interrupt
—	47	—	—	—	—
—	48	—	—	—	—
SI2C2 – I2C2 Slave Events	49	000076h	IFS3<1>	IEC3<1>	SI2C2Interrupt
MI2C2 – I2C2 Master Events	50	000078h	IFS3<2>	IEC3<2>	MI2C2Interrupt
—	51	—	—	—	—
—	52	—	—	—	—
INT3 – External Interrupt 3	53	00007Eh	IFS3<5>	IEC3<5>	INT3Interrupt
INT4 – External Interrupt 4	54	000080h	IFS3<6>	IEC3<6>	INT4Interrupt
—	55	—	—	—	—
—	56	—	—	—	—
—	57	—	—	—	—
SPI1RX – SPI1 Receive Done	58	000088h	IFS3<10>	IEC3<10>	SPI1RXInterrupt
SPI2RX – SPI2 Receive Done	59	00008Ah	IFS3<11>	IEC3<11>	SPI2RXInterrupt
SPI3RX – SPI3 Receive Done	60	00008Ch	IFS3<12>	IEC3<12>	SPI3RXInterrupt
DMA5 – Direct Memory Access 5	61	00008Eh	IFS3<13>	IEC3<13>	DMA5Interrupt
RTCC – Real-Time Clock and Calendar	62	000090h	IFS3<14>	IEC3<14>	RTCCInterrupt
CCP1 – Capture/Compare 1	63	000092h	IFS3<15>	IEC3<15>	CCP1Interrupt
CCP2 – Capture/Compare 2	64	000094h	IFS4<0>	IEC4<0>	CCP2Interrupt
U1E – UART1 Error	65	000096h	IFS4<1>	IEC4<1>	U1EInterrupt
U2E – UART2 Error	66	000098h	IFS4<2>	IEC4<2>	U2EInterrupt
CRC – Cyclic Redundancy Check	67	00009Ah	IFS4<3>	IEC4<3>	CRCInterrupt
—	68	—	—	—	—
—	69	—	—	—	—
—	70	—	—	—	—
—	71	—	—	—	—
HLVD – High/Low-Voltage Detect	72	0000A4h	IFS4<8>	IEC4<8>	HLVDInterrupt
—	73	—	—	—	—
—	74	—	—	—	—
—	75	—	—	—	—
—	76	—	—	—	—
CTMU – Interrupt	77	0000AEh	IFS4<13>	IEC4<13>	CTMUInterrupt
—	78	—	—	—	—
—	79	—	—	—	—
—	80	—	—	—	—
—	81	—	—	—	—
—	82	—	—	—	—
—	83	—	—	—	—

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

U-0	R-x(2)	R-x(2)	R-x(2)	U-0	R/W-x(2)	R/W-x(2)	R/W-x(2)
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

R/W-0	R/W-0	R-0(4)	U-0	R/CO-0	R/W-0	R/W-0	R/W-0
CLKLOCK	IOLOCK(3)	LOCK	—	CF	POSCEN	SOSCEN	OSWEN
bit 7							bit 0

Legend:	CO = Clearable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits(2)
111 = Oscillator with Frequency Divider (OSCFDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Oscillator with Frequency Divider (OSCFDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
If FSCM is Enabled (FCKSM<1:0> = 00):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is Disabled (FCKSM<1:0> = 1x):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **IOLOCK:** I/O Lock Enable bit(3)
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit(4)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

Note 1: OSCCON is protected by a write lock to prevent inadvertent clock switches. See **Section 9.4 "Clock Switching Operation"** for more information.
2: Reset values for these bits are determined by the FNOSCx Configuration bits.
3: The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1', once the IOLOCK bit is set, it cannot be cleared.
4: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

REGISTER 11-8: IOCPx: INTERRUPT-ON-CHANGE POSITIVE EDGE x REGISTER(1,2,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
IOCPx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCPx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **IOCPx<15:0>:** Interrupt-on-Change Positive Edge x Enable bits
- 1 = Interrupt-on-Change is enabled on the IOCx pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
- 0 = Interrupt-on-Change is disabled on the IOCx pin for a positive going edge

Note 1: Setting both IOCPx and IOCNx will enable the IOCx pin for both edges, while clearing both registers will disable the functionality.
2: Changing the value of this register while the module is enabled (IOCON = 1) may cause a spurious IOC event. The corresponding interrupt must be ignored, cleared (using IOCFx) or masked (within the interrupt controller), or this module must be enabled (IOCON = 0) when changing this register.
3: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-9: IOCNx: INTERRUPT-ON-CHANGE NEGATIVE EDGE x REGISTER(1,2,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
IOCNx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCNx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **IOCNx<15:0>:** Interrupt-on-Change Negative Edge x Enable bits
- 1 = Interrupt-on-Change is enabled on the IOCx pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
- 0 = Interrupt-on-Change is disabled on the IOCx pin for a negative going edge

Note 1: Setting both IOCPx and IOCNx will enable the IOCx pin for both edges, while clearing both registers will disable the functionality.
2: Changing the value of this register while the module is enabled (IOCON = 1) may cause a spurious IOC event. The corresponding interrupt must be ignored, cleared (using IOCFx) or masked (within the interrupt controller), or this module must be enabled (IOCON = 0) when changing this register.
3: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-46: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP28R<5:0>:** RP28 Output Pin Mapping bits

Peripheral Output Number n is assigned to pin, RP28 (see Table 11-7 for peripheral function numbers).

REGISTER 13-1: TxCON: TIMER2 CONTROL REGISTER(1) (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers
In 32-bit mode, T3CON control bits do not affect 32-bit timer operation.

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(2)
1 = Timer source is selected by TECS<1:0>
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TxCK or TyCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

3: In 32-bit mode, the T3CON control bits do not affect 32-bit timer operation.

16.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal Trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 16-6 depicts a simplified block diagram of the Input Capture mode.

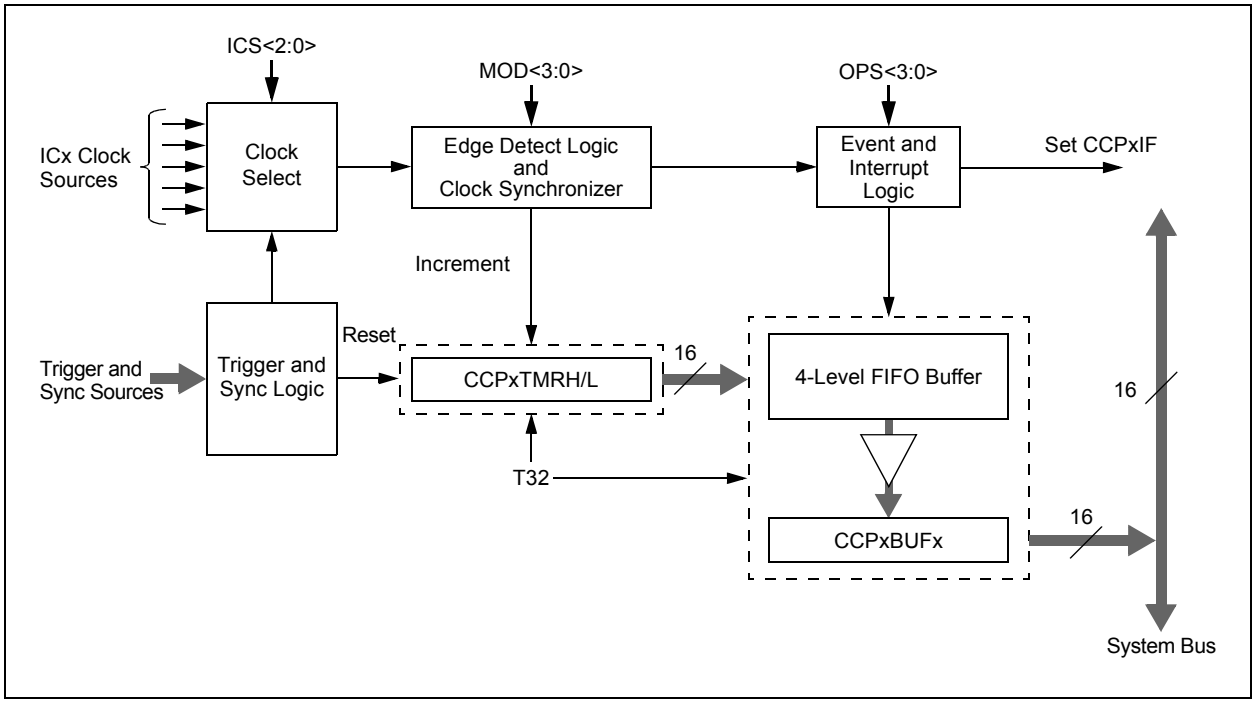
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L registers.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 16-3.

TABLE 16-3: INPUT CAPTURE MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 16-6: INPUT CAPTURE x BLOCK DIAGRAM



REGISTER 16-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **OCxEN:** Output Enable/Steering Control bits
1 = OCMx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCMx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output is defined by module operating mode (see Table 16-4)
01 = Time base rollover event (all modes)
00 = Disabled

bit 2-0 **ICS<2:0>:** Input Capture Source Select bits
111 = Reserved
110 = Reserved
101 = CLC2 output
100 = CLC1 output
011 = Comparator 3 output
010 = Comparator 2 output
001 = Comparator 1 output
000 = Input Capture x (ICMx) I/O pin

REGISTER 17-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.
2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

REGISTER 17-6: SPIxBUFL: SPIx BUFFER REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DATA<15:0>:** SPIx FIFO Data bits

When the MODE<32,16> or WLENGTH<4:0> bits select 16 to 9-bit data, the SPIx only uses DATA<15:0>. When the MODE<32,16> or WLENGTH<4:0> bits select 8 to 2-bit data, the SPIx only uses DATA<7:0>.

REGISTER 17-7: SPIxBUFH: SPIx BUFFER REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DATA<31:16>:** SPIx FIFO Data bits

When the MODE<32,16> or WLENGTH<4:0> bits select 32 to 25-bit data, the SPIx uses DATA<31:16>. When the MODE<32,16> or WLENGTH<4:0> bits select 24 to 17-bit data, the SPIx only uses DATA<23:16>.

REGISTER 18-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT(1)	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit(1)
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL<12>) will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCONL<12>) and SCLx is held low
0 = Data holding is disabled

Note 1: This bit must be set to '0' for 1 MHz operation.

20.0 ENHANCED PARALLEL MASTER PORT (EPMP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Enhanced Parallel Master Port (EPMP)"** (DS39730), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Enhanced Parallel Master Port (EPMP) module provides a parallel, 4-bit (Master mode only) or 8-bit (Master and Slave modes) data bus interface to communicate with off-chip modules, such as memories, FIFOs, LCD Controllers and other microcontrollers. This module can serve as either the master or the slave on the communication bus.

For EPMP Master modes, all external addresses are mapped into the internal Extended Data Space (EDS). This is done by allocating a region of the EDS for each Chip Select, and then assigning each Chip Select to a particular external resource, such as a memory or external controller. This region should not be assigned to another device resource, such as RAM or SFRs. To perform a write or read on an external resource, the CPU simply performs a write or read within the address range assigned for the EPMP.

Key features of the EPMP module are:

- Extended Data Space (EDS) Interface Allows Direct Access from the CPU
- Up to 10 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgment Lines (one per Chip Select)
- 4-Bit or 8-Bit Wide Data Bus
- Programmable Strobe Options (per Chip Select):
  - Individual read and write strobes or;
  - Read/$\overline{\text{Write}}$ strobe with enable strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per Chip Select)
- Programmable Polarity on Control Signals (per Chip Select)
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4-byte deep auto-incrementing buffer

Only the higher pin count packages in the family implement the EPMP. The EPMP feature is not available on 28-pin devices.

REGISTER 20-9: PADCON: PAD CONFIGURATION CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
IOCON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PMPTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IOCON:** Used for Non-PMP functionality

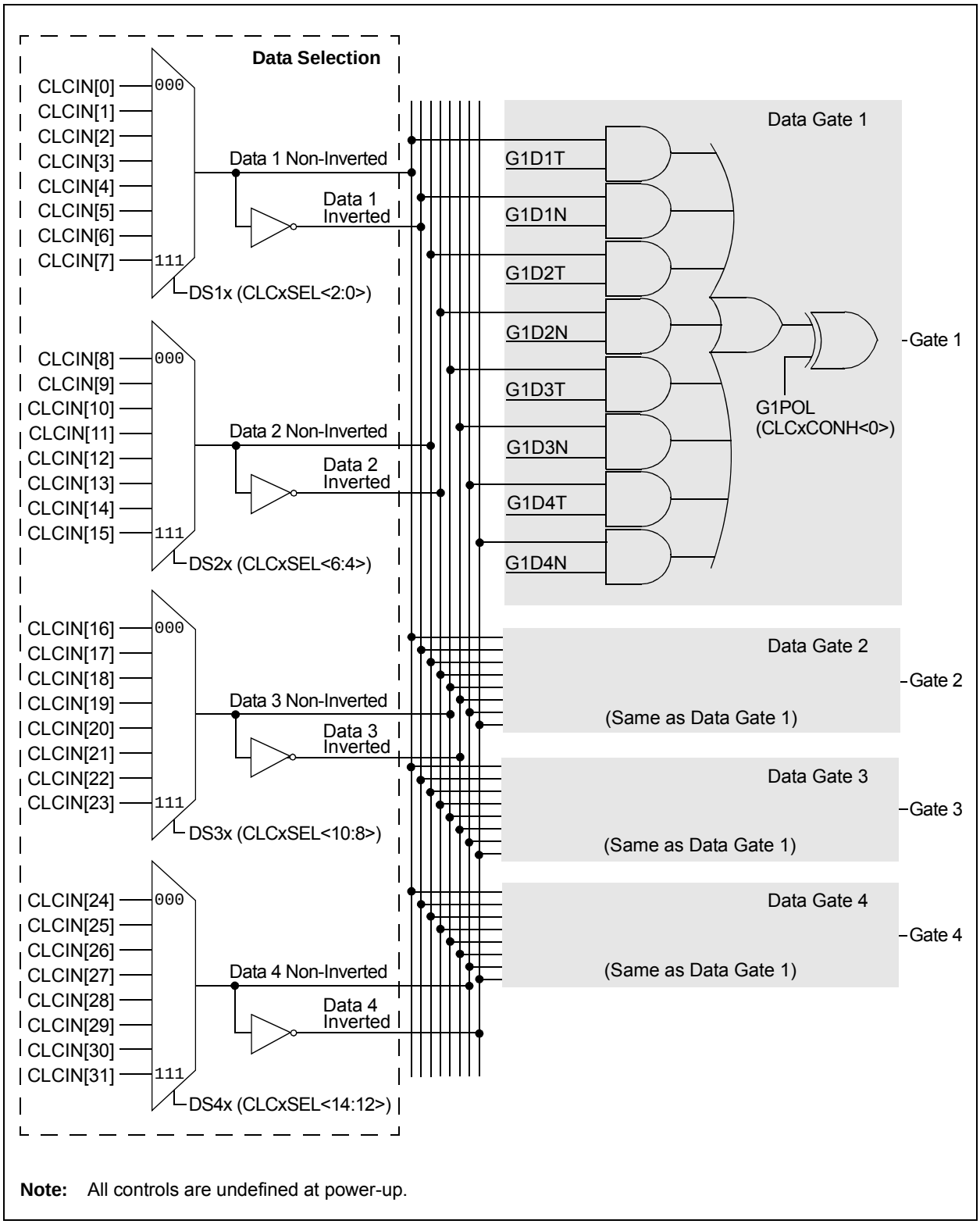
bit 14-1 **Unimplemented:** Read as '0'

bit 0 **PMPTTL:** EPMP Module TTL Input Buffer Select bit

1 = EPMP module inputs (PMDx, PMCS1) use TTL input buffers

0 = EPMP module inputs use Schmitt Trigger input buffers

FIGURE 23-3: CLCx INPUT SOURCE SELECTION DIAGRAM



Note: All controls are undefined at power-up.

REGISTER 23-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS4<2:0>			—	DS3<2:0>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS2<2:0>			—	DS1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits
111 = MCCP3 Compare Event Interrupt Flag (CCP3IF)
110 = MCCP1 Compare Event Interrupt Flag (CCP1IF)
101 = Unimplemented
100 = CTMU A/D trigger
011 = SPIx Input (SDIx) corresponding to the CLCx module (see Table 23-1)
010 = Comparator 3 output
001 = Module-specific CLCx output (see Table 23-1)
000 = CLCINB I/O pin

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits
111 = MCCP3 Compare Event Interrupt Flag (CCP3IF)
110 = MCCP2 Compare Event Interrupt Flag (CCP2IF)
101 = DMA Channel 1 interrupt
100 = UARTx RX output corresponding to the CLCx module (see Table 23-1)
011 = SPIx Output (SDOx) corresponding to the CLCx module (see Table 23-1)
010 = Comparator 2 output
001 = CLCx output (see Table 23-1)
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits
111 = MCCP2 Compare Event Interrupt Flag (CCP2IF)
110 = MCCP1 Compare Event Interrupt Flag (CCP1IF)
101 = DMA Channel 0 interrupt
100 = A/D conversion done interrupt
011 = UARTx TX input corresponding to the CLCx module (see Table 23-1)
010 = Comparator 1 output
001 = CLCx output (see Table 23-1)
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits
111 = Timer3 match event
110 = Timer2 match event
101 = Unimplemented
100 = REFO output
011 = INTRC/LPRC clock source
010 = SOSC clock source
001 = System clock (TCY)
000 = CLCINA I/O pin

TABLE 32-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

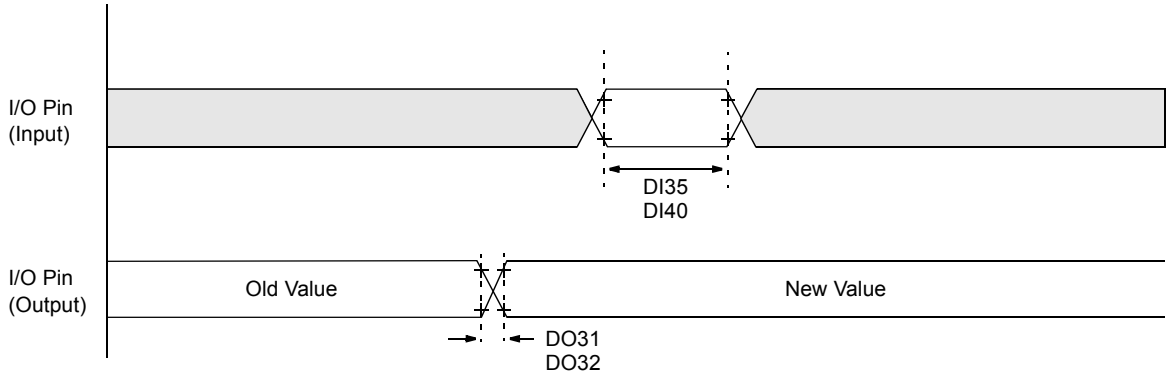
Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR	TVREG	Voltage Regulator Start-up Time	—	10	—	μs	VREGS = 0 with any POR or BOR
DVR10	VBG	Internal Band Gap Reference	1.14	1.2	1.26	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	1.6	1.8	2.0	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	10	—	—	μF	Series resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

TABLE 32-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0100(1)	3.45	—	3.73	V	
			HLVDL<3:0> = 0101	3.25	—	3.58	V	
			HLVDL<3:0> = 0110	2.95	—	3.25	V	
			HLVDL<3:0> = 0111	2.75	—	3.04	V	
			HLVDL<3:0> = 1000	2.65	—	2.92	V	
			HLVDL<3:0> = 1001	2.45	—	2.70	V	
			HLVDL<3:0> = 1010	2.35	—	2.60	V	
			HLVDL<3:0> = 1011	2.25	—	2.49	V	
			HLVDL<3:0> = 1100	2.15	—	2.39	V	
			HLVDL<3:0> = 1101	2.08	—	2.28	V	
			HLVDL<3:0> = 1110	2.00	—	2.15	V	
DC101	VTHL	HLVD Voltage on HLVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.20	—	V	
DC105	TONLVD	HLVD Module Enable Time		—	5	—	μS	From POR or HLVDEN = 1

Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0011', are not implemented.

FIGURE 32-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 32-2 for load conditions.

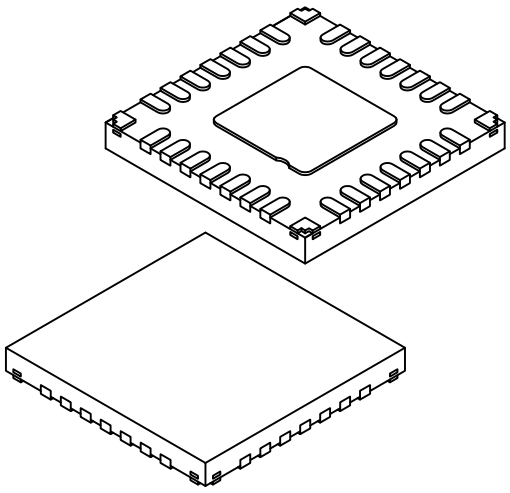
TABLE 32-22: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	TCY	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	TCY	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

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ISBN: 978-1-5224-1023-2