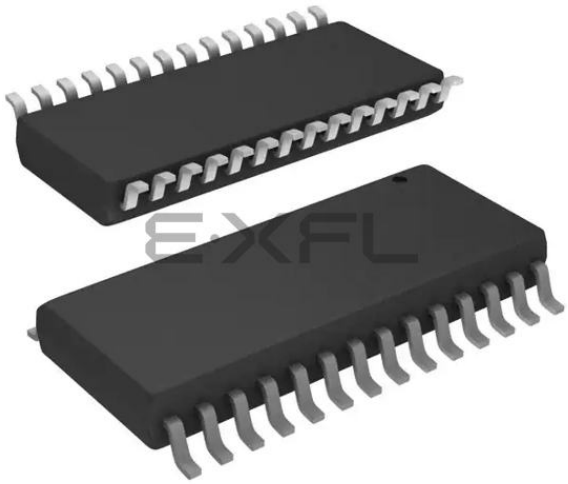

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Speed	32MHz
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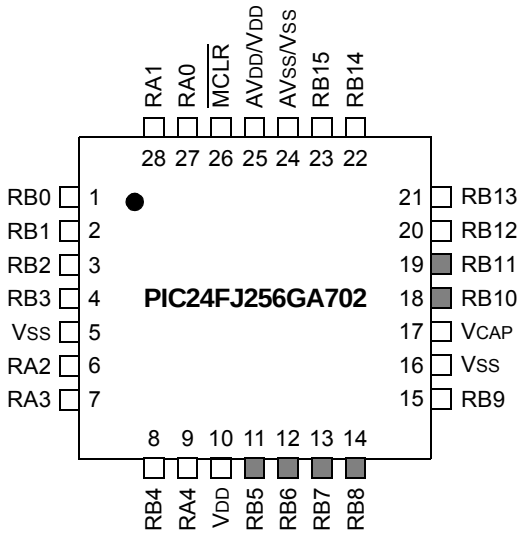
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga702-i-so

Pin Diagrams (PIC24FJ256GA702 Devices)

28-Pin QFN, UQFN



Legend: See Table 1 for a complete description of pin functions. Pinouts are subject to change.

Note: Gray shading indicates 5.5V tolerant input pins.

TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA702 QFN, UQFN)

Pin	Function	Pin	Function
1	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	15	TDO/C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/RB9
2	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	16	Vss
3	AN4/C1INB/**RP2**/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/**RP3**/SCL2/CTED8/RB3	18	PGD2/TDI/**RP10**/OCM1C/CTED11/RB10
5	Vss	19	PGC2/TMS/REFI1/**RP11**/CTED9/RB11
6	OSCI/CLKI/C1IND/RA2	20	AN8/LVDIN/**RP12**/RB12
7	OSCO/CLKO/C2IND/RA3	21	AN7/C1INC/**RP13**/OCM1D/CTPLS/RB13
8	SOSCI/**RP4**/RB4	22	CVREF/AN6/C3INB/**RP14**/CTED5/RB14
9	SOSCO/PWRLCLK/RA4	23	AN9/C3INA/**RP15**/CTED6/RB15
10	VDD	24	AVSS/VSS
11	PGD3/**RP5**/ASDA1/OCM1E/RB5	25	AVDD/VDD
12	PGC3/**RP6**/ASCL1/OCM1F/RB6	26	$\overline{\text{MCLR}}$
13	**RP7**/OCM1A/CTED3/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0
14	TCK/**RP8**/SCL1/OCM1B/CTED10/RB8	28	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1

Legend: **RPn** represents remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

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TABLE 4-4: SFR MAP: 0000h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
CPU CORE			**INTERRUPT CONTROLLER (CONTINUED)**		
WREG0	0000	0000	IEC1	009A	0000
WREG1	0002	0000	IEC2	009C	0000
WREG2	0004	0000	IEC3	009E	0000
WREG3	0006	0000	IEC4	00A0	0000
WREG4	0008	0000	IEC5	00A2	0000
WREG5	000A	0000	IEC6	00A4	0000
WREG6	000C	0000	IEC7	00A6	0000
WREG7	000E	0000	IPC0	00A8	4444
WREG8	0010	0000	IPC1	00AA	4444
WREG9	0012	0000	IPC2	00AC	4444
WREG10	0014	0000	IPC3	00AE	4444
WREG11	0016	0000	IPC4	00B0	4444
WREG12	0018	0000	IPC5	00B2	4404
WREG13	001A	0000	IPC6	00B4	4444
WREG14	001C	0000	IPC7	00B6	4444
WREG15	001E	0800	IPC8	00B8	0044
SPLIM	0020	xxxx	IPC9	00BA	4444
PCL	002E	0000	IPC10	00BC	4444
PCH	0030	0000	IPC11	00BE	4444
DSRPAG	0032	0000	IPC12	00C0	4444
DSWPAG	0034	0000	IPC13	00C2	0440
RCOUNT	0036	xxxx	IPC14	00C4	4400
SR	0042	0000	IPC15	00C6	4444
CORCON	0044	0004	IPC16	00C8	4444
DISICNT	0052	xxxx	IPC17	00CA	4444
TBLPAG	0054	0000	IPC18	00CC	0044
INTERRUPT CONTROLLER			IPC19	00CE	0040
INTCON1	0080	0000	IPC20	00D0	4440
INTCON2	0082	8000	IPC21	00D2	4444
INTCON4	0086	0000	IPC22	00D4	4444
IFS0	0088	0000	IPC23	00D6	4400
IFS1	008A	0000	IPC24	00D8	4444
IFS2	008C	0000	IPC25	00DA	0440
IFS3	008E	0000	IPC26	00DC	0400
IFS4	0090	0000	IPC27	00DE	4440
IFS5	0092	0000	IPC28	00E0	4444
IFS6	0094	0000	IPC29	00E2	0044
IFS7	0096	0000	INTTREG	00E4	0000
IEC0	0098	0000			

Legend: x = undefined. Reset values are shown in hexadecimal.

TABLE 8-2: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	IRQ #	IVT Address	Interrupt Bit Location		
			Flag	Enable	Priority
PMP – Parallel Master Port	45	00006Eh	IFS2<13>	IEC2<13>	PMPInterrupt
DMA4 – Direct Memory Access 4	46	000070h	IFS2<14>	IEC2<14>	DMA4Interrupt
—	47	—	—	—	—
—	48	—	—	—	—
SI2C2 – I2C2 Slave Events	49	000076h	IFS3<1>	IEC3<1>	SI2C2Interrupt
MI2C2 – I2C2 Master Events	50	000078h	IFS3<2>	IEC3<2>	MI2C2Interrupt
—	51	—	—	—	—
—	52	—	—	—	—
INT3 – External Interrupt 3	53	00007Eh	IFS3<5>	IEC3<5>	INT3Interrupt
INT4 – External Interrupt 4	54	000080h	IFS3<6>	IEC3<6>	INT4Interrupt
—	55	—	—	—	—
—	56	—	—	—	—
—	57	—	—	—	—
SPI1RX – SPI1 Receive Done	58	000088h	IFS3<10>	IEC3<10>	SPI1RXInterrupt
SPI2RX – SPI2 Receive Done	59	00008Ah	IFS3<11>	IEC3<11>	SPI2RXInterrupt
SPI3RX – SPI3 Receive Done	60	00008Ch	IFS3<12>	IEC3<12>	SPI3RXInterrupt
DMA5 – Direct Memory Access 5	61	00008Eh	IFS3<13>	IEC3<13>	DMA5Interrupt
RTCC – Real-Time Clock and Calendar	62	000090h	IFS3<14>	IEC3<14>	RTCCInterrupt
CCP1 – Capture/Compare 1	63	000092h	IFS3<15>	IEC3<15>	CCP1Interrupt
CCP2 – Capture/Compare 2	64	000094h	IFS4<0>	IEC4<0>	CCP2Interrupt
U1E – UART1 Error	65	000096h	IFS4<1>	IEC4<1>	U1EInterrupt
U2E – UART2 Error	66	000098h	IFS4<2>	IEC4<2>	U2EInterrupt
CRC – Cyclic Redundancy Check	67	00009Ah	IFS4<3>	IEC4<3>	CRCInterrupt
—	68	—	—	—	—
—	69	—	—	—	—
—	70	—	—	—	—
—	71	—	—	—	—
HLVD – High/Low-Voltage Detect	72	0000A4h	IFS4<8>	IEC4<8>	HLVDInterrupt
—	73	—	—	—	—
—	74	—	—	—	—
—	75	—	—	—	—
—	76	—	—	—	—
CTMU – Interrupt	77	0000AEh	IFS4<13>	IEC4<13>	CTMUInterrupt
—	78	—	—	—	—
—	79	—	—	—	—
—	80	—	—	—	—
—	81	—	—	—	—
—	82	—	—	—	—
—	83	—	—	—	—

REGISTER 11-19: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **IC2R<5:0>:** Assign Input Capture 2 (IC2) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IC1R<5:0>:** Assign Input Capture 1 (IC1) to Corresponding RPn or RPIn Pin bits

REGISTER 11-20: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IC3R<5:0>:** Assign Input Capture 3 (IC3) to Corresponding RPn or RPIn Pin bits

REGISTER 11-27: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK2R<5:0>:** Assign SPI2 Clock Input (SCK2IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI2R<5:0>:** Assign SPI2 Data Input (SDI2) to Corresponding RPn or RPIn Pin bits

REGISTER 11-28: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TXCKR5	TXCKR4	TXCKR3	TXCKR2	TXCKR1	TXCKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS2R5	SS2R4	SS2R3	SS2R2	SS2R1	SS2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TXCKR<5:0>:** Assign General Timer External Input (TxCK) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS2R<5:0>:** Assign SPI2 Slave Select Input (SS2IN) to Corresponding RPn or RPIn Pin bits

REGISTER 11-36: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP9R5	RP9R4	RP9R3	RP9R2	RP9R1	RP9R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP8R5	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP9R<5:0>:** RP9 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP9 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP8R<5:0>:** RP8 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP8 (see Table 11-7 for peripheral function numbers).

REGISTER 11-37: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP11R<5:0>:** RP11 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP11 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP10R<5:0>:** RP10 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP10 (see Table 11-7 for peripheral function numbers).

15.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 15-1 for PWM mode timing details. Table 15-1 and Table 15-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

EQUATION 15-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{CY}}{F_{PWM} \bullet (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

EXAMPLE 15-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS(1)

1. Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where FOSC = 32 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.

   TCY = 2 • TOSC = 62.5 ns

   PWM Period = 1/PWM Frequency = 1/52.08 kHz = 19.2 µS

   PWM Period = (PR2 + 1) • TCY • (Timer2 Prescale Value)

   19.2 µS = (PR2 + 1) • 62.5 ns • 1

   PR2 = 306

2. Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:

   PWM Resolution = $\log_{10}(F_{CY}/F_{PWM})/\log_{10}2)$ bits

   = $(\log_{10}(16\text{ MHz}/52.08\text{ kHz})/\log_{10}2)$ bits

   = 8.3 bits

Note 1: Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

TABLE 15-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (FCY = 4 MHz)(1)

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

TABLE 15-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (FCY = 16 MHz)(1)

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

REGISTER 16-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

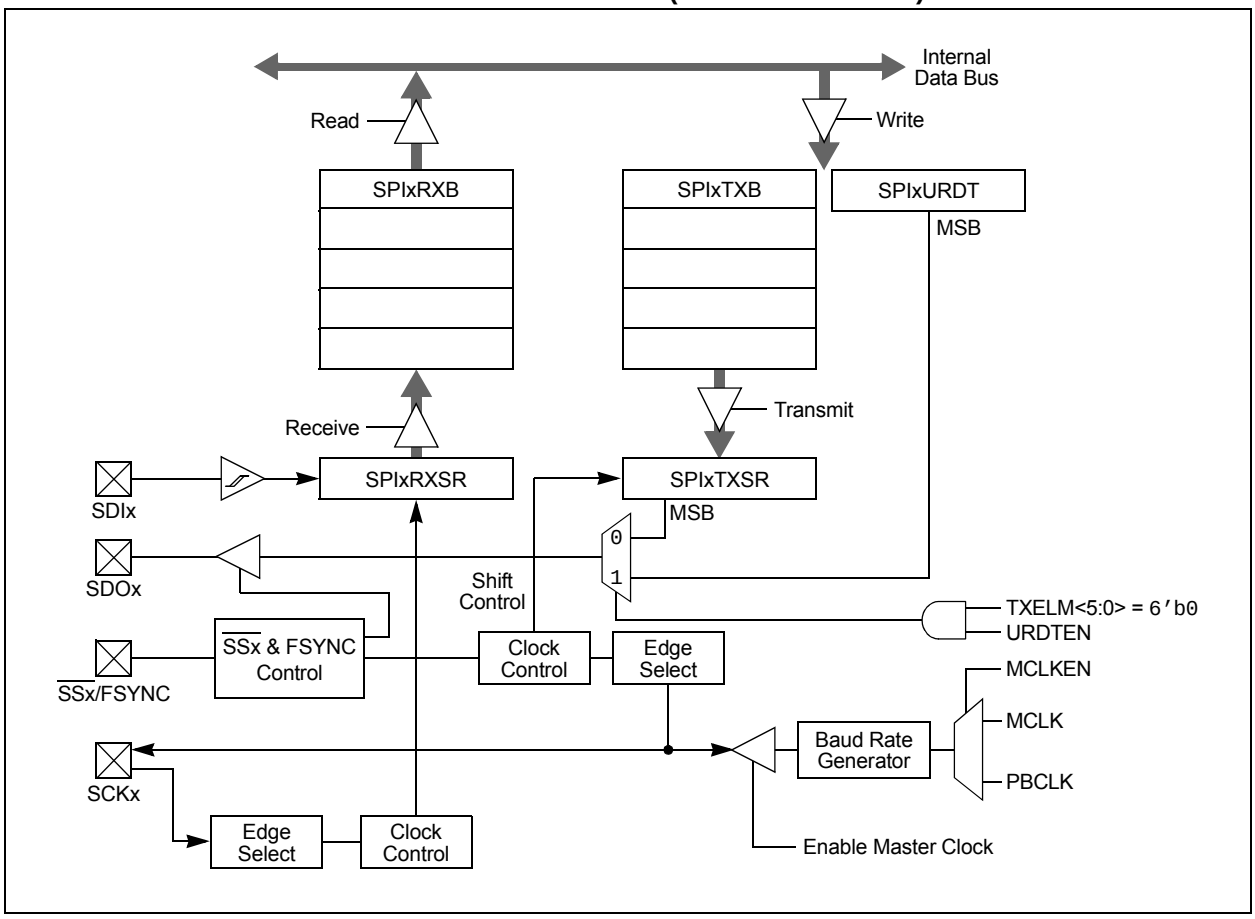
bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT<5:0>:** CCPx Dead-Time Select bits(1)

111111 = Inserts 63 dead-time delay periods between complementary output signals
111110 = Inserts 62 dead-time delay periods between complementary output signals
...
000010 = Inserts 2 dead-time delay periods between complementary output signals
000001 = Inserts 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in the MCCP1 module only.

FIGURE 17-1: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



17.3 Audio Mode Operation

To initialize the SPIx module for Audio mode, follow the steps to initialize it for Master/Slave mode, but also set the AUDEN bit (SPIxCON1H<15>). In Master+Audio mode:

- This mode enables the device to generate SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module generates LRC and SCKx continuously in all cases, regardless of the transmit data, while in Master mode.
- The SPIx module drives the leading edge of LRC and SCKx within 1 SCKx period, and the serial data shifts in and out continuously, even when the TX FIFO is empty.

In Slave+Audio mode:

- This mode enables the device to receive SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module drives zeros out of SDOx, but does not shift data out or in (SDIx) until the module receives the LRC (i.e., the edge that precedes the left channel).
- Once the module receives the leading edge of LRC, it starts receiving data if DISSDI (SPIxCON1L<4>) = 0 and the serial data shifts out continuously, even when the TX FIFO is empty.

REGISTER 17-11: SPIxURDTL: SPIx UNDERRUN DATA REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **URDATA<15:0>:** SPIx Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

When the MODE<32,16> or WLENGTH<4:0> bits select 16 to 9-bit data, the SPIx only uses URDATA<15:0>. When the MODE<32,16> or WLENGTH<4:0> bits select 8 to 2-bit data, the SPIx only uses URDATA<7:0>.

REGISTER 17-12: SPIxURDTH: SPIx UNDERRUN DATA REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **URDATA<31:16>:** SPIx Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

When the MODE<32,16> or WLENGTH<4:0> bits select 32 to 25-bit data, the SPIx only uses URDATA<31:16>. When the MODE<32,16> or WLENGTH<4:0> bits select 24 to 17-bit data, the SPIx only uses URDATA<23:16>.

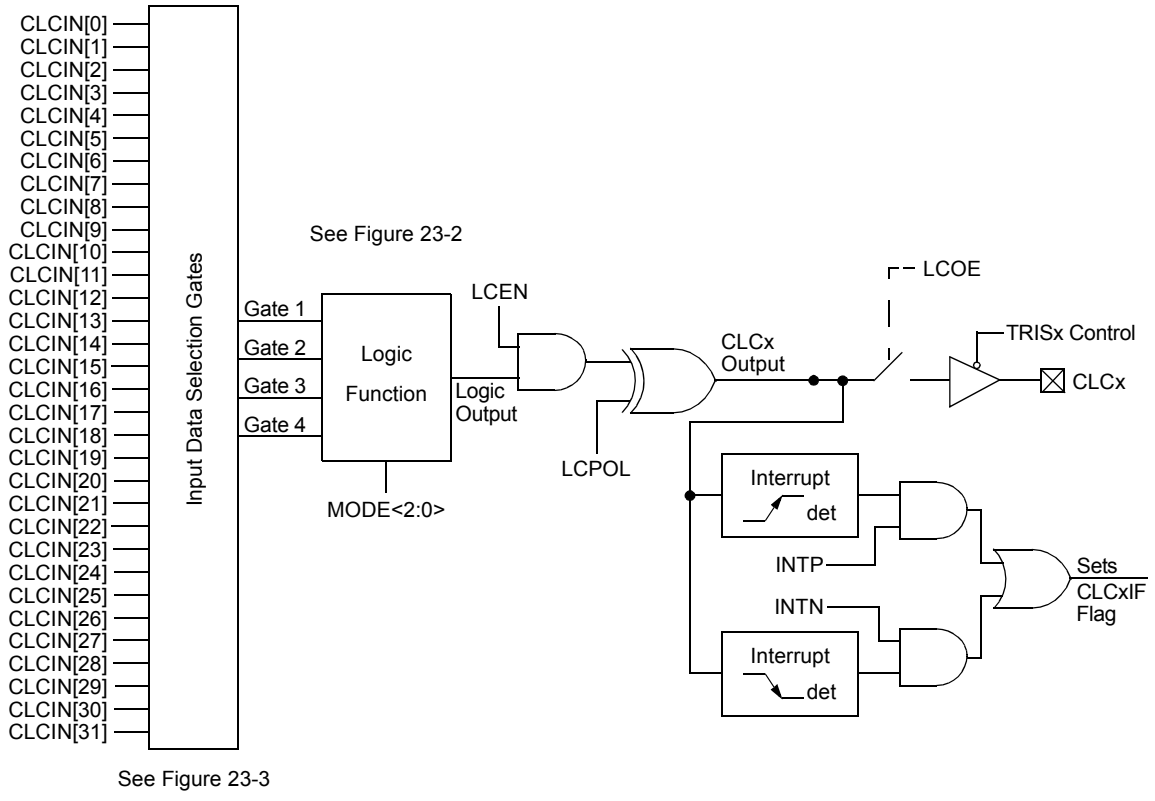
23.0 CONFIGURABLE LOGIC CELL (CLC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Configurable Logic Cell (CLC)"** (DS33949), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

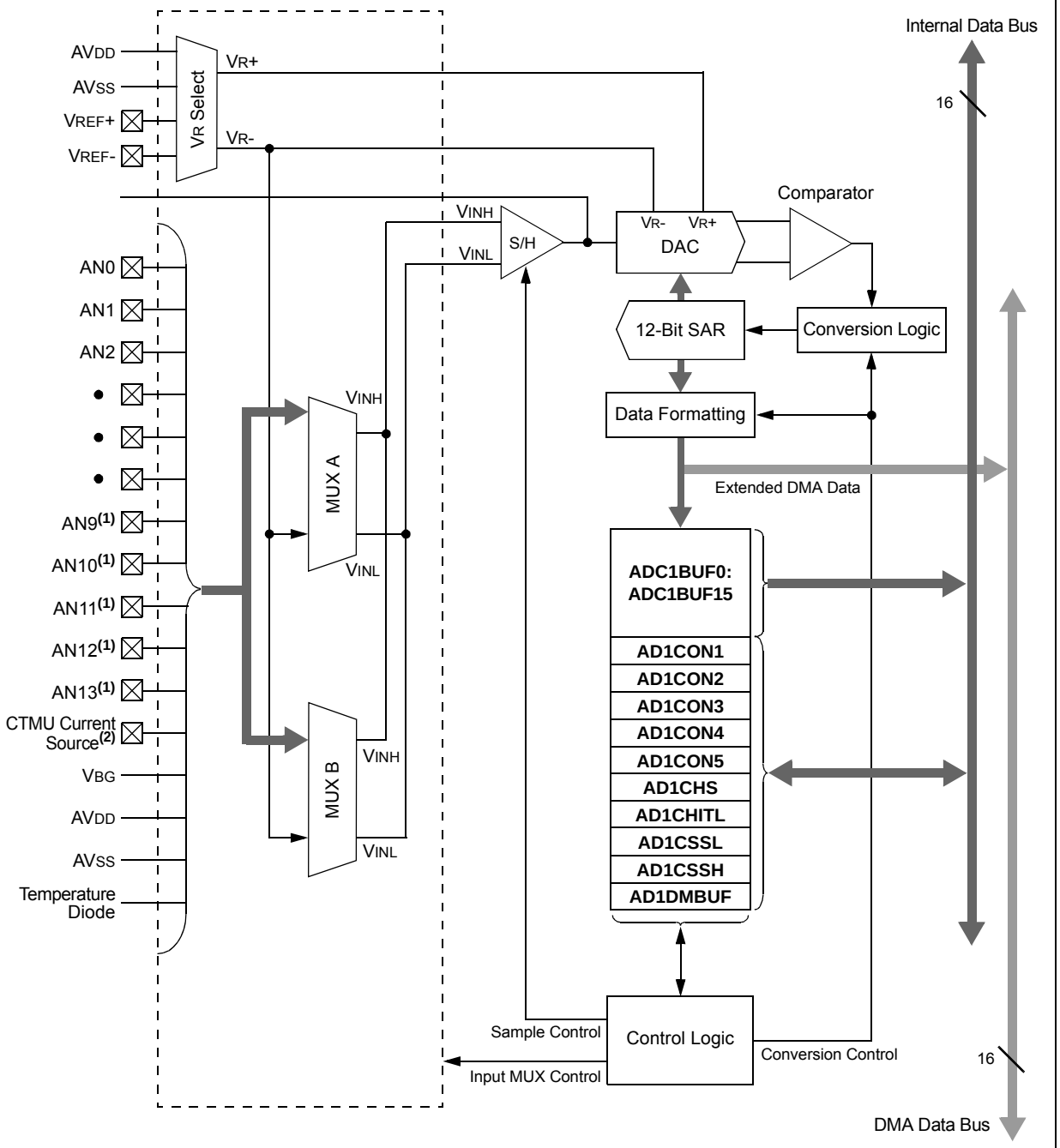
There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 23-1 shows an overview of the module. Figure 23-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 23-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCONL register.

FIGURE 24-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM (PIC24FJ256GA705 FAMILY)



Note 1: Available ANx pins are package-dependent.

2: CTMU current source is routed to the selected ANx pin when SAMP = 1 and TGEN = 0. See **Section 27.0 "Charge Time Measurement Unit (CTMU)"** for details.

REGISTER 24-2: AD1CON2: A/D CONTROL REGISTER 2 (CONTINUED)

bit 6-2 **SMPI<4:0>:** Interrupt Sample/DMA Increment Rate Select bits

When DMAEN = 1 and DMABM = 0:

11111 = Increments the DMA address after completion of the 32nd sample/conversion operation
11110 = Increments the DMA address after completion of the 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of the 2nd sample/conversion operation
00000 = Increments the DMA address after completion of each sample/conversion operation

When DMAEN = 1 and DMABM = 1:

11111 = Resets the DMA offset after completion of the 32nd sample/conversion operation
11110 = Resets the DMA offset after completion of the 31nd sample/conversion operation
•
•
•
00001 = Resets the DMA offset after completion of the 2nd sample/conversion operation
00000 = Resets the DMA offset after completion of every sample/conversion operation

When DMAEN = 0:

11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
•
•
•
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts buffer filling at ADC1BUF0 on first interrupt and ADC1BUF13 on next interrupt
0 = Always starts filling buffer at ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
0 = Always uses channel input selects for Sample A

NOTES:

REGISTER 27-1: CTMUCON1L: CTMU CONTROL REGISTER 1 LOW (CONTINUED)

bit 1-0 **IRNG<1:0>:** Current Source Range Select bits

If IRNGH = 0:
11 = 55 µA range
10 = 5.5 µA range
01 = 550 nA range
00 = 550 µA range

If IRNGH = 1:
11 = Reserved
10 = Reserved
01 = 2.2 mA range
00 = 550 µA range

REGISTER 27-2: CTMUCON1H: CTMU CONTROL REGISTER 1 HIGH (CONTINUED)

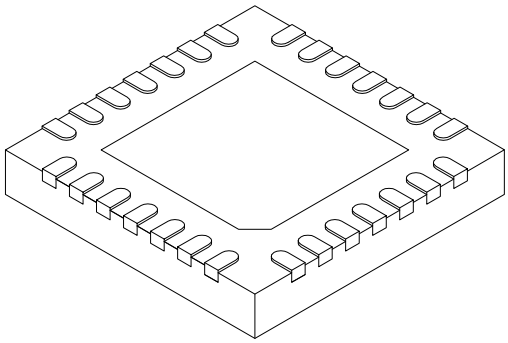
bit 5-2 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = CMP C3OUT
1110 = CMP C2OUT
1101 = CMP C1OUT
1100 = Peripheral clock
1011 = IC3 interrupt
1010 = IC2 interrupt
1001 = IC1 interrupt
1000 = CTED13 pin
0111 = CTED12 pin
0110 = CTED11 pin
0101 = CTED10 pin
0100 = CTED9 pin
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1
0000 = Timer1 match

bit 1 **Unimplemented:** Read as '0'

bit 0 **IRNGH:** High-Current Range Select bit
1 = Uses the higher current ranges (550 µA-2.2 mA)
0 = Uses the lower current ranges (550 nA-50 µA)
Current output is set by the IRNG<1:0> bits in the CTMUCON1L register.

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

Note the following details of the code protection feature on Microchip devices:

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