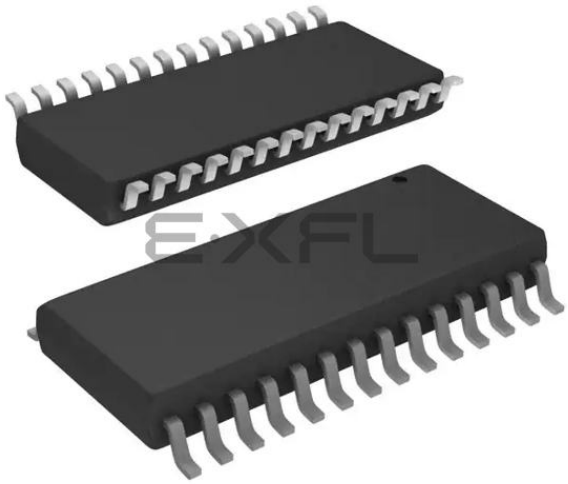
Microchip Technology - PIC24FJ256GA702T-I/SO Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga702t-i-so

TABLE 4-9: SFR MAP: 0500h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
DMA (CONTINUED)			**DMA (CONTINUED)**		
DMAINT5	0500	0000	DMADST5	0504	0000
DMASRC5	0502	0000	DMACNT5	0506	0001

Legend: x = undefined. Reset values are shown in hexadecimal.

TABLE 4-10: SFR MAP: 0600h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
I/O			**PORTB (CONTINUED)**		
PADCON	065E	0000	ANSB	067E	FFFF
IOCSTAT	0660	0000	IOCPB	0680	0000
PORTA			IOCNB	0682	0000
TRISA	0662	FFFF	IOCFB	0684	0000
PORTA	0664	0000	IOCPUB	0686	0000
LATA	0666	0000	IOCPDB	0688	0000
ODCA	0668	0000	**PORTC**		
ANSA	066A	FFFF	TRISC	068A	FFFF
IOCPA	066C	0000	PORTC	068C	0000
IOCNA	066E	0000	LATC	068E	0000
IOCFA	0670	0000	ODCC	0690	0000
IOCPUA	0672	0000	ANSC	0692	FFFF
IOCPDA	0674	0000	IOCPC	0694	0000
PORTB			IOCNC	0696	0000
TRISB	0676	FFFF	IOCFC	0698	0000
PORTB	0678	0000	IOCPUC	069A	0000
LATB	067A	0000	IOCPDC	069C	0000
ODCB	067C	0000			

Legend: x = undefined. Reset values are shown in hexadecimal.

4.2.5.2 Data Write into EDS

In order to write data to EDS, such as in EDS reads, an Address Pointer is set up by loading the required EDS page number into the DSWPAG register, and assigning the offset address to one of the W registers. Once the above assignment is done, then the EDS window is enabled by setting bit 15 of the Working register, assigned with the offset address, and the accessed location can be written.

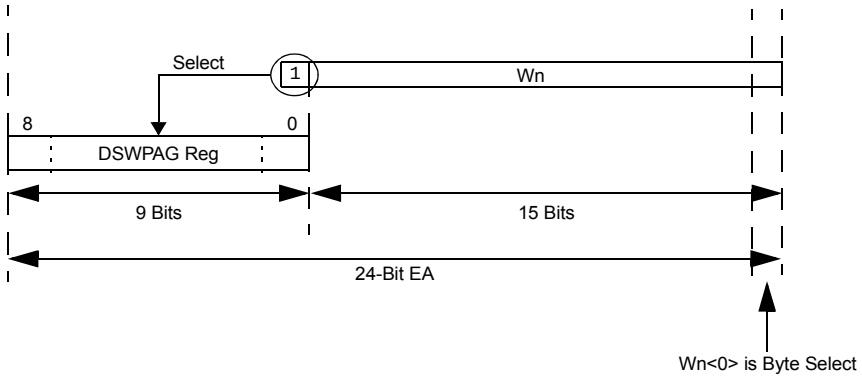
Figure 4-5 illustrates how the EDS address is generated for write operations.

When the MSbs of EA are '1', the lower 9 bits of DSWPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS address for write operations. Example 4-2 shows how to write a byte, word and double word to EDS.

The Data Space Page registers (DSRPAG/DSWPAG) do not update automatically while crossing a page boundary when the rollover happens from 0xFFFF to 0x8000. While developing code in assembly, care must be taken to update the Data Space Page registers when an Address Pointer crosses the page boundary. The 'C' compiler keeps track of the addressing, and increments or decrements the Page registers accordingly, while accessing contiguous data memory locations.

Note 1:	All write operations to EDS are executed in a single cycle.
2:	Use of Read/Modify/Write operation on any EDS location under a `REPEAT` instruction is not supported. For example: `BCLR`, `BSW`, `BTG`, `RLC f`, `RLNC f`, `RRC f`, `RRNC f`, `ADD f`, `SUB f`, `SUBR f`, `AND f`, `IOR f`, `XOR f`, `ASR f`, `ASL f`.
3:	Use the DSRPAG register while performing Read/Modify/Write operations.

FIGURE 4-5: EDS ADDRESS GENERATION FOR WRITE OPERATIONS



EXAMPLE 4-2: EDS WRITE CODE IN ASSEMBLY

```
; Set the EDS page where the data to be written
    mov     #0x0002, w0
    mov     w0, DSWPAG      ;page 2 is selected for write
    mov     #0x0800, w1     ;select the location (0x800) to be written
    bset    w1, #15         ;set the MSB of the base address, enable EDS mode

;Write a byte to the selected location
    mov     #0x00A5, w2
    mov     #0x003C, w3
    mov.b   w2, [w1++]      ;write Low byte
    mov.b   w3, [w1++]      ;write High byte

;Write a word to the selected location
    mov     #0x1234, w2     ;
    mov     w2, [w1]        ;

;Write a Double - word to the selected location
    mov     #0x1122, w2
    mov     #0x4455, w3
    mov.d   w2, [w1]        ;2 EDS writes
```

REGISTER 6-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/S-0, HC(1)	R/W-0(1)	R-0, HSC(1)	R/W-0	r-0	r-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	NVMOP3(2)	NVMOP2(2)	NVMOP1(2)	NVMOP0(2)
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	r = Reserved bit
R = Readable bit	W = Writable bit	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR	'1' = Bit is set	U = Unimplemented bit, read as '0'	
HSC = Hardware Settable/Clearable bit			

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle bit
- 1 = Removes power from the program memory when device enters Idle mode
- 0 = Powers program memory in Standby mode when the device enters Idle mode

bit 11-10 **Reserved:** Maintain as '0'

bit 9-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(1,2)
- 1110 = Chip erases user memory (does not erase Device ID, customer OTP or executive memory)
- 0100 = Unused
- 0011 = Erases a page of program or executive memory
- 0010 = Row programming operation
- 0001 = Double-word programming operation

Note 1: These bits can only be reset on a Power-on Reset.

2: All other combinations of NVMOP<3:0> are unimplemented.

EXAMPLE 6-2: INITIATING A PROGRAMMING SEQUENCE

```
        DISI    #5                      ; Block all interrupts with priority <7
                                        ; for next 5 instructions
        MOV.B   #0x55, W0
        MOV     W0, NVMKEY              ; Write the 0x55 key
        MOV.B   #0xAA, W1               ;
        MOV     W1, NVMKEY              ; Write the 0xAA key
        BSET    NVMCON, #WR             ; Start the programming sequence
        NOP                             ; Required delays
        NOP
        BTSC    NVMCON, #15             ; and wait for it to be
        BRA     $-2                     ; completed
```

REGISTER 7-1: RCON: RESET CONTROL REGISTER (CONTINUED)

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(4)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit(1)
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake from Sleep Flag bit(1)
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit(1)
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = A Brown-out Reset has occurred (also set after a Power-on Reset)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the $\overline{\text{LPCFG}}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect. Retention mode preserves the SRAM contents during Sleep.

3: Re-enabling the regulator after it enters Standby mode will add a delay, TVREG, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

4: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled**,** regardless of the SWDTEN bit setting.

5: The BOREN<1:0> (FPOR<1:0>) Configuration bits must be set to '01' in order for SBOREN to have an effect.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	CLRWDT, PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #0 Instruction	POR
IDLE (RCON<2>)	PWRSAV #1 Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

REGISTER 8-1: SR: ALU STATUS REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> Status bits are concatenated with the IPL3 Status bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1. User interrupts are disabled when IPL3 = 1.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 9-8: REFOTRIML: REFERENCE OSCILLATOR TRIM REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<0:7>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ROTRIM8	—	—	—	—	—	—	—
bit 7							bit 0

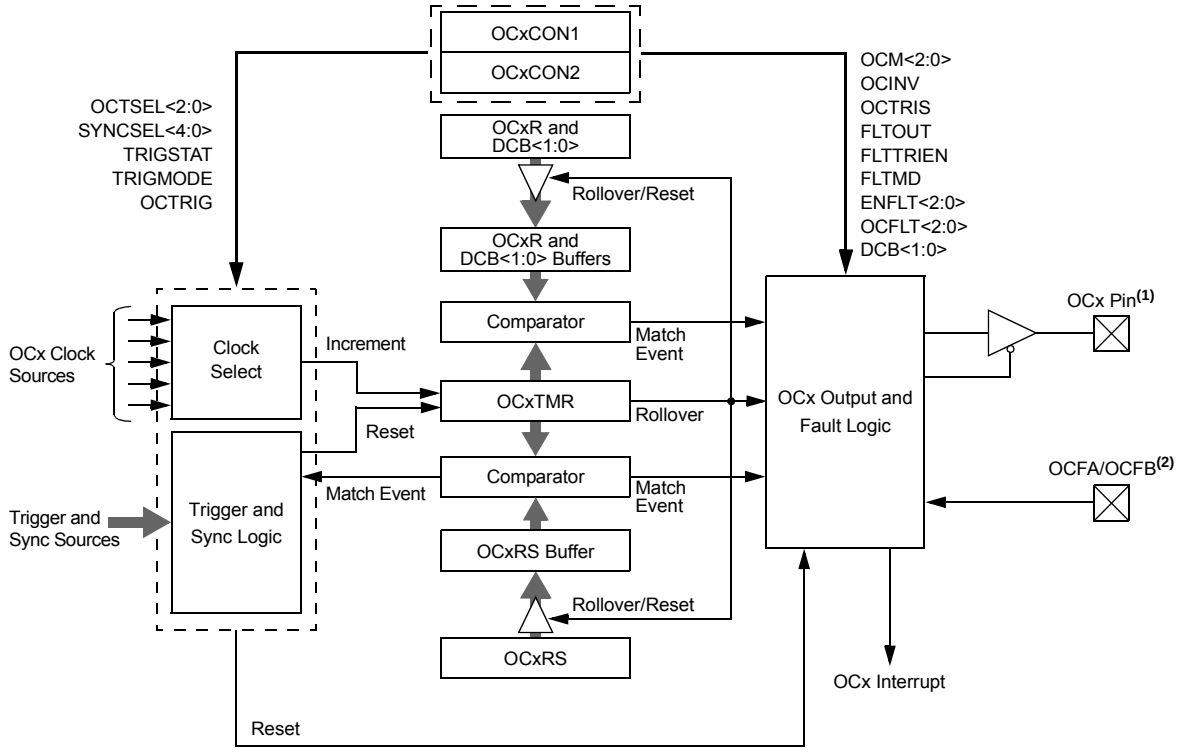
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **ROTRIM<0:8>:** REFO Trim bits

These bits provide a fractional additive to the RODIVx value for the 1/2 period of the REFO clock.
000000000 = 0/512 (0.0 divisor added to the RODIVx value)
000000001 = 1/512 (0.001953125 divisor added to the RODIVx value)
000000010 = 2/512 (0.00390625 divisor added to the RODIVx value)
•
•
•
100000000 = 256/512 (0.5000 divisor added to the RODIVx value)
•
•
•
111111110 = 510/512 (0.99609375 divisor added to the RODIVx value)
111111111 = 511/512 (0.998046875 divisor added to the RODIVx value)

bit 6-0 **Unimplemented:** Read as ‘0’

FIGURE 15-2: OUTPUT COMPARE x BLOCK DIAGRAM (DOUBLE-BUFFERED, 16-BIT PWM MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

15.3.1 PWM PERIOD

The PWM period is specified by writing to PRy, the Timer Period register. The PWM period can be calculated using Equation 15-1.

EQUATION 15-1: CALCULATING THE PWM PERIOD(1)

$$\text{PWM Period} = [(\text{PRy}) + 1 \cdot T_{CY} \cdot (\text{Timer Prescale Value})$$

Where:

$$\text{PWM Frequency} = 1/[\text{PWM Period}]$$

Note 1: Based on $T_{CY} = T_{OSC} * 2$; Doze mode and PLL are disabled.

Note: A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7, written into the PRy register, will yield a period consisting of 8 time base cycles.

REGISTER 17-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW (CONTINUED)

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Transmit happens on transition from active clock state to Idle clock state
0 = Transmit happens on transition from Idle clock state to active clock state

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used by the macro in Slave mode; $\overline{SSx}$ pin is used as the slave select input
0 = $\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

bit 6 **CKP:** SPIx Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx Input Port bit
1 = SDIx pin is not used by the module; pin is controlled by the port function
0 = SDIx pin is controlled by the module

bit 3 **DISSCK:** Disable SCKx Output Port bit
1 = SCKx pin is not used by the module; pin is controlled by the port function
0 = SCKx pin is controlled by the module

bit 2 **MCLKEN:** Master Clock Enable bit(3)
1 = MCLK is used by the BRG
0 = PBCLK is used by the BRG

bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0 = Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

bit 0 **ENHBUF:** Enhanced Buffer Mode Enable bit
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When AUDEN = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows the FRMSYPW bit.

REGISTER 17-4: SPIxSTATL: SPIx STATUS REGISTER LOW

U-0	U-0	U-0	R/C-0, HS	R-0, HSC	U-0	U-0	R-0, HSC
—	—	—	FRMERR	SPIBUSY	—	—	SPITUR(1)
bit 15							bit 8

R-0, HSC	R/C-0, HS	R-1, HSC	U-0	R-1, HSC	U-0	R-0, HSC	R-0, HSC
SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	x = Bit is unknown
R = Readable bit	W = Writable bit	'0' = Bit is cleared	HSC = Hardware Settable/Clearable bit
-n = Value at POR	'1' = Bit is set	U = Unimplemented bit, read as '0'	

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR**: SPIx Frame Error Status bit
1 = Frame error is detected
0 = No frame error is detected

bit 11 **SPIBUSY:** SPIx Activity Status bit
1 = Module is currently busy with some transactions
0 = No ongoing transactions (at time of read)

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** SPIx Transmit Underrun Status bit(1)
1 = Transmit buffer has encountered a Transmit Underrun condition
0 = Transmit buffer does not have a Transmit Underrun condition

bit 7 **SRMT:** Shift Register Empty Status bit
1 = No current or pending transactions (i.e., neither SPIxTXB or SPIxTXSR contains data to transmit)
0 = Current or pending transactions

bit 6 **SPIROV:** SPIx Receive Overflow Status bit
1 = A new byte/half-word/word has been completely received when the SPIxRXB is full
0 = No overflow

bit 5 **SPIRBE:** SPIx RX Buffer Empty Status bit
1 = RX buffer is empty
0 = RX buffer is not empty
Standard Buffer Mode:
Automatically set in hardware when SPIxBUF is read from, reading SPIxRXB. Automatically cleared in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB.
Enhanced Buffer Mode:
Indicates RXELM<5:0> = 6'b000000.

bit 4 **Unimplemented:** Read as '0'

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = SPIxTXB is empty
0 = SPIxTXB is not empty
Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Automatically cleared in hardware when SPIxBUF is written, loading SPIxTXB.
Enhanced Buffer Mode:
Indicates TXELM<5:0> = 6'b000000.

Note 1: SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

FIGURE 17-5: SPIx MASTER, FRAME SLAVE CONNECTION DIAGRAM

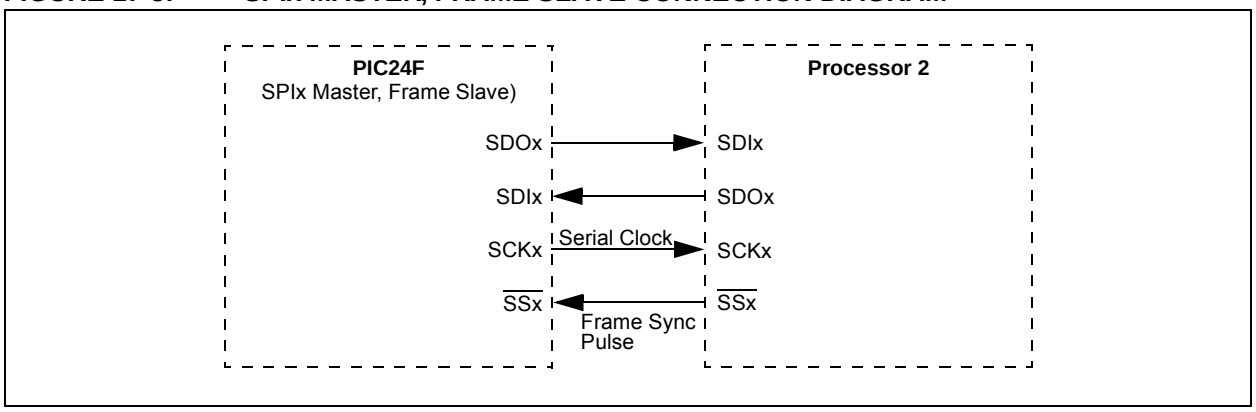


FIGURE 17-6: SPIx SLAVE, FRAME MASTER CONNECTION DIAGRAM

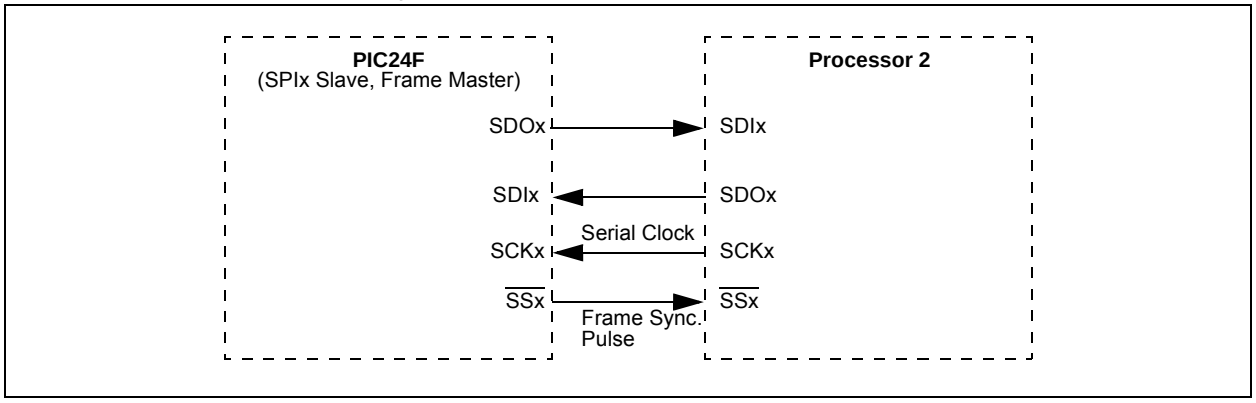
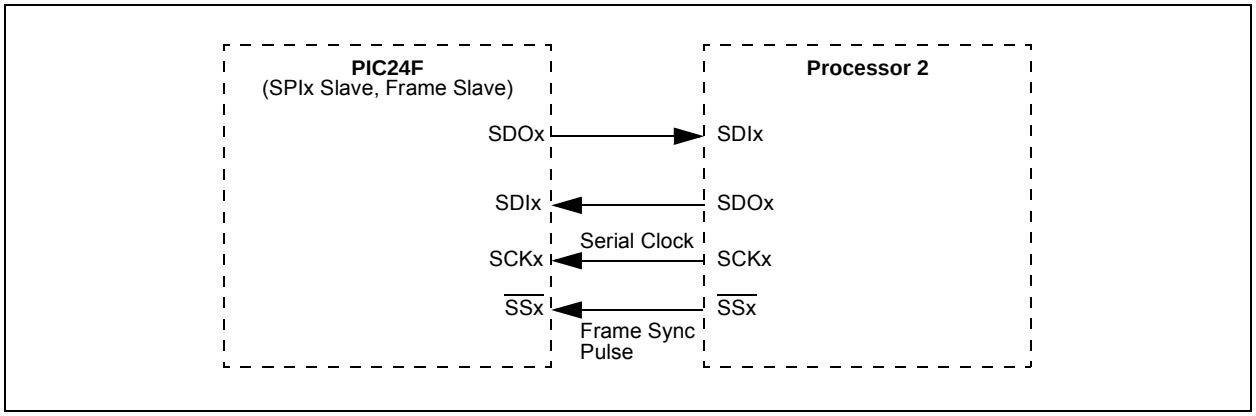


FIGURE 17-7: SPIx SLAVE, FRAME SLAVE CONNECTION DIAGRAM



EQUATION 17-1: RELATIONSHIP BETWEEN DEVICE AND SPIx CLOCK SPEED

$$\text{Baud Rate} = \frac{F_{PB}}{(2 * (SPIxBRG + 1))}$$

Where:

F_{PB} is the Peripheral Bus Clock Frequency.

REGISTER 20-6: PMCSxBS: EPMP CHIP SELECT x BASE ADDRESS REGISTER(2)

R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
BASE<23:16>							
bit 15							bit 8

R/W(1)	U-0	U-0	U-0	R/W(1)	U-0	U-0	U-0
BASE15	—	—	—	BASE11	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **BASE<23:15>:** Chip Select x Base Address bits(1)

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BASE11:** Chip Select x Base Address bit(1)

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The value at POR is 0080h for PMCS1BS and 8080h for PMCS2BS.

2: If the whole PMCS2BS register is written together as 0x0000, then the last EDS address for the Chip Select 1 will be FFFFFFh. In this case, Chip Select 2 should not be used. PMCS1BS has no such feature.

21.3.2 RTCVAL REGISTER MAPPINGS

REGISTER 21-4: RTCCON2H: RTCC CONTROL REGISTER 2 (HIGH)(1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

Note 1: A write to this register is only allowed when WRLOCK = 1.

REGISTER 21-5: RTCCON3L: RTCC CONTROL REGISTER 3 (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSAMP<7:0>:** Power Control Sample Window Timer bits
11111111 = Sample window is always enabled, even when PWCEN = 0
11111110 = Sample window is 254 TPWCCLK clock periods
•
•
•
00000001 = Sample window is 1 TPWCCLK clock period
00000000 = No sample window

bit 7-0 **PWCSTAB<7:0>:** Power Control Stability Window Timer bits(1)
11111111 = Stability window is 255 TPWCCLK clock periods
11111110 = Stability window is 254 TPWCCLK clock periods
•
•
•
00000001 = Stability window is 1 TPWCCLK clock period
00000000 = No stability window; sample window starts when the alarm event triggers

Note 1: The sample window always starts when the stability window timer expires, except when its initial value is 00h.

REGISTER 21-16: TSATIMEH: RTCC TIMESTAMP A TIME REGISTER (HIGH)(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours '10' Digit bits
Contains a value from 0 to 2.

bit 11-8 **HRONE<3:0>:** Binary Coded Decimal Value of Hours '1' Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes '10' Digit bits
Contains a value from 0 to 5.

bit 3-0 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes '1' Digit bits
Contains a value from 0 to 9.

Note 1: If TSAEN = 0, bits<15:0> can be used for persistence storage throughout a non-Power-on Reset ($\overline{\text{MCLR}}$, WDT, etc.).

TABLE 32-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.0	—	3.6	V	BOR is disabled
			VBOR	—	3.6	V	BOR is enabled
DC12	VDR	**RAM Data Retention Voltage(1)**	Greater of: VPORREL or VBOR	—	—	V	VBOR is used only if BOR is enabled (BOREN = 1)
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	—	V	**(Note 2)**
DC17A	SVDD	**Recommended VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1V/20 ms	—	1V/10 µS	sec	**(Note 2, Note 4)**
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	2.1	2.2	V	**(Note 3)**

Note 1: This is the limit to which VDD may be lowered and the RAM contents will always be retained.

2: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

3: On a rising VDD power-up sequence, application firmware execution begins at the higher of the VPORREL or VBOR level (when BOREN = 1).

4: VDD rise times outside this window may not internally reset the processor and are not parametrically tested.

TABLE 32-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

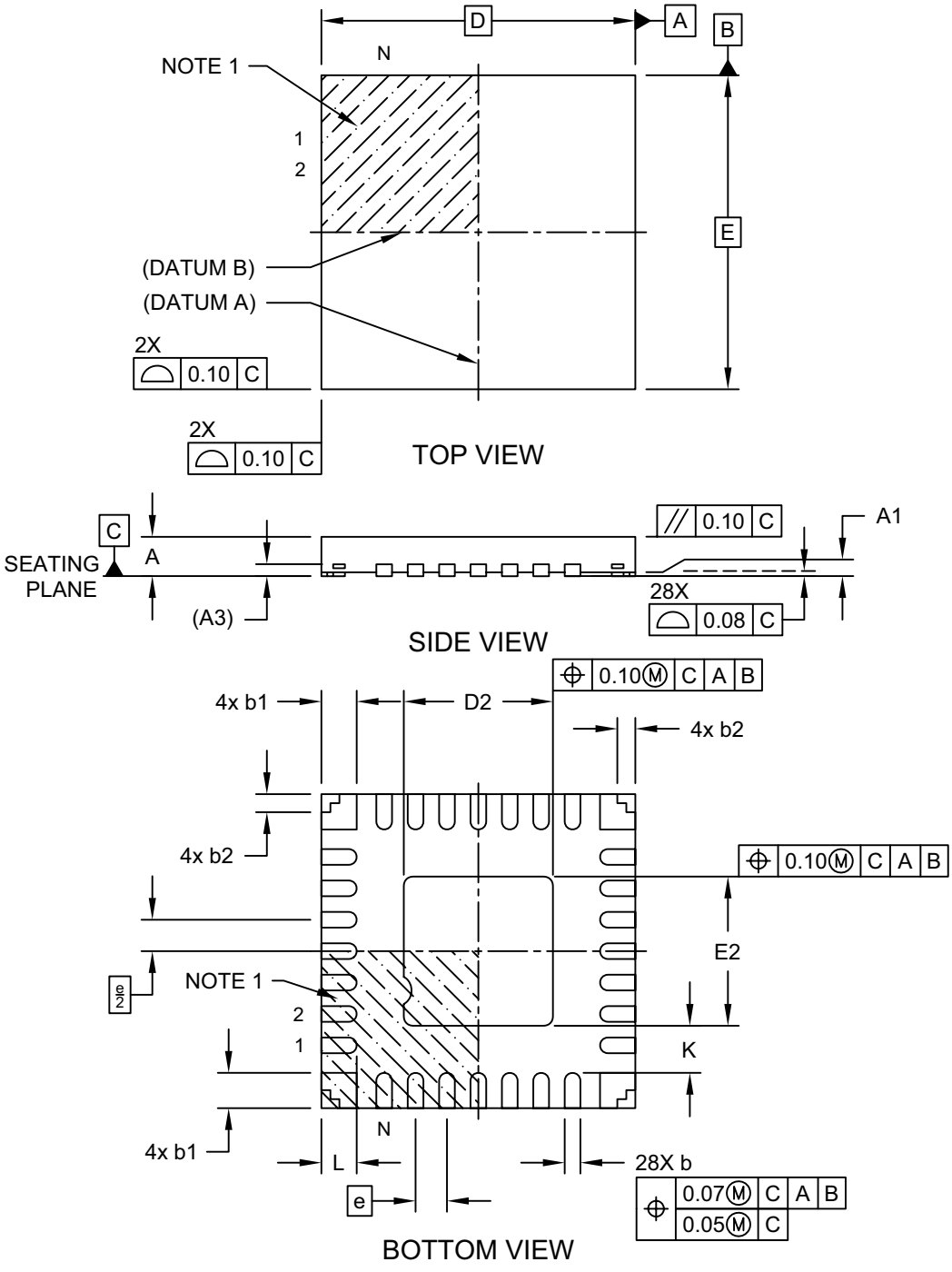
DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Operating Current (IDD)(2)						
DC19	230	365	μA	-40°C to +85°C	2.0V	0.5 MIPS, FOSC = 1 MHz
	250	365	μA	-40°C to +85°C	3.3V	
DC20	430	640	μA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	440	640	μA	-40°C to +85°C	3.3V	
DC23	1.5	2.4	mA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	1.65	2.4	mA	-40°C to +85°C	3.3V	
DC24	6.1	7.7	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	6.3	7.7	mA	-40°C to +85°C	3.3V	
DC31	43	130	μA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	46	130	μA	-40°C to +85°C	3.3V	
DC32	1.6	2.5	mA	-40°C to +85°C	2.0V	FRC (4 MIPS), FOSC = 8 MHz
	1.65	2.5	mA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Typical parameters are for design guidance only and are not tested.

2: The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail-to-rail. All I/O pins are configured as outputs and driving low. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. CPU, program memory and data memory are operational. No peripheral modules are operating or being clocked (defined PMDx bits are all '1's). JTAG interface is disabled.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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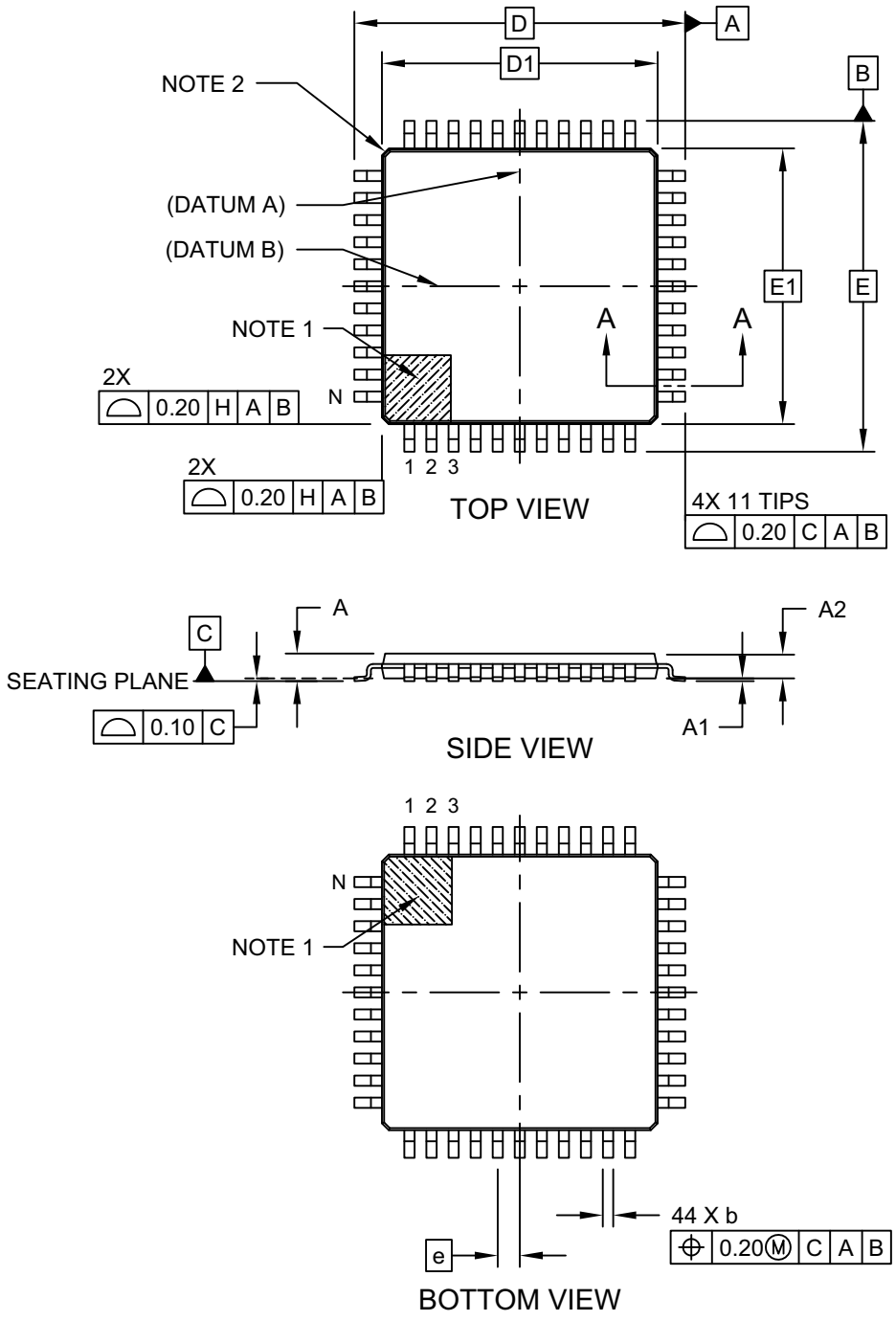
44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

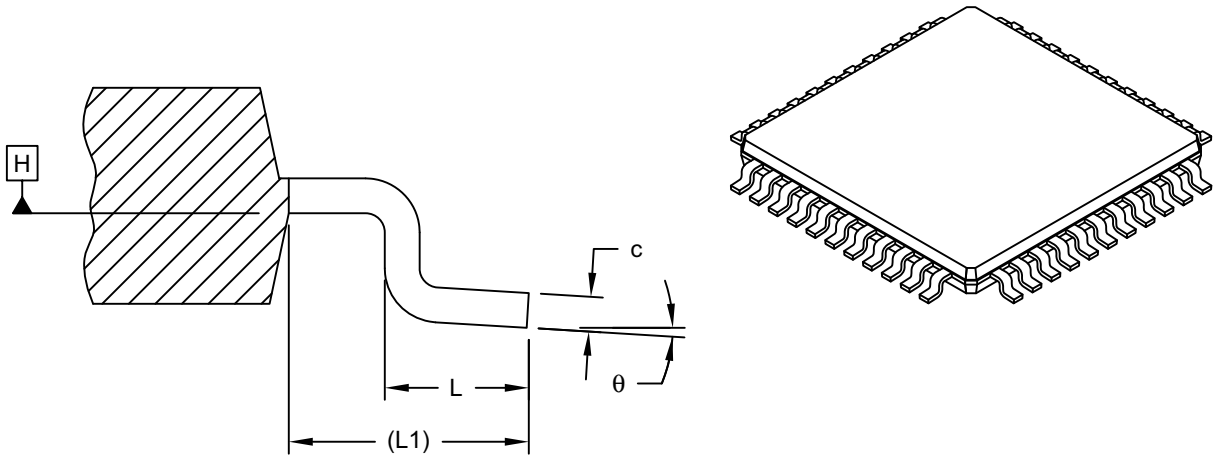
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-076C Sheet 1 of 2

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2