Microchip Technology - PIC24FJ256GA705-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga705-i-pt

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJXXXGA702: 28-PIN DEVICES

Features	PIC24FJ64GA702	PIC24FJ128GA702	PIC24FJ256GA702
Operating Frequency	DC – 32 MHz		
Program Memory (bytes)	64K	128K	256K
Program Memory (instruction words, 24 bits)	22,528	45,056	88,064
Data Memory (bytes)	16K		
Interrupt Sources (soft vectors/NMI traps)	124		
I/O Ports	Ports A, B		
Total I/O Pins	22		
Remappable Pins	18 (18 I/Os, 0 input only)		
DMA	1 6-channel		
16-Bit Timers	3(1)		
Real-Time Clock and Calendar (RTCC)	Yes		
Cyclic Redundancy Check (CRC)	Yes		
Input Capture Channels	3(1)		
Output Compare/PWM Channels	3(1)		
Input Change Notification Interrupt	21 (remappable pins)		
Serial Communications:			
UART	2(1)		
SPI (3-wire/4-wire)	3(1)		
I^2C	2		
Configurable Logic Cell (CLC)	2(1)		
Parallel Communications (EPMP/PSP)	No		
Capture/Compare/PWM/Timer Modules	4 Multiple CCPs 1 (6-output), 3 (2-output)		
JTAG Boundary Scan	Yes		
10/12-Bit Analog-to-Digital Converter (A/D) Module (input channels)	10		
Analog Comparators	3		
CTMU Interface	Yes		
Universal Serial Bus Controller	No		
Resets (and Delays)	Core POR, VDD POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)		
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations		
Packages	28-Pin QFN, UQFN, SOIC, SSOP and SPDIP		

Note 1: Some peripherals are accessible through remappable pins.

4.0 MEMORY ORGANIZATION

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"PIC24F Flash Program Memory"** (DS30009715), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and buses. This architecture also allows direct access of program memory from the Data Space during code execution.

4.1 Program Memory Space

The program address memory space of the PIC24FJ256GA705 family devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or Data Space remapping, as described in **Section 4.3 "Interfacing Program and Data Memory Spaces"**.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and customer OTP sections of the configuration memory space.

The memory map for the PIC24FJ256GA705 family of devices is shown in Figure 4-1.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCUs and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode, [Ws++], will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The Most Significant Byte (MSB) is not modified.

A Sign-Extend (SE) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing with a 16-bit address field.

4.2.4 SPECIAL FUNCTION REGISTER (SFR) SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A diagram of the SFR space, showing where the SFRs are actually implemented, is shown in Table 4-3. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete list of implemented SFRs, including their addresses, is shown in Table 4-4 through 4-11.

TABLE 4-3: IMPLEMENTED REGIONS OF SFR DATA SPACE(2)

	SFR Space Address															
	xx00	**xx10**	**xx20**	**xx30**	**xx40**	**xx50**	**xx60**	**xx70**	**xx80**	**xx90**	**xxA0**	**xxB0**	**xxC0**	**xxD0**	**xxE0**	**xxF0**
000h	Core															
100h	OSC	Reset(1)	EPMP			CRC	REFO	PMD		Timers		—	CTMU	RTCC		
200h	Capture			Compare			MCCP								Comp	ANCFG
300h	MCCP				—	—	—	—	—	UART				—	—	— SPI
400h	SPI					—	CLC		—	—	I^2C			DMA		
500h	DMA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
600h	—	—	—	—	—	I/O										—
700h	—	A/D					NVM	—	—	PPS						

Legend: — = No implemented SFRs in this block

Note 1: Includes HLVD control.

2: Regions shown are approximate. Refer to Table 4-4 through Table 4-11 for exact addresses.

TABLE 4-6: SFR MAP: 0200h BLOCK (CONTINUED)

File Name	Address	All Resets	File Name	Address	All Resets
COMPARATORS			**COMPARATORS (CONTINUED)**		
CMSTAT	02E6	0000	CM3CON	02EE	0000
CVRCON	02E8	00xx	**ANALOG CONFIGURATION**		
CM1CON	02EA	0000	ANCFG	02F4	0000
CM2CON	02EC	0000			

Legend: x = undefined. Reset values are shown in hexadecimal.

TABLE 4-7: SFR MAP: 0300h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
MULTIPLE OUTPUT CAPTURE/COMPARE/PWM			**UART**		
CCP4CON1L	0300	0000	U1MODE	0398	0000
CCP4CON1H	0302	0000	U1STA	039A	0110
CCP4CON2L	0304	0000	U1TXREG	039C	x0xx
CCP4CON2H	0306	0100	U1RXREG	039E	0000
CCP4CON3L	0308	0000	U1BRG	03A0	0000
CCP4CON3H	030A	0000	U1ADMD	03A2	0000
CCP4STATL	030C	00x0	U2MODE	03AE	0000
CCP4STATH	030E	0000	U2STA	03B0	0110
CCP4TMRL	0310	0000	U2TXREG	03B2	xxxx
CCP4TMRH	0312	0000	U2RXREG	03B4	0000
CCP4PRL	0314	FFFF	U2BRG	03B6	0000
CCP4PRH	0316	FFFF	U2ADMD	03B8	0000
CCP4RAL	0318	0000	**SPI**		
CCP4RAH	031A	0000	SPI1CON1L	03F4	0x00
CCP4RBL	031C	0000	SPI1CON1H	03F6	0000
CCP4RBH	031E	0000	SPI1CON2L	03F8	0000
CCP4BUFL	0320	0000	SPI1STATL	03FC	0028
CCP4BUFH	0322	0000	SPI1CON2H	03F8	0000
			SPI1STATH	03FE	0000

Legend: x = undefined. Reset values are shown in hexadecimal.

7.1 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSC<2:0> bits in the FOSCSEL Flash Configuration Word (see Table 7-2). The RCFGCAL and NVMCON registers are only affected by a POR.

7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-3. Note that the Master Reset Signal, $\overline{\text{SYSRST}}$, is released after the POR delay time expires.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The Fail-Safe Clock Monitor (FSCM) delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

7.3 Brown-out Reset (BOR)

PIC24FJ256GA705 family devices implement a BOR circuit that provides the user with several configuration and power-saving options. The BOR is controlled by the BOREN<1:0> (FPOR<1:0>) Configuration bits.

When BOR is enabled, any drop of V_{DD} below the BOR threshold results in a device BOR. Threshold levels are described in **Section 32.1 "DC Characteristics"**.

7.4 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 7-2. If clock switching is disabled, the system clock source is always selected according to the Oscillator Configuration bits. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual*", **"Oscillator"** (DS39700).

TABLE 7-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC<2:0> Configuration bits (FOSCSEL<2:0>)
BOR	
$\overline{\text{MCLR}}$	COSC<2:0> Control bits (OSCCON<14:12>)
WDTO	
SWR	

9.1 CPU Clocking Scheme

The system clock source can be provided by one of four sources:

- Primary Oscillator (POSC) on the OSCI and OSCO pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins
- Fast Internal RC (FRC) Oscillator
- Low-Power Internal RC (LPRC) Oscillator

The Primary Oscillator and FRC sources have the option of using the internal PLL block, which can generate a 4x, 6x or 8x PLL clock. If the PLL is used, the PLL clocks can then be postscaled, if necessary, and used as the system clock. Refer to **Section 9.5 "Oscillator Modes"** for additional information. The internal FRC provides an 8 MHz clock source.

Each clock source (PRIPLL, FRCPLL, PRI, FRC, LPRC and SOSC) can be used as an input to an additional divider, which can then be used to produce a divided clock source for use as a system clock (OSCFDIV).

The selected clock source generates the processor and peripheral clock sources. The processor clock source is divided by two to produce the internal instruction cycle clock, FCY. In this document, the instruction cycle clock is also denoted by FOSC/2. The internal instruction cycle clock, FOSC/2, can be provided on the OSCO I/O pin for some operating modes of the Primary Oscillator.

9.2 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory (refer to **Section 29.1 "Configuration Bits"** for further details). The Primary Oscillator Configuration bits, POSCMD<1:0> (FOSC<1:0>), and the Oscillator Select Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), select the oscillator source that is used at a Power-on Reset. The OSCFDIV clock source is the default (unprogrammed) selection; the default input source to the OSCFDIV divider is the FRC clock source. Other oscillators may be chosen by programming these bit locations.

The Configuration bits allow users to choose between the various Clock modes shown in Table 9-1.

9.2.1 CLOCK SWITCHING MODE CONFIGURATION BITS

The FCKSM<1:0> Configuration bits (FOSC<7:6>) are used to jointly configure device clock switching and the Fail-Safe Clock Monitor (FSCM). Clock switching is enabled only when FCKSM1 is programmed ('0'). The FSCM is enabled only when FCKSM<1:0> are both programmed ('00').

TABLE 10-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	—	—	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
PMD2	—	—	—	—	—	IC3MD	IC2MD	IC1MD	—	—	—	—	—	OC3MD	OC2MD	OC1MD	0000
PMD3	—	—	—	—	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	LVDMD	—	0000
PMD5	—	—	—	—	—	—	—	—	—	—	—	—	CCP4MD	CCP3MD	CCP2MD	CCP1MD	0000
PMD6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPI3MD	0000
PMD7	—	—	—	—	—	—	—	—	—	—	DMA1MD	DMA0MD	—	—	—	—	0000
PMD8	—	—	—	—	—	—	—	—	—	—	—	—	CLC2MD	CLC1MD	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 11-29: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **CLCINBR<5:0>:** Assign CLC Input B to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **CLCINAR<5:0>:** Assign CLC Input A to Corresponding RPn or RPIn Pin bits

REGISTER 11-30: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK3R5	SCK3R4	SCK3R3	SCK3R2	SCK3R1	SCK3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI3R5	SDI3R4	SDI3R3	SDI3R2	SDI3R1	SDI3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

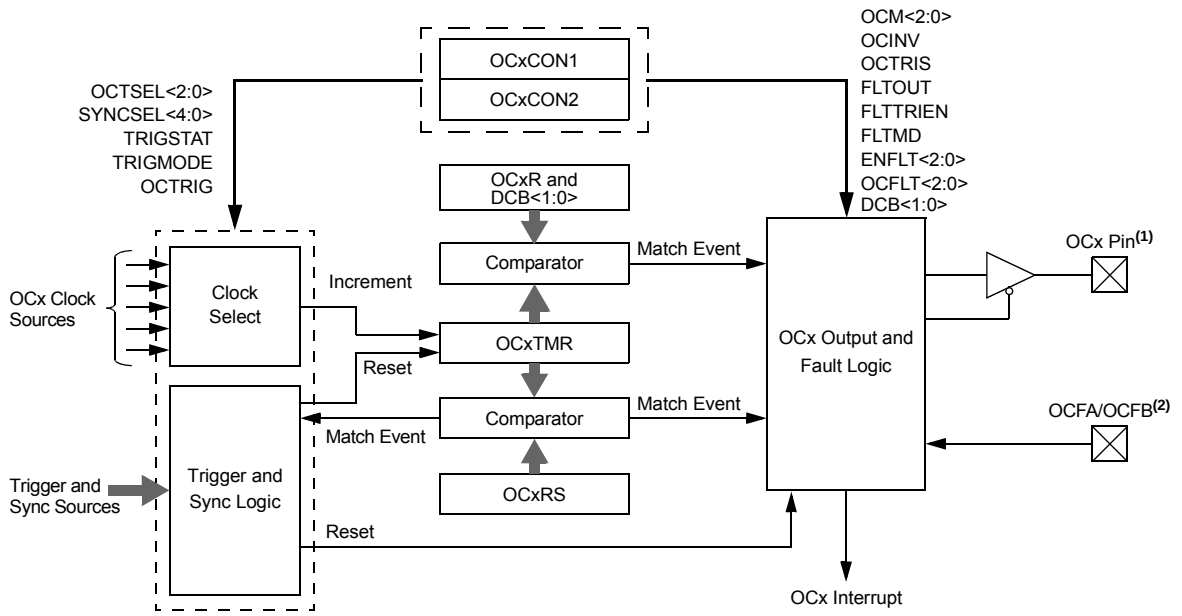
bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK3R<5:0>:** Assign SPI3 Clock Input (SCK3IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI3R<5:0>:** Assign SPI3 Data Input (SDI3) to Corresponding RPn or RPIn Pin bits

FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

15.2 Compare Operations

In Compare mode (Figure 15-1), the output compare module can be configured for Single-Shot or Continuous mode pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins if available on the OCx module you are using. Otherwise, configure the dedicated OCx output pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate the time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= `0xx`).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure Trigger mode operation and TRIGSTAT to select a hardware or software trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the Trigger or Sync source. If free-running timer operation is required, set the SYNCSELx bits to '`00000`' (no Sync/Trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bit for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a Trigger source event occurs.

15.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 15-1 for PWM mode timing details. Table 15-1 and Table 15-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

EQUATION 15-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{CY}}{F_{PWM} \bullet (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

EXAMPLE 15-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS(1)

1. Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where FOSC = 32 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.

   TCY = 2 • TOSC = 62.5 ns

   PWM Period = 1/PWM Frequency = 1/52.08 kHz = 19.2 µS

   PWM Period = (PR2 + 1) • TCY • (Timer2 Prescale Value)

   19.2 µS = (PR2 + 1) • 62.5 ns • 1

   PR2 = 306

2. Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:

   PWM Resolution = $\log_{10}(F_{CY}/F_{PWM})/\log_{10}2)$ bits

   = $(\log_{10}(16\text{ MHz}/52.08\text{ kHz})/\log_{10}2)$ bits

   = 8.3 bits

Note 1: Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

TABLE 15-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (FCY = 4 MHz)(1)

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

TABLE 15-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (FCY = 16 MHz)(1)

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

NOTES:

16.5 Auxiliary Output

The MCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other MCCPx modules, or other digital peripherals, to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT<1:0> control bits (CCPxCON2H<4:3>). The type of output signal is also dependent on the module operating mode.

On the PIC24FJ256GA705 family of devices, only the CTMU discharge trigger has access to the auxiliary output signal.

TABLE 16-4: AUXILIARY OUTPUT

AUXOUT<1:0>	CCSEL	MOD<3:0>	Comments	Signal Description
00	x	xxxx	Auxiliary Output Disabled	No Output
01	0	0000	Time Base Modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare Modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture Modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

REGISTER 16-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot trigger event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit (1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits (1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in the MCCP1 module only.

REGISTER 16-7: CCPxSTATL: CCPx STATUS REGISTER LOW

U-0	U-0	U-0	U-0	U-0	W-0	U-0	U-0
—	—	—	—	—	ICGARM	—	—
bit 15							bit 8

R-0	W1-0	W1-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
bit 7							bit 0

Legend:	C = Clearable bit	W = Writable bit	
R = Readable bit	W1 = Write '1' Only bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **ICGARM:** Input Capture Gate Arm bit

A write of '1' to this location will arm the Input Capture x module for a one-shot gating event when ICGSM<1:0> = 01 or 10; read as '0'.

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CCPTRIG:** CCPx Trigger Status bit

1 = Timer has been triggered and is running
0 = Timer has not been triggered and is held in Reset

bit 6 **TRSET:** CCPx Trigger Set Request bit

Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

bit 5 **TRCLR:** CCPx Trigger Clear Request bit

Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit

1 = A shutdown event is in progress; CCPx outputs are in the shutdown state
0 = CCPx outputs operate normally

bit 3 **SCEVT:** Single Edge Compare Event Status bit

1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture x Disable bit

1 = Event on Input Capture x pin (ICMx) does not generate a capture event
0 = Event on Input Capture x pin will generate a capture event

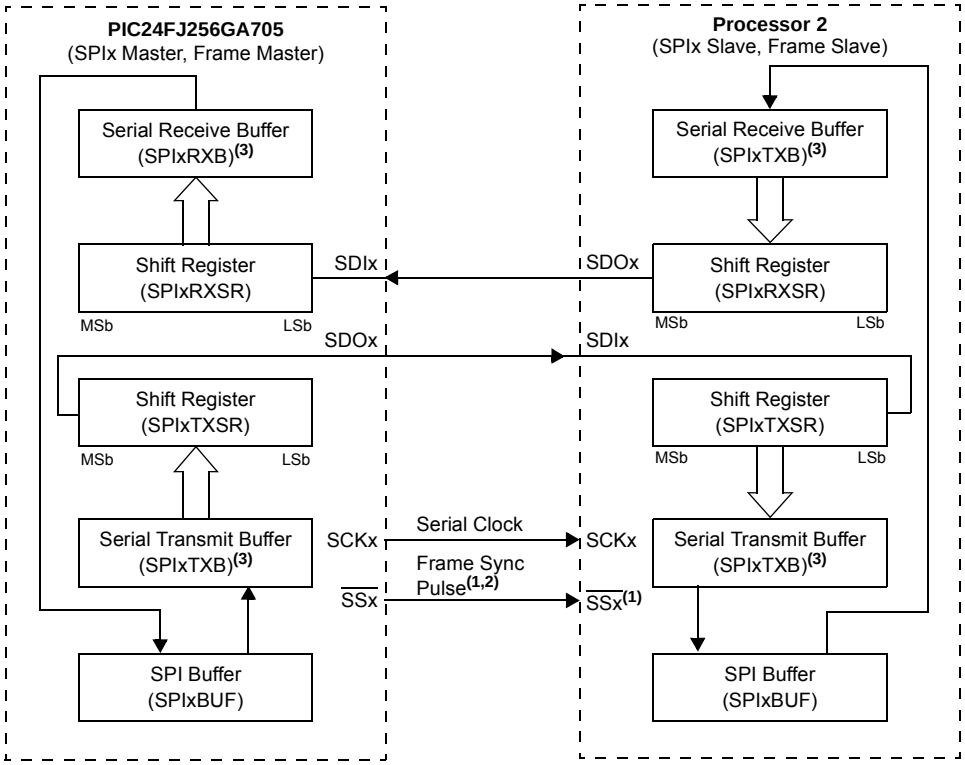
bit 1 **ICOV:** Input Capture x Buffer Overflow Status bit

1 = The Input Capture x FIFO buffer has overflowed
0 = The Input Capture x FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture x Buffer Status bit

1 = Input Capture x buffer has data available
0 = Input Capture x buffer is empty

FIGURE 17-4: SPIx MASTER, FRAME MASTER CONNECTION DIAGRAM



Note 1: In Framed SPI modes, the $\overline{SSx}$ pin is used to transmit/receive the Frame Synchronization pulse.
2: Framed SPI modes require the use of all four pins (i.e., using the $\overline{SSx}$ pin is not optional).
3: The SPIxTXB and SPIxRXB registers are memory-mapped to the SPIxBUF register.

18.2 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator reload value, use Equation 18-1.

EQUATION 18-1: COMPUTING BAUD RATE RELOAD VALUE(1,2,3)

$$F_{SCL} = \frac{F_{CY}}{(I2CxBRG + 2) * 2}$$

or:

$$I2CxBRG = \left[\frac{F_{CY}}{(F_{SCL} * 2)} - 2 \right]$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

3: BRG values of 0 and 1 are forbidden.

18.3 Slave Address Masking

The I2CxMSK register (Register 18-4) designates address bit positions as "don't care" for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the slave module to respond, whether the corresponding address bit value is a '0' or a '1'. For example, when I2CxMSK is set to '0010000000', the slave module will detect both addresses, '0000000000' and '0010000000'.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the STRICT bit (I2CxCONL<11>).

Note: As a result of changes in the I^2C protocol, the addresses in Table 18-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 18-1: I2Cx CLOCK RATES(1,2)

Required System FSCL	FCY	I2CxBRG Value		Actual FSCL
		(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	78	4E	100 kHz
100 kHz	8 MHz	38	26	100 kHz
100 kHz	4 MHz	18	12	100 kHz
400 kHz	16 MHz	18	12	400 kHz
400 kHz	8 MHz	8	8	400 kHz
400 kHz	4 MHz	3	3	400 kHz
1 MHz	16 MHz	6	6	1.000 MHz
1 MHz	8 MHz	2	2	1.000 MHz

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

TABLE 18-2: I2Cx RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 0xx	x	10-Bit Slave Upper Byte(3)
1111 1xx	x	Reserved

Note 1: The address bits listed here will never cause an address match independent of address mask settings.

2: This address will be Acknowledged only if GCEN = 1.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

22.1.3 DATA SHIFT DIRECTION

The LENDIAN bit (CRCCON1<3>) is used to control the shift direction. By default, the CRC will shift data through the engine, MSb first. Setting LENDIAN (= 1) causes the CRC to shift data, LSb first. This setting allows better integration with various communication schemes and removes the overhead of reversing the bit order in software. Note that this only changes the direction the data is shifted into the engine. The result of the CRC calculation will still be a normal CRC result, not a reverse CRC result.

22.1.4 INTERRUPT OPERATION

The module generates an interrupt that is configurable by the user for either of two conditions.

If CRCISEL is '0', an interrupt is generated when the VWORD<4:0> bits make a transition from a value of '1' to '0'. If CRCISEL is '1', an interrupt will be generated after the CRC operation finishes and the module sets the CRCGO bit to '0'. Manually setting CRCGO to '0' will not generate an interrupt. Note that when an interrupt occurs, the CRC calculation would not yet be complete. The module will still need (PLENx + 1)/2 clock cycles after the interrupt is generated until the CRC calculation is finished.

22.1.5 TYPICAL OPERATION

To use the module for a typical CRC calculation:

1. Set the CRCEN bit to enable the module.
2. Configure the module for desired operation:
   a) Program the desired polynomial using the CRCXOR registers and PLEN<4:0> bits.
   b) Configure the data width and shift direction using the DWIDTH<4:0> and LENDIAN bits.
3. Set the CRCGO bit to start the calculations.
4. Set the desired CRC non-direct initial value by writing to the CRCWDAT registers.
5. Load all data into the FIFO by writing to the CRCDAT registers as space becomes available (the CRCFUL bit must be zero before the next data loading).
6. Wait until the data FIFO is empty (CRCMPT bit is set).
7. Read the result:
   If the data width (DWIDTH<4:0> bits) is more than the polynomial length (PLEN<4:0> bits):
   a) Wait (DWIDTH<4:0> + 1)/2 instruction cycles to make sure that shifts from the shift buffer are finished.
   b) Change the data width to the polynomial length (DWIDTH<4:0> = PLEN<4:0>).
   c) Write one dummy data word to the CRCDAT registers.
   d) Wait 2 instruction cycles to move the data from the FIFO to the shift buffer and (PLEN<4:0> + 1)/2 instruction cycles to shift out the result.

   Or, if the data width (DWIDTH<4:0> bits) is less than the polynomial length (PLEN<4:0> bits):
   1. Clear the CRC Interrupt Selection bit (CRCISEL = 0) to get the interrupt when all shifts are done. Clear the CRC interrupt flag. Write dummy data in the CRCDAT registers and wait until the CRC interrupt flag is set.
   2. Read the final CRC result from the CRCWDAT registers.
   3. Restore the data width (DWIDTH<4:0> bits) for further calculations (OPTIONAL). If the data width (DWIDTH<4:0> bits) is equal to, or less than, the polynomial length (PLEN<4:0> bits):
      a) Clear the CRC Interrupt Selection bit (CRCISEL = 0) to get the interrupt when all shifts are done.
      b) Suspend the calculation by setting CRCGO = 0.
      c) Clear the CRC interrupt flag.
      d) Write the dummy data with the total data length equal to the polynomial length in the CRCDAT registers.
      e) Resume the calculation by setting CRCGO = 1.
      f) Wait until the CRC interrupt flag is set.
      g) Read the final CRC result from the CRCWDAT registers.

There are eight registers used to control programmable CRC operation:

- CRCCON1
- CRCCON2
- CRCXORL
- CRCXORH
- CRCDATL
- CRCDATH
- CRCWDATL
- CRCWDATH

The CRCCON1 and CRCCON2 registers (Register 22-1 and Register 22-2) control the operation of the module and configure the various settings.

The CRCXOR registers (Register 22-3 and Register 22-4) select the polynomial terms to be used in the CRC equation. The CRCDAT and CRCWDAT registers are each register pairs that serve as buffers for the double-word input data, and CRC processed output, respectively.

REGISTER 24-11: AD1CTMENH: A/D CTMU ENABLE REGISTER (HIGH WORD)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	CTMEN<30:28>			—	—	CTMEN<25:24>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<23:16>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CTMEN<30:28>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

bit 11-10 **Unimplemented:** Read as '0'

bit 9-0 **CTMEN<25:16>:** CTMU Enabled During Conversion bits(1)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: CTMEN<23:16> bits are not available on 64-pin parts.

REGISTER 24-12: AD1CTMENL: A/D CTMU ENABLE REGISTER (LOW WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CTMEN<15:0>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

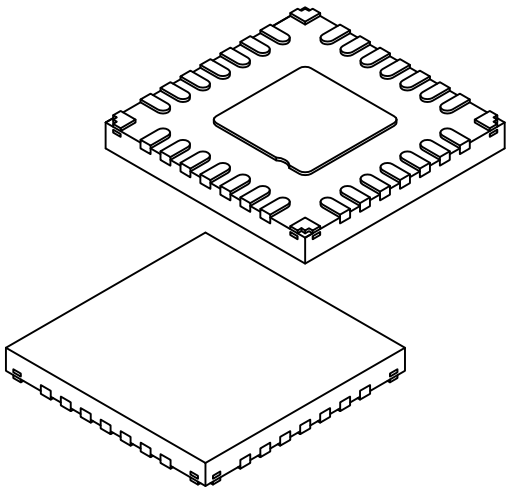
30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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