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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga702-i-ss

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJ256GA704 TQFP)

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/$\overline{\text{TMPRN}}$/**RP9**/SDA1/T1CK/CTED4/PMD3/RB9	23	AN4/C1INB/**RP2**/SDA2/CTED13/RB2
2	**RP22**/PMA1/PMALH/RC6	24	AN5/C1INA/**RP3**/SCL2/CTED8/RB3
3	**RP23**/PMA0/PMALL/RC7	25	AN10/**RP16**/PMBE1/RC0
4	**RP24**/PMA5/RC8	26	AN11/**RP17**/PMA15/PMCS2/RC1
5	**RP25**/CTED7/PMA6/RC9	27	AN12/**RP18**/PMACK1/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGD2/**RP10**/OCM1C/CTED11/PMD2/RB10	30	OSCI/CLKI/C1IND/RA2
9	PGC2/REFI1/**RP11**/CTED9/PMD1/RB11	31	OSCO/CLKO/C2IND/RA3
10	AN8/LVDIN/**RP12**/PMD0/RB12	32	TDO/PMA8/RA8
11	AN7/C1INC/**RP13**/OCM1D/CTPLS/PMRD/$\overline{\text{PMWR}}$/RB13	33	SOSCI/**RP4**/RB4
12	TMS/**RP28**/PMA2/PMALU/RA10	34	SOSCO/PWRLCLK/RA4
13	TCK/PMA7/RA7	35	TDI/PMA9/RA9
14	CVREF/AN6/C3INB/**RP14**/CTED5/PMWR/PMENB/RB14	36	AN13/**RP19**/PMBE0/RC3
15	AN9/C3INA/**RP15**/CTED6/PMA14/PMCS/PMCS1/RB15	37	**RP20**/PMA4/RC4
16	AVSS	38	**RP21**/PMA3/RC5
17	AVDD	39	Vss
18	$\overline{\text{MCLR}}$	40	VDD
19	VREF+/CVREF+/AN0/C3INC/**RP26**/CTED1/RA0	41	PGD3/**RP5**/ASDA1/OCM1E/PMD7/RB5
20	VREF-/CVREF-/AN1/C3IND/**RP27**/CTED2/RA1	42	PGC3/**RP6**/ASCL1/OCM1F/PMD6/RB6
21	PGD1/AN2/CTCMP/C2INB/**RP0**/RB0	43	**RP7**/OCM1A/CTED3/PMD5/INT0/RB7
22	PGC1/AN1-/AN3/C2INA/**RP1**/CTED12/RB1	44	**RP8**/SCL1/OCM1B/CTED10/PMD4/RB8

Legend: **RPn** represents remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJXXXGA70X: 44-PIN AND 48-PIN DEVICES

Features	PIC24FJ64GA70X	PIC24FJ128GA70X	PIC24FJ256GA70X
Operating Frequency	DC – 32 MHz		
Program Memory (bytes)	64K	128K	256K
Program Memory (instruction words, 24 bits)	22,528	45,056	88,064
Data Memory (bytes)	16K		
Interrupt Sources (soft vectors/NMI traps)	124		
I/O Ports	Ports A, B, C		
Total I/O Pins:			
44-pin	35	35	35
48-pin	39	39	39
Remappable Pins:			
44-pin	29 (29 I/Os, 0 input only)		
48-pin	33 (29 I/Os, 4 input only)		
DMA (6-channel)	1		
16-Bit Timers	3(1)		
Real-Time Clock and Calendar (RTCC)	Yes		
Cyclic Redundancy Check (CRC)	Yes		
Input Capture Channels	3(1)		
Output Compare/PWM Channels	3(1)		
Input Change Notification Interrupt	25 (remappable pins)		
Serial Communications:			
UART	2(1)		
SPI (3-wire/4-wire)	3(1)		
I^2C	2		
Configurable Logic Cell (CLC)	2(1)		
Parallel Communications (EPMP/PSP)	Yes		
Capture/Compare/PWM/Timer Modules (MCCP)	4 Modules 1 (6-output), 3 (2-output)		
JTAG Boundary Scan	Yes		
10/12-Bit Analog-to-Digital Converter (A/D) Module (input channels)	14		
Analog Comparators	3		
CTMU Interface	Yes		
Universal Serial Bus Controller	No		
Resets (and delays)	Core POR, VDD POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)		
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations		
Packages	44-Pin TQFP, 48-Pin TQFP and QFN		

Note 1: Some peripherals are accessible through remappable pins.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCUs and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode, [Ws++], will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The Most Significant Byte (MSB) is not modified.

A Sign-Extend (SE) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing with a 16-bit address field.

4.2.4 SPECIAL FUNCTION REGISTER (SFR) SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A diagram of the SFR space, showing where the SFRs are actually implemented, is shown in Table 4-3. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete list of implemented SFRs, including their addresses, is shown in Table 4-4 through 4-11.

TABLE 4-3: IMPLEMENTED REGIONS OF SFR DATA SPACE(2)

	SFR Space Address															
	xx00	**xx10**	**xx20**	**xx30**	**xx40**	**xx50**	**xx60**	**xx70**	**xx80**	**xx90**	**xxA0**	**xxB0**	**xxC0**	**xxD0**	**xxE0**	**xxF0**
000h	Core															
100h	OSC	Reset(1)	EPMP			CRC	REFO	PMD		Timers		—	CTMU	RTCC		
200h	Capture			Compare			MCCP								Comp	ANCFG
300h	MCCP				—	—	—	—	—	UART				—	—	— SPI
400h	SPI					—	CLC		—	—	I^2C			DMA		
500h	DMA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
600h	—	—	—	—	—	I/O										—
700h	—	A/D					NVM	—	—	PPS						

Legend: — = No implemented SFRs in this block

Note 1: Includes HLVD control.

2: Regions shown are approximate. Refer to Table 4-4 through Table 4-11 for exact addresses.

4.2.5.2 Data Write into EDS

In order to write data to EDS, such as in EDS reads, an Address Pointer is set up by loading the required EDS page number into the DSWPAG register, and assigning the offset address to one of the W registers. Once the above assignment is done, then the EDS window is enabled by setting bit 15 of the Working register, assigned with the offset address, and the accessed location can be written.

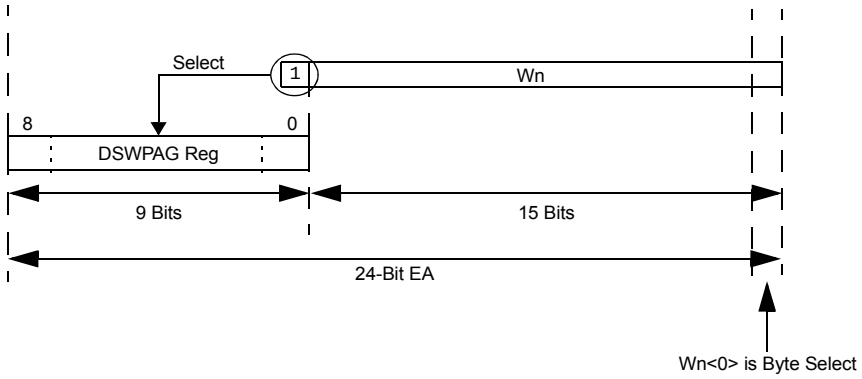
Figure 4-5 illustrates how the EDS address is generated for write operations.

When the MSbs of EA are '1', the lower 9 bits of DSWPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS address for write operations. Example 4-2 shows how to write a byte, word and double word to EDS.

The Data Space Page registers (DSRPAG/DSWPAG) do not update automatically while crossing a page boundary when the rollover happens from 0xFFFF to 0x8000. While developing code in assembly, care must be taken to update the Data Space Page registers when an Address Pointer crosses the page boundary. The 'C' compiler keeps track of the addressing, and increments or decrements the Page registers accordingly, while accessing contiguous data memory locations.

Note 1:	All write operations to EDS are executed in a single cycle.
2:	Use of Read/Modify/Write operation on any EDS location under a `REPEAT` instruction is not supported. For example: `BCLR`, `BSW`, `BTG`, `RLC f`, `RLNC f`, `RRC f`, `RRNC f`, `ADD f`, `SUB f`, `SUBR f`, `AND f`, `IOR f`, `XOR f`, `ASR f`, `ASL f`.
3:	Use the DSRPAG register while performing Read/Modify/Write operations.

FIGURE 4-5: EDS ADDRESS GENERATION FOR WRITE OPERATIONS



EXAMPLE 4-2: EDS WRITE CODE IN ASSEMBLY

```
; Set the EDS page where the data to be written
    mov     #0x0002, w0
    mov     w0, DSWPAG      ;page 2 is selected for write
    mov     #0x0800, w1     ;select the location (0x800) to be written
    bset    w1, #15         ;set the MSB of the base address, enable EDS mode

;Write a byte to the selected location
    mov     #0x00A5, w2
    mov     #0x003C, w3
    mov.b   w2, [w1++]      ;write Low byte
    mov.b   w3, [w1++]      ;write High byte

;Write a word to the selected location
    mov     #0x1234, w2     ;
    mov     w2, [w1]        ;

;Write a Double - word to the selected location
    mov     #0x1122, w2
    mov     #0x4455, w3
    mov.d   w2, [w1]        ;2 EDS writes
```

9.6 Reference Clock Output

In addition to the CLKO output (FOSC/2) available in certain Oscillator modes, the device clock in the PIC24FJ256GA705 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. CLKO is enabled by Configuration bit, OSCIOFCN, and is independent of the REFO reference clock. REFO is mappable to any I/O pin that has mapped output capability. Refer to Table 11-7 for more information.

This reference clock output is controlled by the REFOCONL, REFOCONH and REFOTRIML registers. Setting the ROEN bit (REFOCONL<15>) makes the clock signal available on the REFO pin. The RODIV<14:0> bits (REFOCONH<14:0>) enable the selection of different clock divider options. The ROTRIM<0:8> bits (REFOTRIML<7:15>) allow the user to provide a fractional addition to the RODIVx value. The ROSWEN bit (REFOCONL<9>) indicates that the clock divider has successfully switched. In order to switch the divider or trim the REFO frequency, the user should wait until this bit has been cleared. Write the updated values to ROTRIMx and RODIVx, set the ROSWEN bit and then wait until it is cleared before assuming that the REFO clock is valid.

The ROSEL<3:0> bits (REFOCONL<3:0>) determine which clock source is used for the reference clock output. The ROSLP bit (REFOCONL<11>) determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSLP bit must be set and the clock selected by the ROSELx bits must be enabled for operation during Sleep mode, if possible. Clearing the ROSELx bits allows the reference output frequency to change as the system clock changes during any clock switches. The ROOUT bit enables/disables the reference clock output on the REFO pin.

The ROACTIVE bit (REFOCONL<8>) indicates that the module is active; it can be cleared by disabling the module (setting ROEN to '0'). The user must not change the reference clock source or adjust the trim or divider when the ROACTIVE bit indicates that the module is active. To avoid glitches, the user should not disable the module until the ROACTIVE bit is '1'.

The PLLSS Configuration bit (FOSC<4>), when cleared, can be used to generate a REFO clock with the PLL that is independent of the system clock. The PLL cannot be used in the primary clock chain. For example, if the system clock is using FRC at 8 MHz, the PLL can use the FRC as the input and generate 32 MHz (PLL4x mode) out of REFO.

9.7 Secondary Oscillator

9.7.1 BASIC SOSC OPERATION

PIC24FJ256GA705 family devices do not have to set the SOSCEN bit to use the Secondary Oscillator. Any module requiring the SOSC (such as the RTCC or Timer1) will automatically turn on the SOSC when the clock signal is needed. The SOSC, however, has a long start-up time (as long as 1 second). To avoid delays for peripheral start-up, the SOSC can be manually started using the SOSCEN bit.

To use the Secondary Oscillator, the SOSCSEL bit (FOSC<3>) must be set to '1'. Programming the SOSCSEL bit to '0' configures the SOSC pins for Digital mode, enabling digital I/O functionality on the pins.

9.7.2 CRYSTAL SELECTION

The 32.768 kHz crystal used for the SOSC must have the following specifications in order to properly start up and run at the correct frequency when the SOSC is in High-Power mode (default):

- 12.5 pF loading capacitance
- 1.0 pF shunt capacitance
- A typical ESR of 35K-50K; 70K maximum

In addition, the two external crystal loading capacitors should be in the range of 18-22 pF, which will be based on the PC board layout. The capacitors should be C0G, 5% tolerance and rated 25V or greater.

The accuracy and duty cycle of the SOSC can be measured on the REFO pin, and is recommended to be in the range of 40-60% and accurate to ±0.65 Hz.

9.7.3 LOW-POWER SOSC OPERATION

The Secondary Oscillator can operate in two distinct levels of power consumption based on device configuration. In Low-Power mode, the oscillator operates in a low drive strength, low-power state. By default, the oscillator uses a higher drive strength, and therefore, requires more power. Low-Power mode is selected by Configuration bit, SOSCHP (FDEVOPT1<3>). The lower drive strength of this mode makes the SOSC more sensitive to noise and requires a longer start-up time. This mode can be used with lower load capacitance crystals (6 pF-9 pF) to reduce Sleep current in the RTCC. When Low-Power mode is used, care must be taken in the design and layout of the SOSC circuit to ensure that the oscillator starts up and oscillates properly. PC board layout issues, stray capacitance and other factors will need to be carefully controlled in order for the crystal to operate.

REGISTER 10-8: PMD8: PERIPHERAL MODULE DISABLE REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	CLC2MD	CLC1MD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **CLC2MD:** CLC2 Module Disable bit
- 1 = Module is disabled
- 0 = Module power and clock sources are enabled

bit 2 **CLC1MD:** CLC1 Module Disable bit
- 1 = Module is disabled
- 0 = Module power and clock sources are enabled

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 11-3: TRISx: OUTPUT ENABLE FOR PORTx REGISTER(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TRISx<15:0>:** Output Enable for PORTx bits
1 = LATx[n] is not driven on the PORTx[n] pin
0 = LATx[n] is driven on the PORTx[n] pin

Note 1: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-4: PORTx: INPUT DATA FOR PORTx REGISTER(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PORTx<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PORTx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PORTx<15:0>:** PORTx Data Input Value bits

Note 1: See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-15: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCTRIG2R5	OCTRIG2R4	OCTRIG2R3	OCTRIG2R2	OCTRIG2R1	OCTRIG2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT4R5	INT4R4	INT4R3	INT4R2	INT4R1	INT4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **OCTRIG2R<5:0>:** Assign Output Compare Trigger 2 to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **INT4R<5:0>:** Assign External Interrupt 4 (INT4) to Corresponding RPn or RPIn Pin bits

REGISTER 11-16: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **T3CKR<5:0>**: Assign Timer3 Clock to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **T2CKR<5:0>:** Assign Timer2 Clock to Corresponding RPn or RPIn Pin bits

REGISTER 11-32: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP1R<5:0>:** RP1 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP1 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP0R<5:0>:** RP0 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP0 (see Table 11-7 for peripheral function numbers).

REGISTER 11-33: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP3R<5:0>:** RP3 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP3 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP2R<5:0>:** RP2 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP2 (see Table 11-7 for peripheral function numbers).

REGISTER 11-44: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP25R5	RP25R4	RP25R3	RP25R2	RP25R1	RP25R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP24R5	RP24R4	RP24R3	RP24R2	RP24R1	RP24R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP25R<5:0>:** RP25 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP25 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP24R<5:0>:** RP24 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP24 (see Table 11-7 for peripheral function numbers).

REGISTER 11-45: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP27R5	RP27R4	RP27R3	RP27R2	RP27R1	RP27R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP26R5	RP26R4	RP26R3	RP26R2	RP26R1	RP26R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP27R<5:0>:** RP27 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP27 (see Table 11-7 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP26R<5:0>:** RP26 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP26 (see Table 11-7 for peripheral function numbers).

NOTES:

REGISTER 16-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot trigger event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit (1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits (1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in the MCCP1 module only.

REGISTER 23-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

NOTES:

REGISTER 25-1: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 THROUGH 3) (CONTINUED)

bit 4 **CREF:** Comparator Reference Select bits (non-inverting input)
1 = Non-inverting input connects to the internal CVREF voltage
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of the comparator connects to the internal selectable reference voltage specified by the CVREFM<1:0> bits in the CVRCON register
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

REGISTER 25-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit (read-only)
Shows the current event status of Comparator 3 (CM3CON<9>).

bit 9 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 8 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit (read-only)
Shows the current output of Comparator 3 (CM3CON<8>).

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

FIGURE 29-2: WDT BLOCK DIAGRAM

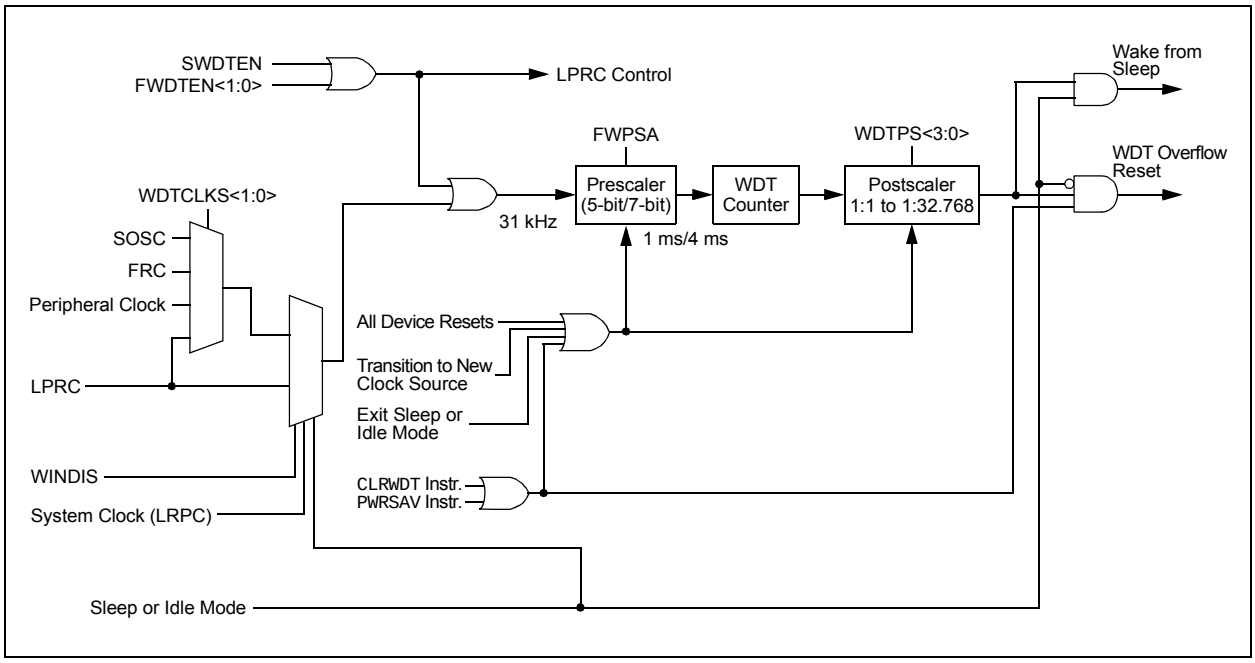


TABLE 32-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Power-Down Current(4,5)						
DC60	2.5	10	μA	-40°C	2.0V	Sleep(2)
	3.2	10	μA	+25°C		
	11.5	45	μA	+85°C		
	3.2	10	μA	-40°C	3.3V	
	4.4	10	μA	+25°C		
	12.2	45	μA	+85°C		
DC61	165	—	nA	-40°C	2.0V	Low-Voltage Retention Sleep(3)
	190	—	nA	+25°C		
	14.5	—	μA	+85°C		
	220	—	nA	-40°C	3.3V	
	300	—	nA	+25°C		
	15	—	μA	+85°C		

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The retention low-voltage regulator is disabled; RETEN (RCON<12>) = 0, $\overline{\text{LPCFG}}$ (FPOR<2>) = 1.

3: The retention low-voltage regulator is enabled; RETEN (RCON<12>) = 1, $\overline{\text{LPCFG}}$ (FPOR<2>) = 0.

4: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and driven low. WDT, BOR and JTAG are all disabled.

5: These currents are measured on the device containing the most memory in this family.

TABLE 32-19: AC SPECIFICATIONS FOR PHASE-LOCKED LOOP MODE

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Sym	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
FIN	Input Frequency Range	2	—	24	MHz	
FMIN	Minimum Output Frequency from the Frequency Multiplier	—	—	16	MHz	4 MHz FIN with 4x feedback ratio, 2 MHz FIN with 8x feedback ratio
FMAX	Maximum Output Frequency from the Frequency Multiplier	96	—	—	MHz	4 MHz FIN with 24x net multiplication ratio, 24 MHz FIN with 4x net multiplication ratio
FSLEW	Maximum Step Function of FIN at which the PLL will be Ensured to Maintain Lock	-4	—	+4	%	Full input range of FIN
TLOCK	Lock Time for VCO	—	—	24	μs	With the specified minimum, TREF, and a lock timer count of one cycle, this is the maximum VCO lock time supported
JFM8	Cumulative Jitter of Frequency Multiplier Over Voltage and Temperature during Any Eight Consecutive Cycles of the PLL Output	—	—	±0.12	%	4 MHz FIN with 4x feedback ratio

TABLE 32-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
F20	FRC Accuracy @ 8 MHz	-1.5	+0.15	1.5	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +85°C **(Note 1)**
		-2	—	2	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ 0°C
F21	LPRC @ 31 kHz	-20	—	20	%	VCAP Output Voltage = 1.8V
F22	OSCTUN Step-Size	—	0.1	—	%/bit	

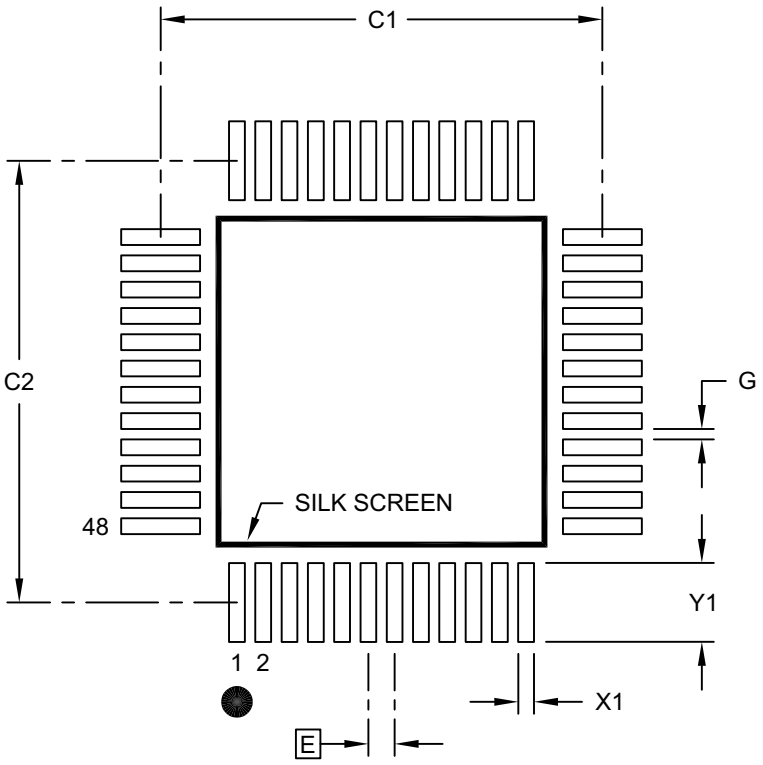
Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

TABLE 32-21: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
FR0	TFRC	FRC Oscillator Start-up Time	—	15	—	μs	
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	—	50	—	μs	

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-PT Rev A

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