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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga702t-i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga702t-i-so</a>

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## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA705
- PIC24FJ128GA705
- PIC24FJ256GA705
- PIC24FJ64GA704
- PIC24FJ128GA704
- PIC24FJ256GA704
- PIC24FJ64GA702
- PIC24FJ128GA702
- PIC24FJ256GA702

The PIC24FJ256GA705 family introduces large Flash and SRAM memory in smaller package sizes. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSP).

Table 1-3 lists the functions of the various pins shown in the pinout diagrams.

### 1.1 Core Features

#### 1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

#### 1.1.2 POWER-SAVING TECHNOLOGY

The PIC24FJ256GA705 family of devices includes Retention Sleep, a low-power mode with essential circuits being powered from a separate low-voltage regulator.

This new low-power mode also supports the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from this new feature, PIC24FJ256GA705 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of the Idle and Sleep modes

#### 1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GA705 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- External Clock (EC) mode
- A Phase-Locked Loop (PLL) frequency multiplier, which allows processor speeds up to 32 MHz
- An internal Fast RC Oscillator (FRC), a nominal 8 MHz output with multiple frequency divider options
- A separate internal Low-Power RC Oscillator (LPRC), 31 kHz nominal for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

#### 1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger device.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

# PIC24FJ256GA705 FAMILY

## 2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

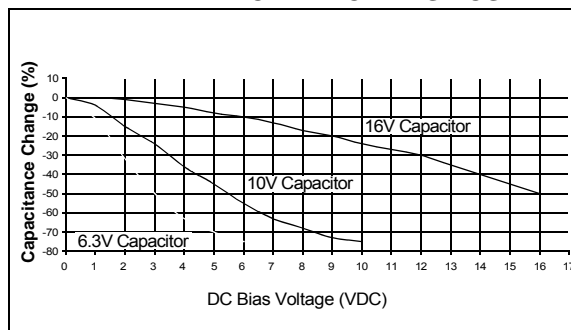
Typical low-cost, 10  $\mu$ F ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as  $\pm 10\%$  to  $\pm 20\%$  (X5R and X7R) or  $-20\%$  to  $+80\%$  (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex:  $\pm 15\%$  over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of  $+22\%$  to  $-82\%$ . Due to the extreme temperature tolerance, a 10  $\mu$ F nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

**FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS**



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at a minimum of 16V for the 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

## 2.5 ICSP Pins

The PGCx and PGDx pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100 $\Omega$ .

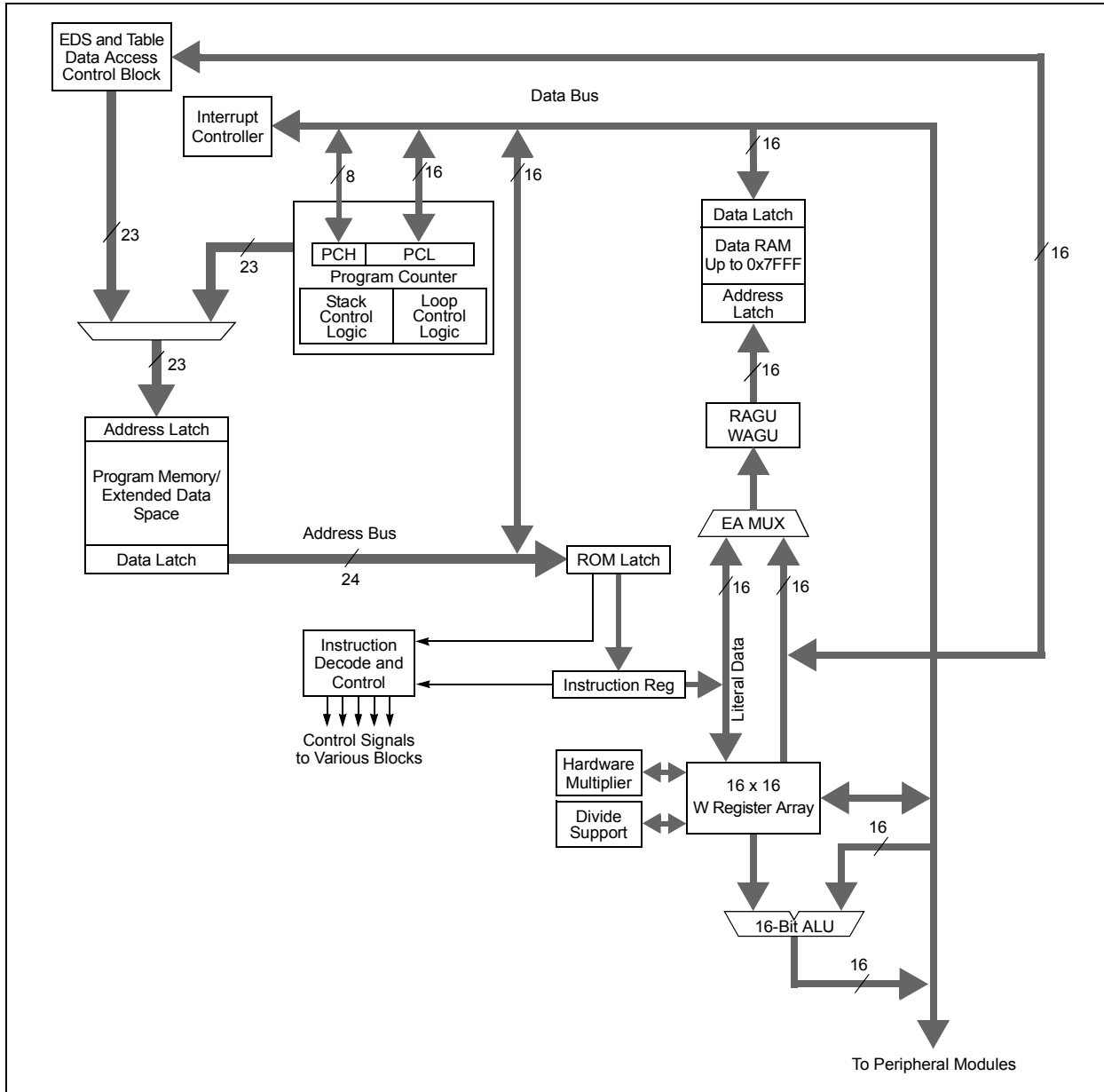
Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Voltage Input High (VIH) and Voltage Input Low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" pins (i.e., PGCx/PGDx) programmed into the device match the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 30.0 "Development Support"**.

# PIC24FJ256GA705 FAMILY

**FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM**



**TABLE 3-1: CPU CORE REGISTERS**

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

# PIC24FJ256GA705 FAMILY

## 4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ ). In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

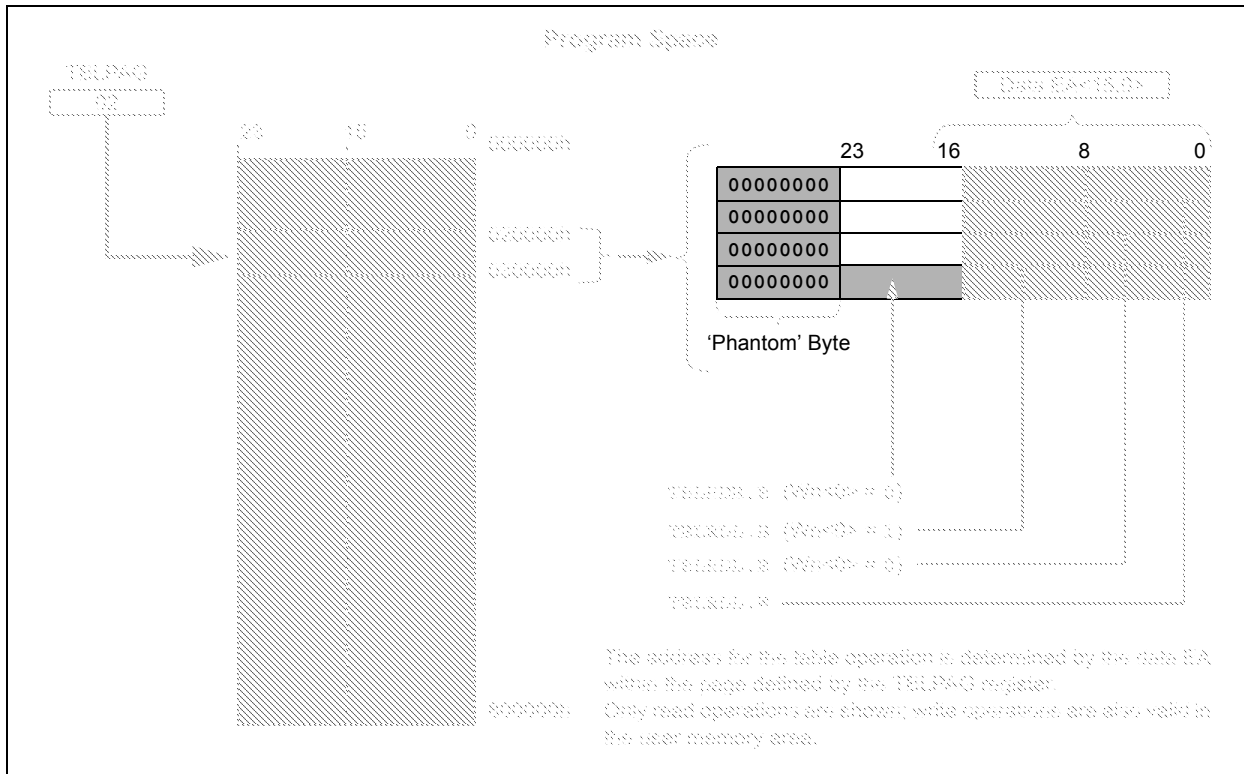
2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. Note that  $D<15:8>$ , the 'phantom' byte, will always be '0'. In Byte mode, it maps the upper or lower byte of the program word to  $D<7:0>$  of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 6.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When  $TBLPAG<7> = 0$ , the table page is located in the user memory space. When  $TBLPAG<7> = 1$ , the page is located in configuration space.

**Note:** Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed.

**FIGURE 4-8: ACCESS PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



# PIC24FJ256GA705 FAMILY

**REGISTER 5-2: DMACHn: DMA CHANNEL n CONTROL REGISTER**

U-0	U-0	U-0	r-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	NULLW	RELOAD <sup>(1)</sup>	CHREQ <sup>(3)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMODE1	SAMODE0	DAMODE1	DAMODE0	TRMODE1	TRMODE0	SIZE	CHEN
bit 7							bit 0

<b>Legend:</b>	r = Reserved bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 15-13	<b>Unimplemented:</b> Read as '0'
bit 12	<b>Reserved:</b> Maintain as '0'
bit 11	<b>Unimplemented:</b> Read as '0'
bit 10	<b>NULLW:</b> Null Write Mode bit 1 = A dummy write is initiated to DMASRCn for every write to DMADSTn 0 = No dummy write is initiated
bit 9	<b>RELOAD:</b> Address and Count Reload bit <sup>(1)</sup> 1 = DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation 0 = DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation <sup>(2)</sup>
bit 8	<b>CHREQ:</b> DMA Channel Software Request bit <sup>(3)</sup> 1 = A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer 0 = No DMA request is pending
bit 7-6	<b>SAMODE&lt;1:0&gt;:</b> Source Address Mode Selection bits 11 = DMASRCn is used in Peripheral Indirect Addressing and remains unchanged 10 = DMASRCn is decremented based on the SIZE bit after a transfer completion 01 = DMASRCn is incremented based on the SIZE bit after a transfer completion 00 = DMASRCn remains unchanged after a transfer completion
bit 5-4	<b>DAMODE&lt;1:0&gt;:</b> Destination Address Mode Selection bits 11 = DMADSTn is used in Peripheral Indirect Addressing and remains unchanged 10 = DMADSTn is decremented based on the SIZE bit after a transfer completion 01 = DMADSTn is incremented based on the SIZE bit after a transfer completion 00 = DMADSTn remains unchanged after a transfer completion
bit 3-2	<b>TRMODE&lt;1:0&gt;:</b> Transfer Mode Selection bits 11 = Repeated Continuous mode 10 = Continuous mode 01 = Repeated One-Shot mode 00 = One-Shot mode
bit 1	<b>SIZE:</b> Data Size Selection bit 1 = Byte (8-bit) 0 = Word (16-bit)
bit 0	<b>CHEN:</b> DMA Channel Enable bit 1 = The corresponding channel is enabled 0 = The corresponding channel is disabled

- Note 1:** Only the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn.  
**Note 2:** DMASRCn, DMADSTn and DMACNTn are always reloaded in Repeated mode transfers (DMACHn<2> = 1), regardless of the state of the RELOAD bit.  
**Note 3:** The number of transfers executed while CHREQ is set depends on the configuration of TRMODE<1:0>.

# PIC24FJ256GA705 FAMILY

## 6.6.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time. To do this, it is necessary to erase the 8-row erase block containing the desired row. The general process is:

1. Read eight rows of program memory (1024 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 6-1):
  - a) Set the NVMOP<3:0> bits (NVMCON<3:0>) to '0011' to configure for block erase. Set the WREN (NVMCON<14>) bit.
  - b) Write the starting address of the block to be erased into the NVMADRU/NVMADR registers.
  - c) Write 55h to NVMKEY.
  - d) Write AAh to NVMKEY.
  - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Update the TBLPAG register to point to the programming latches on the device. Update the NVMADRU/NVMADR registers to point to the destination in the program memory.
5. Write the first 128 instructions from data RAM into the program memory buffers (see Table 6-1).
6. Write the program block to Flash memory:
  - a) Set the NVMOPx bits to '0010' to configure for row programming. Set the WREN bit.
  - b) Write 55h to NVMKEY.
  - c) Write AAh to NVMKEY.
  - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
7. Repeat Steps 4 through 6, using the next available 128 instructions from the block in data RAM, by incrementing the value in NVMADRU/NVMADR until all 1024 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as shown in Example 6-2.

**TABLE 6-1: EXAMPLE PAGE ERASE**

<b>Step 1:</b> Set the NVMCON register to erase a page.	
MOV	#0x4003, W0
MOV	W0, NVMCON
<b>Step 2:</b> Load the address of the page to be erased into the NVMADR register pair.	
MOV	#PAGE_ADDR_LO, W0
MOV	W0, NVMADR
MOV	#PAGE_ADDR_HI, W0
MOV	W0, NVMADRU
<b>Step 3:</b> Set the WR bit.	
MOV	#0x55, W0
MOV	W0, NVMKEY
MOV	#0xAA, W0
MOV	W0, NVMKEY
BSET	NVMCON, #WR
NOP	
NOP	
NOP	



# PIC24FJ256GA705 FAMILY

## 8.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 8.3.1 KEY RESOURCES

- “**Interrupts**” (DS70000600) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

## 8.4 Interrupt Control and Status Registers

PIC24FJ256GA705 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON4
- IFS0 through IFS7
- IEC0 through IEC7
- IPC0 through ICP29
- INTTREG

### 8.4.1 INTCON1-INTCON4

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources.

The INTCON2 register controls global interrupt generation, the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT).

The INTCON4 register contains the Software Generated Hard Trap bit (SGHT) and ECC Double-Bit Error (ECCDBE) trap.

### 8.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal, and is cleared via software.

### 8.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

### 8.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

### 8.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM<7:0>) and Interrupt Priority Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 8-2. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IPx bits in the first position of IPC0 (IPC0<2:0>).

### 8.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to “**CPU with Extended Data Space (EDS)**” (DS39732) in the “*dsPIC33/PIC24 Family Reference Manual*”.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with the IPL<2:0> bits, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 8-3 through Register 8-6 in the following pages.

# PIC24FJ256GA705 FAMILY

## REGISTER 11-38: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP13R5	RP13R4	RP13R3	RP13R2	RP13R1	RP13R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP12R5	RP12R4	RP12R3	RP12R2	RP12R1	RP12R0
bit 7						bit 0	

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13-8      **RP13R<5:0>:** RP13 Output Pin Mapping bits  
 Peripheral Output Number n is assigned to pin, RP13 (see Table 11-7 for peripheral function numbers).
- bit 7-6      **Unimplemented:** Read as '0'
- bit 5-0      **RP12R<5:0>:** RP12 Output Pin Mapping bits  
 Peripheral Output Number n is assigned to pin, RP12 (see Table 11-7 for peripheral function numbers).

## REGISTER 11-39: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP15R5	RP15R4	RP15R3	RP15R2	RP15R1	RP15R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP14R5	RP14R4	RP14R3	RP14R2	RP14R1	RP14R0
bit 7						bit 0	

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13-8      **RP15R<5:0>:** RP15 Output Pin Mapping bits  
 Peripheral Output Number n is assigned to pin, RP15 (see Table 11-7 for peripheral function numbers).
- bit 7-6      **Unimplemented:** Read as '0'
- bit 5-0      **RP14R<5:0>:** RP14 Output Pin Mapping bits  
 Peripheral Output Number n is assigned to pin, RP14 (see Table 11-7 for peripheral function numbers).

## 14.0 INPUT CAPTURE WITH DEDICATED TIMERS

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Input Capture with Dedicated Timer” (DS70000352), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ256GA705 family contain three independent input capture modules. Each of the modules offers a wide range of configuration and operating options for capturing external pulse events and generating interrupts.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in All modes by Cascading Two Adjacent modules
- Synchronous and Trigger modes of Output Compare Operation with up to 31 User-Selectable Sync/Trigger Sources Available
- A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to 6 Clock Sources Available for Each module, Driving a Separate Internal 16-Bit Counter

The module is controlled through two registers: ICxCON1 (Register 14-1) and ICxCON2 (Register 14-2). A general block diagram of the module is shown in Figure 14-1.

## 14.1 General Operating Modes

### 14.1.1 SYNCHRONOUS AND TRIGGER MODES

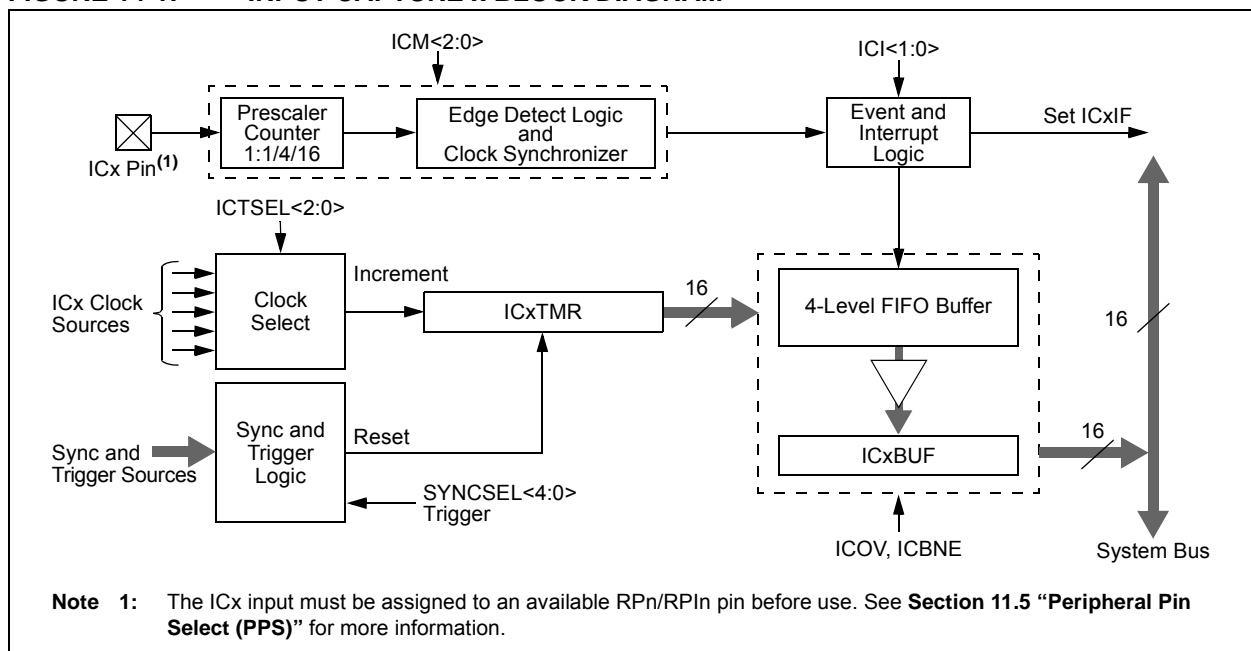
When the input capture module operates in a Free-Running mode, the internal 16-bit counter, ICxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow. Its period is synchronized to the selected external clock source. When a capture event occurs, the current 16-bit value of the internal counter is written to the FIFO buffer.

In Synchronous mode, the module begins capturing events on the ICx pin as soon as its selected clock source is enabled. Whenever an event occurs on the selected Sync source, the internal counter is reset. In Trigger mode, the module waits for a Sync event from another internal module to occur before allowing the internal counter to run.

Standard, free-running operation is selected by setting the SYNCSEL<4:0> bits (ICxCON2<4:0>) to ‘00000’ and clearing the ICTRIG bit (ICxCON2<7>). Synchronous and Trigger modes are selected any time the SYNCSELx bits are set to any value except ‘00000’. The ICTRIG bit selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the Sync/Trigger source.

When the SYNCSELx bits are set to ‘00000’ and ICTRIG is set, the module operates in Software Trigger mode. In this case, capture operations are started by manually setting the TRIGSTAT bit (ICxCON2<6>).

**FIGURE 14-1: INPUT CAPTURE x BLOCK DIAGRAM**



## 16.0 CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “**Capture/Compare/PWM/Timer (MCCP and SCCP)**” (DS33035), which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256GA705 family devices include several Capture/Compare/PWM/Timer base modules, which provide the functionality of three different peripherals of earlier PIC24F devices. The module can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

This family of devices features 4 instances of the MCCP module. MCCP1 provides up to six outputs and an extended range of power control features, whereas MCCP2-MCCP4 support two outputs.

The MCCPx modules can be operated only in one of the three major modes at any time. The other modes are not available unless the module is reconfigured for the new mode.

A conceptual block diagram for the module is shown in Figure 16-1. All three modules share a time base generator and a common Timer register pair (CCPxTMRH/L); other shared hardware components are added as a particular mode requires.

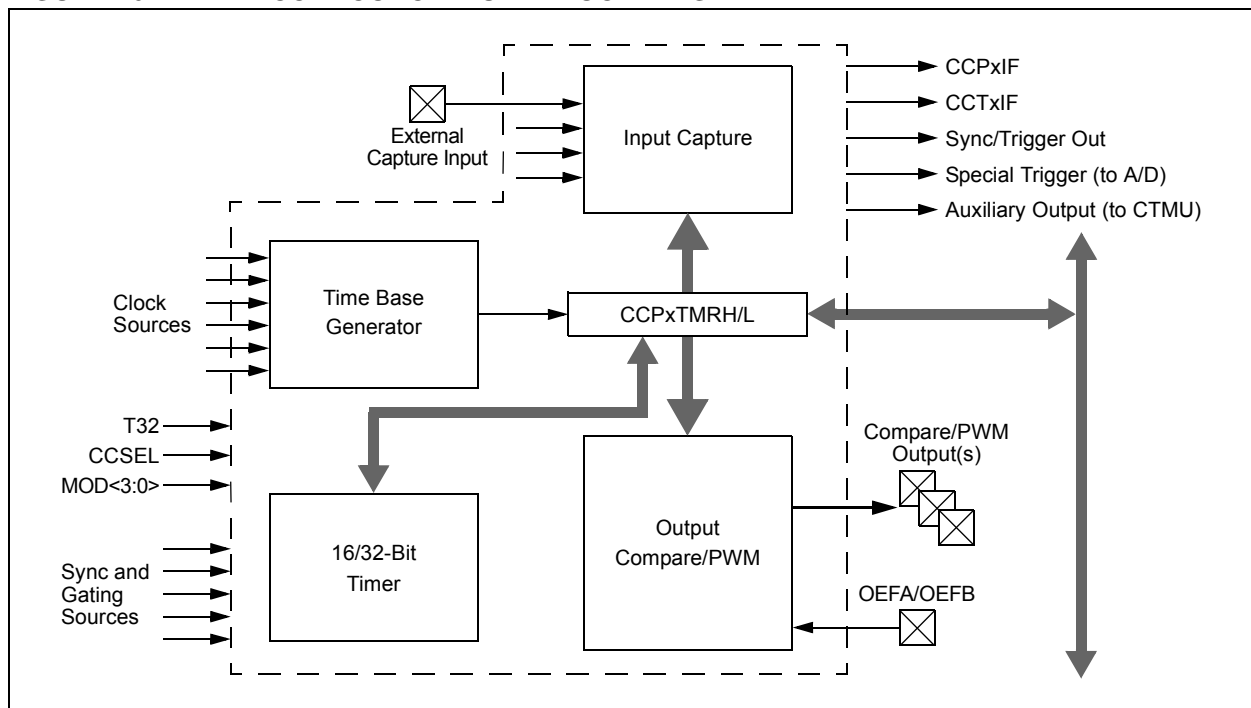
Each module has a total of 8 control and status registers:

- CCPxCON1L (Register 16-1)
- CCPxCON1H (Register 16-2)
- CCPxCON2L (Register 16-3)
- CCPxCON2H (Register 16-4)
- CCPxCON3L (Register 16-5)
- CCPxCON3H (Register 16-6)
- CCPxSTATL (Register 16-7)
- CCPxSTATH (Register 16-8)

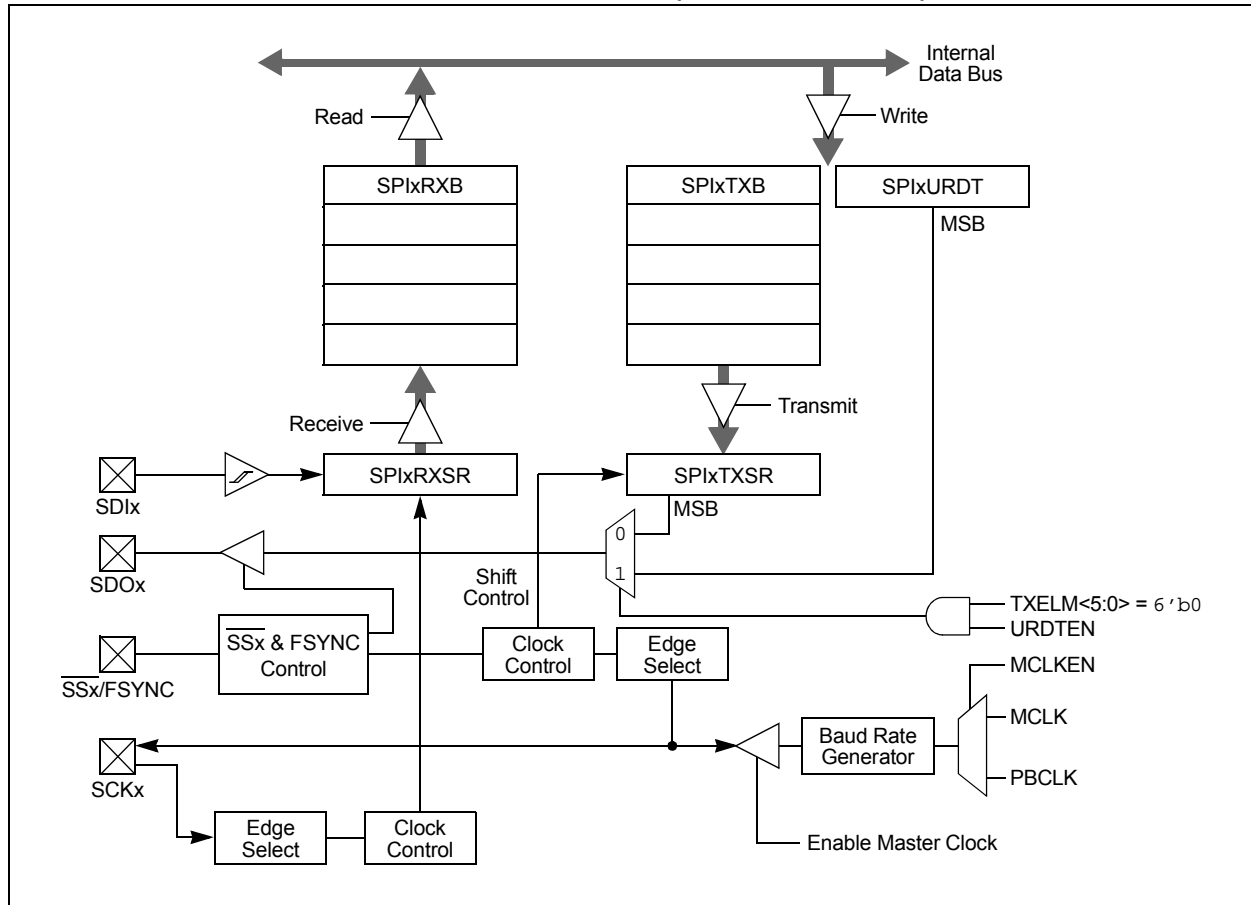
Each module also includes 8 buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMRH/CCPxTMRL (Timer High/Low Counters)
- CCPxPRH/CCPxPRL (Timer Period High/Low)
- CCPxRAH/CCPxRAL (Primary Output Compare Data Buffer)
- CCPxRBH/CCPxRBL (Secondary Output Compare Data Buffer)
- CCPxBUFH/CCPxBUFL (Input Capture High/Low Buffers)

**FIGURE 16-1: MCCPx CONCEPTUAL BLOCK DIAGRAM**



**FIGURE 17-1: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)**



## 17.3 Audio Mode Operation

To initialize the SPIx module for Audio mode, follow the steps to initialize it for Master/Slave mode, but also set the AUDEN bit (SPIxCON1H<15>). In Master+Audio mode:

- This mode enables the device to generate SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module generates LRC and SCKx continuously in all cases, regardless of the transmit data, while in Master mode.
- The SPIx module drives the leading edge of LRC and SCKx within 1 SCKx period, and the serial data shifts in and out continuously, even when the TX FIFO is empty.

In Slave+Audio mode:

- This mode enables the device to receive SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module drives zeros out of SDOx, but does not shift data out or in (SDIx) until the module receives the LRC (i.e., the edge that precedes the left channel).
- Once the module receives the leading edge of LRC, it starts receiving data if DISSDI (SPIxCON1L<4>) = 0 and the serial data shifts out continuously, even when the TX FIFO is empty.

# PIC24FJ256GA705 FAMILY

## REGISTER 24-11: AD1CTMENH: A/D CTMU ENABLE REGISTER (HIGH WORD)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	CTMEN<30:28>			—	—	CTMEN<25:24>	
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<23:16> <sup>(1)</sup>							
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15      **Unimplemented:** Read as '0'

bit 14-12      **CTMEN<30:28>:** CTMU Enabled During Conversion bits  
1 = CTMU is enabled and connected to the selected channel during conversion  
0 = CTMU is not connected to this channel

bit 11-10      **Unimplemented:** Read as '0'

bit 9-0      **CTMEN<25:16>:** CTMU Enabled During Conversion bits<sup>(1)</sup>  
1 = CTMU is enabled and connected to the selected channel during conversion  
0 = CTMU is not connected to this channel

**Note 1:** CTMEN<23:16> bits are not available on 64-pin parts.

## REGISTER 24-12: AD1CTMENL: A/D CTMU ENABLE REGISTER (LOW WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<15:8>							
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<7:0>							
bit 7							bit 0

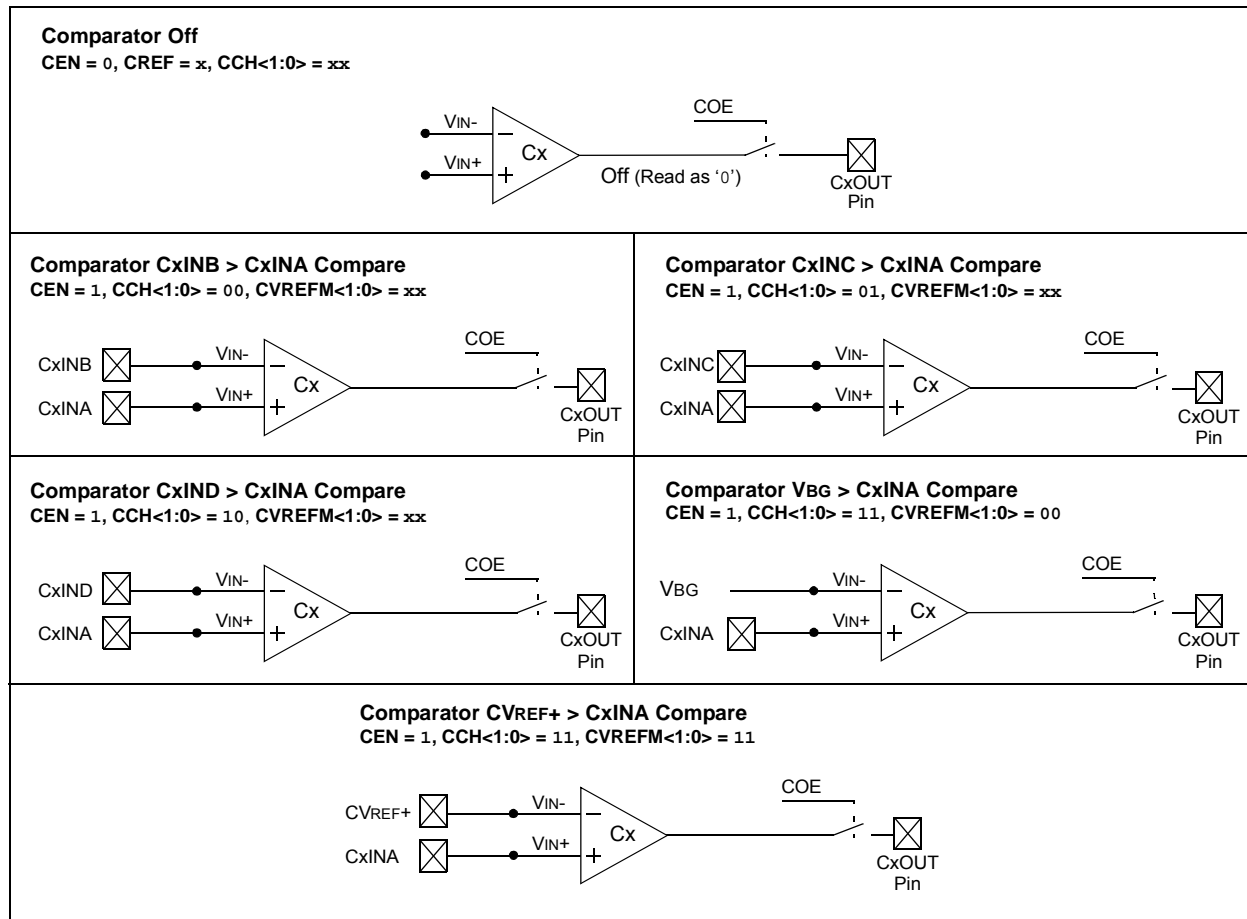
### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

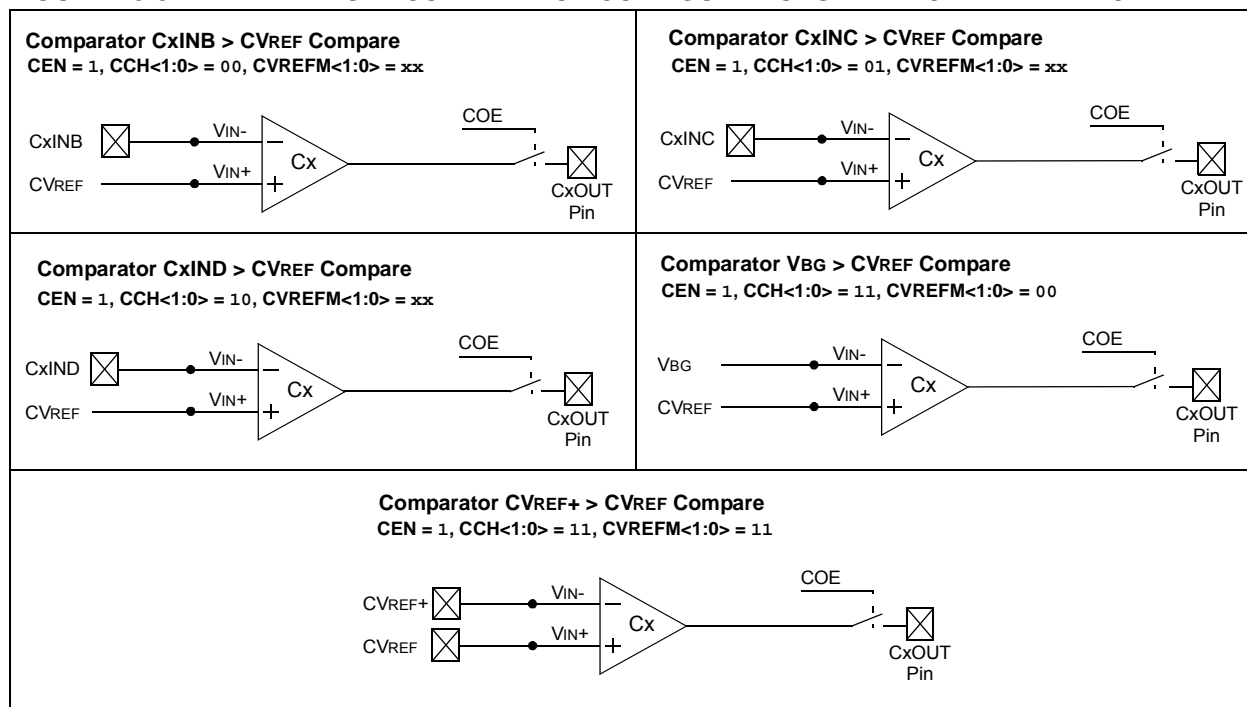
bit 15-0      **CTMEN<15:0>:** CTMU Enabled During Conversion bits  
1 = CTMU is enabled and connected to the selected channel during conversion  
0 = CTMU is not connected to this channel

# PIC24FJ256GA705 FAMILY

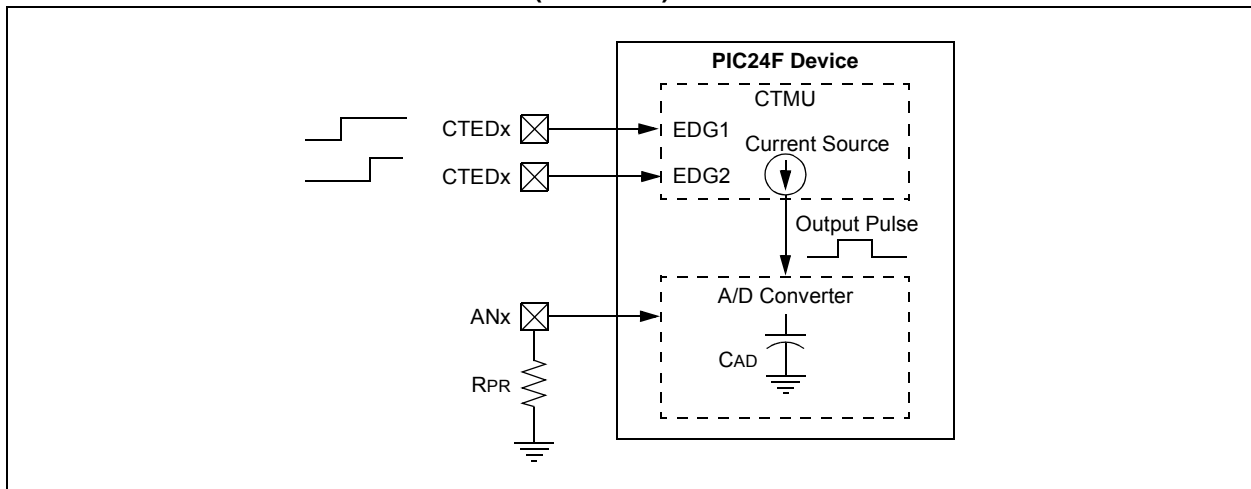
**FIGURE 25-2: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 0**



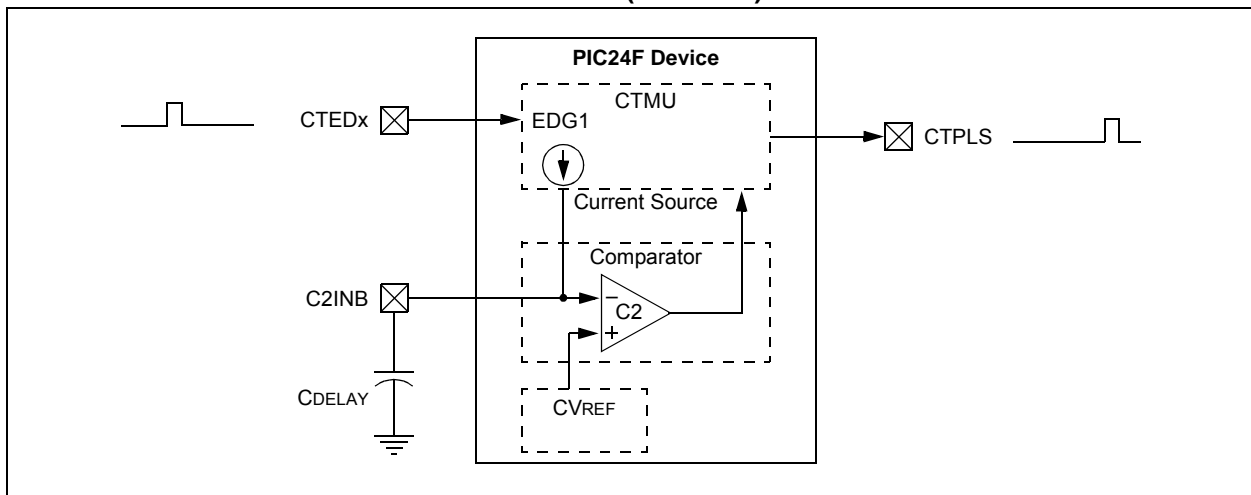
**FIGURE 25-3: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 0**



**FIGURE 27-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT (TGEN = 0)**

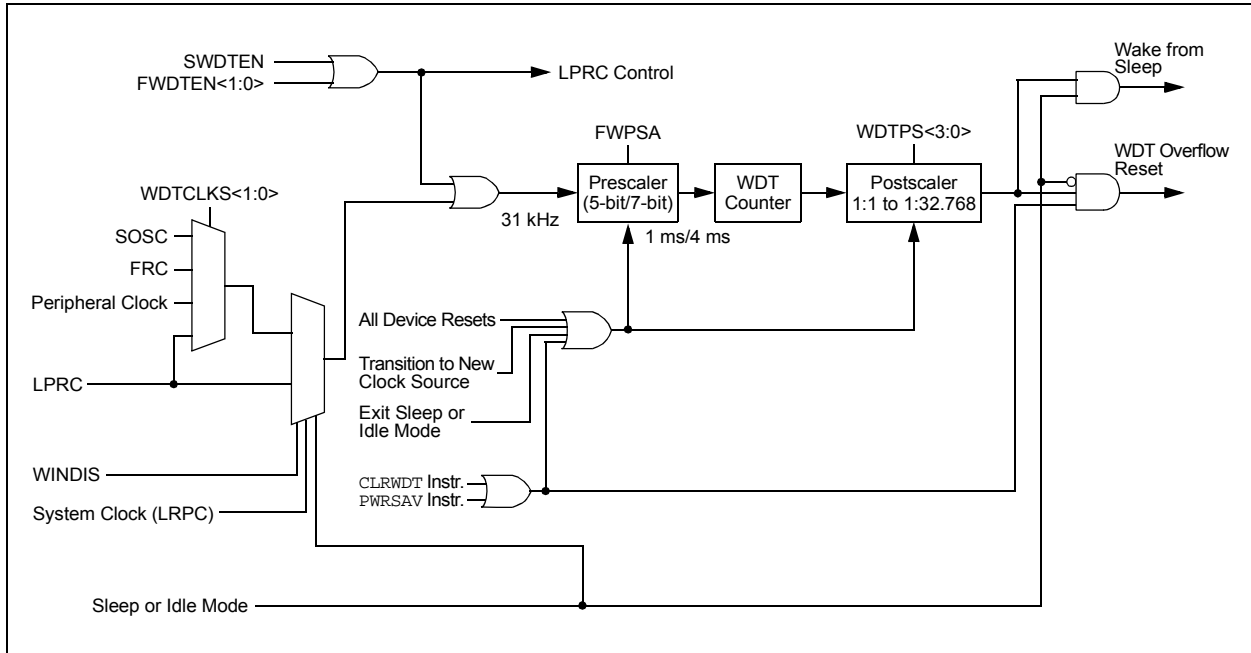


**FIGURE 27-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION (TGEN = 1)**





**FIGURE 29-2: WDT BLOCK DIAGRAM**



## 30.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 30.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 30.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 30.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

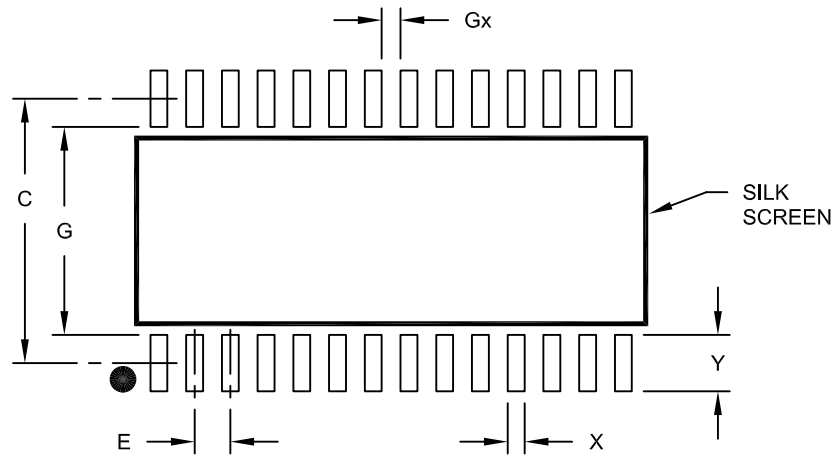
## 30.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

# PIC24FJ256GA705 FAMILY

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

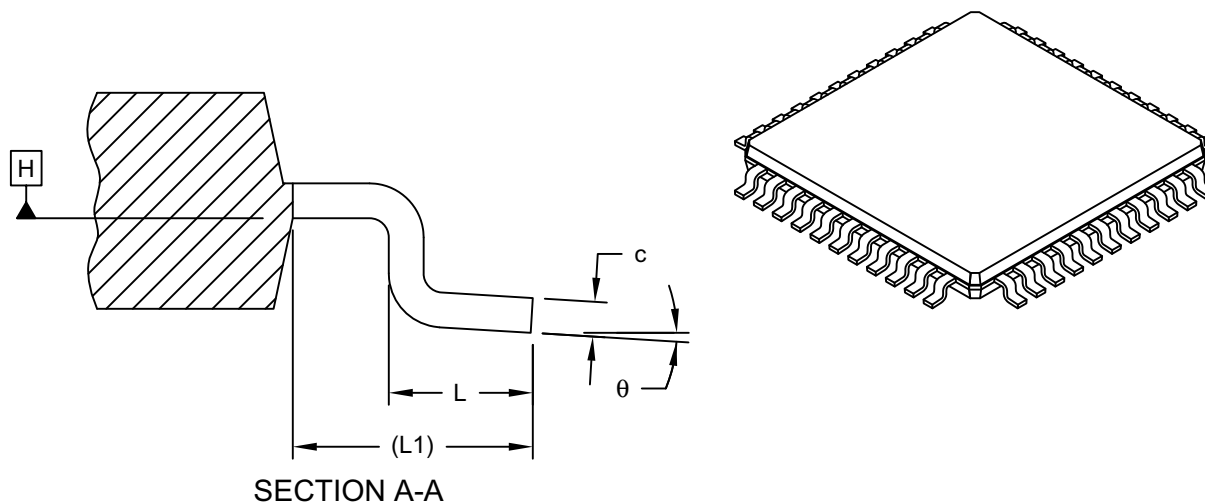
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

# PIC24FJ256GA705 FAMILY

## 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	3.5°	7°

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC	24	FJ	256	GA	7	05	T	-	I	/	PT	-	XXX
Microchip Trademark														
Architecture														
Flash Memory Family														
Program Memory Size (Kbytes)														
Product Group														
Pin Count														
Tape and Reel Flag (if applicable)														
Temperature Range														
Package														
Pattern														

Architecture	24	= 16-Bit Modified Harvard without DSP
Flash Memory Family	FJ	= Flash Program Memory
Pin Count	02	= 28-pin (QFN, UQFN, SOIC, SSOP, SPDIP)
	04	= 44-pin (TQFP)
	05	= 48-pin (UQFN, TQFP)
Temperature Range	I	= -40°C to +85°C (Industrial)
Package	ML	= 28-Lead (6x6 mm) QFN (Plastic Quad Flat)
	M6	= 28-Lead (4x4x0.6 mm) UQFN (Ultra Thin Quad Flatpack)
	SO	= 28-Lead (7.50 mm) SOIC (Plastic Small Outline)
	SS	= 28-Lead (5.30 mm) SSOP (Plastic Shrink Small Outline)
	SP	= 28-Lead (300 mil) SPDIP (Skinny Plastic Dual In-Line)
	PT	= 44-lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	5E	= 48-Lead (7x7 mm) UQFN (Plastic Quad Flat)
	PT	= 48-Lead (7x7x1 mm) TQFP (Thin Quad Flatpack)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	
	ES	= Engineering Sample

### Examples:

- PIC24FJ256GA705-I/PT:  
PIC24F General Purpose Device, 48-Pin, Industrial Temp., TQFP Package.
- PIC24FJ256GA702-I/ML:  
PIC24F General Purpose Device, 28-Pin, Industrial Temp., QFN Package