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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga704t-i-pt

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FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLES



TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	BOA+04h	Oscillator Failure
1	000006h	BOA+06h	Address Error
2	000008h	BOA+08h	General Hardware Error
3	00000Ah	BOA+0Ah	Stack Error
4	00000Ch	BOA+0Ch	Math Error
5	00000Eh	BOA+0Eh	Reserved
6	000010h	BOA+10h	General Software Error
7	000012h	BOA+12h	Reserved

Legend: BOA = Base Offset Address for AIVT segment, which is the starting address of the last page of the Boot Segment.

TABLE 10-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	—	—	T3MD	T2MD	T1MD		—	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD		—	ADCMD	0000
PMD2	_	_	_	—		IC3MD	IC2MD	IC1MD	_		_	_	_	OC3MD	OC2MD	OC1MD	0000
PMD3	_	_	_	—		CMPMD	RTCCMD	PMPMD	CRCMD		_	_	_	_	I2C2MD	-	0000
PMD4	_	_	_	—			_	_	_		_	_	REFOMD	CTMUMD	LVDMD		0000
PMD5	_	_	_	—			_	_	_		_	_	CCP4MD	CCP3MD	CCP2MD	CCP1MD	0000
PMD6	_	_	_	—			_	_	_		_	_	_	_	_	SPI3MD	0000
PMD7	_	_	_	_	_	_	_	_	_	_	DMA1MD	DMA0MD	_	_	_	_	0000
PMD8	_			—			—		—		_		CLC2MD	CLC1MD			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

11.4 I/O Port Control Registers

– bit 8
bit 8
W-0
PTTL
bit 0
1F

REGISTER 11-1: PADCON: PORT CONFIGURATION REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	IOCON: Interrupt-on-Change Enable bit
	 1 = Interrupt-on-Change functionality is enabled 0 = Interrupt-on-Change functionality is disabled
bit 14-1	Unimplemented: Read as '0'
bit 0	PMPTTL: PMP Port Type bit
	1 = TTL levels on PMP port pins
	0 = Schmitt Triggers on PMP port pins

REGISTER 11-2: IOCSTAT: INTERRUPT-ON-CHANGE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0
—	—	—	—	—	IOCPCF	IOCPBF	IOCPAF
bit 7							bit 0

Legend:	HS = Hardware Settable bit	Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-3	Unimplemented: Read as '0'
bit 2	IOCPCF: Interrupt-on-Change PORTC Flag bit
	1 = A change was detected on an IOC-enabled pin on PORTC0 = No change was detected or the user has cleared all detected changes
bit 1	IOCPBF: Interrupt-on-Change PORTB Flag bit
	 1 = A change was detected on an IOC-enabled pin on PORTB 0 = No change was detected or the user has cleared all detected changes
bit 0	IOCPAF: Interrupt-on-Change PORTA Flag bit
	 1 = A change was detected on an IOC-enabled pin on PORTA 0 = No change was detected, or the user has cleared all detected change

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0
bit 15							bit 8
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0
bit 7							bit 0
Legend:							
B = Boodoblo bit $W = Writeblo bit$			hit	II – Unimplor	nontod hit road	1 22 '0'	

REGISTER 11-17: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	ICM2R<5:0>: Input Capture Mode 2 bits

bit 7-6 Unimplemented: Read as '0'

bit 5-0 ICM1R<5:0>: Input Capture Mode 1 bits

REGISTER 11-18: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ICM4R5	ICM4R4	ICM4R3	ICM4R2	ICM4R1	ICM4R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	ICM3R5	ICM3R4	ICM3R3	ICM3R2	ICM3R1	ICM3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 ICM4R<5:0>: Input Capture Mode 4 bits

bit 7-6 Unimplemented: Read as '0'

bit 5-0 ICM3R<5:0>: Input Capture Mode 3 bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC			
UTXISEL	1 UTXINV ⁽¹⁾	UTXISEL0	URXEN	UTXBRK	UTXEN ⁽²⁾	UTXBF	TRMT			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC			
URXISEL	1 URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA			
bit 7							bit 0			
Legend:		C = Clearable	bit	HSC = Hardw	are Settable/C	learable bit				
R = Reada	ble bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'				
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own			
HS = Hardv	vare Settable bit	HC = Hardwa	re Clearable b	it						
bit 15,13	UTXISEL<1:0 11 = Reserve 10 = Interrup transmit 01 = Interrup	D>: UARTx Tran ed; do not use t when a charao buffer become t when the las	nsmission Inte cter is transferi s empty st character is	rrupt Mode Sele red to the Transi s shifted out o	ection bits mit Shift Regist f the Transmit	ter (TSR), and a	as a result, the r; all transmit			
bit 14	operatio 00 = Interrup one cha UTXINV: UAF IREN = 0: 1 = UXTX Idle	ns are complet t when a charac racter open in t RTX IrDA [®] Enco	ed ster is transferr he transmit bu oder Transmit	ed to the Transn ıffer) Polarity Inversic	nit Shift Registe on bit ⁽¹⁾	er (this implies t	here is at least			
	0 = UxTX Idle <u>IREN = 1:</u> 1 = UxTX Idle 0 = UxTX Idle	e state is '1' e state is '1' e state is '0'								
bit 12	URXEN: UAF	RTx Receive En	able bit							
	1 = Receive is	s enabled, UxR	X pin is contro	olled by UARTx						
	0 = Receive i	s disabled, UxF	RX pin is contro	olled by the port	t					
bit 11	UTXBRK: UA	ARTx Transmit I	Break bit							
	1 = Sends Sy cleared b 0 = Sync Bre	ync Break on ne by hardware up eak transmission	ext transmissic on completion n is disabled o	on – Start bit, foll or completed	lowed by twelv	e '0' bits, follow	ed by Stop bit;			
bit 10	UTXEN: UAR	RTx Transmit Er	nable bit ⁽²⁾							
	 UTXEN: UARTx Transmit Enable bit⁽²⁾ 1 = Transmit is enabled, UxTX pin is controlled by UARTx 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the port 									
bit 9	UTXBF: UAR	Tx Transmit Bu	Iffer Full Statu	s bit (read-only)						
	1 = Transmit 0 = Transmit	buffer is full buffer is not full	, at least one	more character	can be written					
bit 8	TRMT: Transi	mit Shift Regist	er Empty bit (r	ead-only)						
	1 = Transmit 0 = Transmit	Shift Register is Shift Register is	empty and tra not empty, a	ansmit buffer is e transmission is	empty (the last in progress or	transmission ha	as completed)			
Note 1:	The value of this (IREN = 1).	bit only affects	the transmit pr	operties of the i	module when t	he IrDA [®] encoc	ler is enabled			

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

2: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see Section 11.5 "Peripheral Pin Select (PPS)".

20.1 Memory Addressable in Different Modes

The memory space addressable by the device depends on the address/data multiplexing selection; it varies from 1K to 2 MB. Refer to Table 20-1 for different Memory-Addressable modes.

20.2 PMDOUT1 and PMDOUT2 Registers

The EPMP Data Output 1 and Data Output 2 registers are used only in Slave mode. These registers act as a buffer for outgoing data.

20.3 PMDIN1 and PMDIN2 Registers

The EPMP Data Input 1 and Data Input 2 registers are used in Slave modes to buffer incoming data. These registers hold data that is asynchronously clocked in. In Master mode, PMDIN1 is the holding register for incoming data.

Data Port Size	PMA<9:8>	PMA<7:0>	PMD<7:4>	PMD<3:0>	Accessible Memory						
Demultiplexed Address (ADRMUX<1:0> = 00)											
8-Bit (PTSZ<1:0> = 00)	Addr<9:8>	Addr<7:0>	Da	ata	1K						
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	Addr<7:0>	—	Data	1K						
	1 Ad	dress Phase (AD	DRMUX<1:0> = 0	1)							
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr<7	:0> Data	1K						
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	PMALL	Addr<7:4>	Addr<3:0>	1K						
			—	Data (1)	7						
	2 Add	Iress Phases (Al	DRMUX<1:0> = 1	L0)	-						
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr	<7:0>	64K						
		PMALH	Addr<	:15:8>							
		—	Da	ata							
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	PMALL	Addr<3:0>		1K						
		PMALH	Addr<7:4>								
		—	Da	ata	1						
	3 Add	Iress Phases (Al	DRMUX<1:0> = 1	1)	-						
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr	<7:0>	2 Mbytes						
		PMALH	Addr<	:15:8>	7						
		PMALU	Addr<22:16>								
		_	Da	ata							
4-Bit (PTSZ<1:0> = 01)	Addr<13:12>	PMALL	Addr	<3:0>	16K						
		PMALH	Addr	<7:4>							
		PMALU	Addr<	<11:8>]						
		—	Da	ata	1						

TABLE 20-1: EPMP FEATURE DIFFERENCES BY DEVICE PIN COUNT

REGISTER 20-8: PMSTAT: EPMP STATUS REGISTER (SLAVE MODE ONLY)

R-0, HSC	R/W-0, HS	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IBF	IBOV	—	—	IB3F ⁽¹⁾	IB2F ⁽¹⁾	IB1F ⁽¹⁾	IB0F ⁽¹⁾
bit 15							bit 8

R-1, HSC	R/W-0, HS	U-0	U-0	R-1, HSC	R-1, HSC	R-1, HSC	R-1, HSC
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend: HS = Hardware Settable bit		HSC = Hardware Settable/Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15	IBF: Input Buffer Full Status bit
	1 = All writable Input Buffer registers are full
	0 = Some or all of the writable Input Buffer registers are empty
bit 14	IBOV: Input Buffer Overflow Status bit
	1 = A write attempt to a full Input register occurred (must be cleared in software)0 = No overflow occurred
bit 13-12	Unimplemented: Read as '0'
bit 11-8	IB3F:IB0F: Input Buffer x Status Full bits ⁽¹⁾
	1 = Input buffer contains unread data (reading the buffer will clear this bit)
	0 = Input buffer does not contain unread data
bit 7	OBE: Output Buffer Empty Status bit
	1 = All readable Output Buffer registers are empty
	0 = Some or all of the readable Output Buffer registers are full
bit 6	OBUF: Output Buffer Underflow Status bit
	1 = A read occurred from an empty Output Buffer register (must be cleared in software)0 = No underflow occurred
bit 5-4	Unimplemented: Read as '0'
bit 3-0	OB3E:OB0E: Output Buffer x Status Empty bits
	1 = Output Buffer x is empty (writing data to the buffer will clear this bit)
	 0 = Output Buffer x contains untransmitted data

Note 1: Even though an individual bit represents the byte in the buffer, the bits corresponding to the word (Byte 0 and 1 or Byte 2 and 3) get cleared, even on byte reading.

22.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the "dsPIC33/PIC24 Family Reference Manual", "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS30009729), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM. The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 22-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 22-2.

FIGURE 22-1: CRC BLOCK DIAGRAM



FIGURE 22-2: CRC SHIFT ENGINE DETAIL



PIC24FJ256GA705 FAMILY



REGISTER 23-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 MODE<2:0>: CLCx Mode bits

- 111 = Cell is a 1-input transparent latch with S and R
- 110 = Cell is a JK flip-flop with R
- 101 = Cell is a 2-input D flip-flop with R
- 100 = Cell is a 1-input D flip-flop with S and R
- 011 = Cell is an SR latch
- 010 = Cell is a 4-input AND
- 001 = Cell is an OR-XOR
- 000 = Cell is an AND-OR

REGISTER 23-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

l egend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0'
bit 3	G4POL: Gate 4 Polarity Control bit
	1 = The output of Channel 4 logic is inverted when applied to the logic cell0 = The output of Channel 4 logic is not inverted
bit 2	G3POL: Gate 3 Polarity Control bit
	1 = The output of Channel 3 logic is inverted when applied to the logic cell0 = The output of Channel 3 logic is not inverted
bit 1	G2POL: Gate 2 Polarity Control bit
	 1 = The output of Channel 2 logic is inverted when applied to the logic cell 0 = The output of Channel 2 logic is not inverted
bit 0	G1POL: Gate 1 Polarity Control bit
	1 = The output of Channel 1 logic is inverted when applied to the logic cell0 = The output of Channel 1 logic is not inverted

FIGURE 24-2: EXAMPLE OF BUFFER ADDRESS GENERATION IN PIA MODE (4-WORD BUFFERS PER CHANNEL)



R/W-0	R/W-0	R/W-0	r-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	_	BUFREGEN	CSCNA	_	_
bit 15		11					bit 8
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0
Legend:		r = Reserved b	it				
R = Readable	e bit	W = Writable b	it	U = Unimpleme	ented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clear	red	x = Bit is unkn	own
bit 15-14	PVCFG<1:0> 1x = Unimple 01 = Externa 00 = AVDD	•: A/D Converter emented, do not I VREF+	Positive Vol use	tage Reference C	Configuration I	bits	
bit 13	NVCFG0: A/I 1 = External V 0 = AVss	⊃ Converter Neg √REF-	ative Voltage	e Reference Conf	iguration bit		
bit 12	Reserved: M	aintain as '0'					
bit 11	BUFREGEN: 1 = Conversio 0 = A/D resul	A/D Buffer Reg on result is loade t buffer is treated	ister Enable ed into the bu d as a FIFO	bit uffer location dete	rmined by the	e converted cha	nnel
bit 10	CSCNA: Sca 1 = Scans inp 0 = Does not	n Input Selectior outs scan inputs	ns for CH0+	During Sample A	bit		
bit 9-8	Unimplemen	ted: Read as '0	,				
bit 7	BUFS: Buffer	Fill Status bit					
	When DMAE 1 = A/D is cu [buffer st 0 = A/D is cu User sho When DMAE 1 = A/D is cu ADC1BU 0 = A/D is cu	N = 1 and DMAE irrently filling the art + (buffer size art + (buffer size irrently filling the uld access data I N = 0: irrently filling AD IF0-ADC1BUF12 irrently filling AD	$\frac{3M = 1}{destination}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$ $\frac{(-1)}{(-1)}$	buffer from [buffer should access da buffer from [buffe [buffer start + (buff DC1BUF25, user C1BUF12, user s	r start + (buffe ta located froi r start] to [buf fer size/2)] to [should access	er size/2)] to m [buffer start] t fer start + (buffe buffer start + (bu s data in data in	o er size/2) – 1]. uffer size – 1)].

REGISTER 24-2: AD1CON2: A/D CONTROL REGISTER 2

REGISTER 24-4: AD1CON4: A/D CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—		DMABL<2:0>(1)
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	1 as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-3 Unimplemented: Read as '0'

bit 2-0

- DMABL<2:0>: DMA Buffer Size Select bits⁽¹⁾
 - 111 = Allocates 128 words of buffer to each analog input
 - 110 = Allocates 64 words of buffer to each analog input
 - 101 = Allocates 32 words of buffer to each analog input
 - 100 = Allocates 16 words of buffer to each analog input
 - 011 = Allocates 8 words of buffer to each analog input
 - 010 = Allocates 4 words of buffer to each analog input
 - 001 = Allocates 2 words of buffer to each analog input
 - 000 = Allocates 1 word of buffer to each analog input
- **Note 1:** The DMABL<2:0> bits are only used when AD1CON1<11> = 1 and AD1CON1<12> = 0; otherwise, their value is ignored.

NOTES:

NOTES:

x = Bit is unknown

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16
U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
_	—	—			BSLIM<12:8>		
bit 15							bit 8
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
			BSLI	M<7:0>			
bit 7							bit 0
Legend:		PO = Program	n Once bit				
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	

REGISTER 29-2: FBSLIM CONFIGURATION REGISTER

'1' = Bit is set

bit 23-13 Unimplemented: Read as '1'

-n = Value at POR

bit 12-0 **BSLIM<12:0>:** Active Boot Segment Code Flash Page Address Limit (Inverted) bits This bit field contains the last active Boot Segment Page + 1 (i.e., first page address of GS). The value is stored as an inverted page address, such that programming additional '0's can only increase the size of BS. If BSLIM<12:0> is set to all '1's (unprogrammed default), the active Boot Segment size is zero.

'0' = Bit is cleared

REGISTER 29-9: FDEVOPT1 CONFIGURATION REGIST
--

	200. 102			REGIOTER				
U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	
	_	—	_	_	—		_	
bit 23							bit 16	
U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	
	—	—	—	—	—	—	—	
bit 15							bit 8	
U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1	
_			ALTI2C1	SOSCHP	TMPRPIN	ALTCMPI	_	
bit 7							bit 0	
Legend:		PO = Prograr	n Once bit					
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own	
bit 23-5	Unimpleme	nted: Read as '	1'					
bit 4	ALTI2C1: AI	ternate I2C1 bit						
	1 = SDA1 ar	nd SCL1 on RB9	and RB8					
	0 = ASDA1 a	and ASCL1 on F	RB5 and RB6					
bit 3	SOSCHP: S	OSC High-Powe	er Enable bit (v	alid only when	SOSCSEL = 1)		
	1 = SOSC H	ligh-Power mode	e is enabled					
	0 = SOSC L informat	ow-Power mode tion)	e is enabled (se	ee Section 9.7.	3 "Low-Powei	r SOSC Operat	ion" for more	
bit 2	TMPRPIN: 7	amper Pin Enat	ole bit					
	1 = TMPRN	pin function is d	isabled (RB9)					
	0 = TMPRN	pin function is e	nabled					

- bit 1 ALTCMPI: Alternate Comparator Input Enable bit 1 = C1INC, C2INC and C3INC are on their standard pin locations 0 = C1INC, C2INC and C3INC are on RB9⁽¹⁾
- bit 0 Unimplemented: Read as '1'
- **Note 1:** RB9 is used for multiple functions, but only one use case is allowable.





48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			4.70
Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.80
Corner Anchor Pad Width (X4)	X3			0.90
Corner Anchor Pad Length (X4)	Y3			0.90
Pad Corner Radius (X 20)	R			0.10
Contact Pad to Center Pad (X48)	G1	0.25		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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