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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 64KB (22K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 14x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga705t-i-pt |

**TABLE 1-3: PIC24FJ256GA705 FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Pin Function | Pin Number/Grid Locator | | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|---|
| | 28-Pin SOIC, SSOP, SPDIP | 28-Pin QFN, UQFN | 44-Pin TQFP | 48-Pin QFN/TQFP | | | |
| RP0 | 4 | 1 | 21 | 23 | I/O | DIG/ST | Remappable Peripherals (input or output) |
| RP1 | 5 | 2 | 22 | 24 | I/O | DIG/ST | |
| RP2 | 6 | 3 | 23 | 25 | I/O | DIG/ST | |
| RP3 | 7 | 4 | 24 | 26 | I/O | DIG/ST | |
| RP4 | 11 | 8 | 33 | 36 | I/O | DIG/ST | |
| RP5 | 14 | 11 | 41 | 45 | I/O | DIG/ST | |
| RP6 | 15 | 12 | 42 | 46 | I/O | DIG/ST | |
| RP7 | 16 | 13 | 43 | 47 | I/O | DIG/ST | |
| RP8 | 17 | 14 | 44 | 48 | I/O | DIG/ST | |
| RP9 | 18 | 15 | 1 | 1 | I/O | DIG/ST | |
| RP10 | 21 | 18 | 8 | 9 | I/O | DIG/ST | |
| RP11 | 22 | 19 | 9 | 10 | I/O | DIG/ST | |
| RP12 | 23 | 20 | 10 | 11 | I/O | DIG/ST | |
| RP13 | 24 | 21 | 11 | 12 | I/O | DIG/ST | |
| RP14 | 25 | 22 | 14 | 15 | I/O | DIG/ST | |
| RP15 | 26 | 23 | 15 | 16 | I/O | DIG/ST | |
| RP16 | — | — | 25 | 27 | I/O | DIG/ST | |
| RP17 | — | — | 26 | 28 | I/O | DIG/ST | |
| RP18 | — | — | 27 | 29 | I/O | DIG/ST | |
| RP19 | — | — | 36 | 39 | I/O | DIG/ST | |
| RP20 | — | — | 37 | 40 | I/O | DIG/ST | |
| RP21 | — | — | 38 | 41 | I/O | DIG/ST | |
| RP22 | — | — | 2 | 2 | I/O | DIG/ST | |
| RP23 | — | — | 3 | 3 | I/O | DIG/ST | |
| RP24 | — | — | 4 | 4 | I/O | DIG/ST | |
| RP25 | — | — | 5 | 5 | I/O | DIG/ST | |
| RP26 | 2 | 27 | 19 | 21 | I/O | DIG/ST | |
| RP27 | 3 | 28 | 20 | 22 | I/O | DIG/ST | |
| RP28 | — | — | 12 | 13 | I/O | DIG/ST | |
| RPI29 | — | — | — | 8 | I | DIG/ST | Remappable Peripherals (input only) |
| RPI30 | — | — | — | 20 | I | DIG/ST | |
| RPI31 | — | — | — | 32 | I | DIG/ST | |
| RPI32 | — | — | — | 44 | I | DIG/ST | |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$/SMBus input buffer
XCVR = Dedicated Transceiver

### 2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

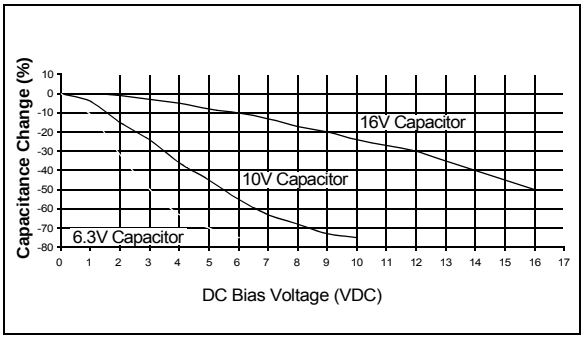
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

**FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS**




When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at a minimum of 16V for the 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

## 2.5 ICSP Pins

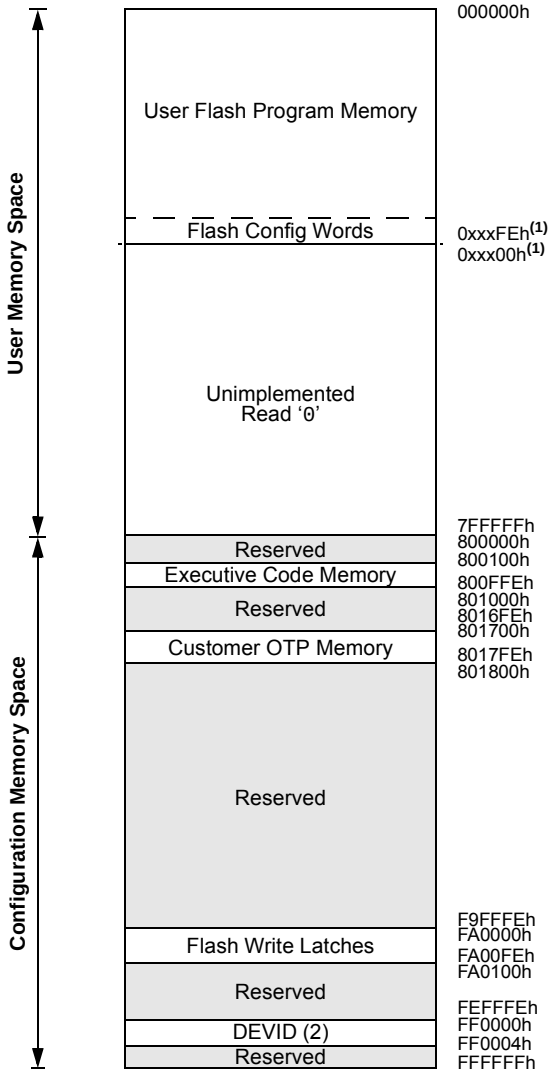
The PGCx and PGDx pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Voltage Input High ($V_{IH}$) and Voltage Input Low ($V_{IL}$) requirements.

For device emulation, ensure that the "Communication Channel Select" pins (i.e., PGCx/PGDx) programmed into the device match the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 30.0 "Development Support"**.

**FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FJ256GA705 DEVICES**




**Legend:** Memory areas are not shown to scale.

**Note 1:** Exact boundary addresses are determined by the size of the implemented program memory (Table 4-1).

**TABLE 4-1: PROGRAM MEMORY SIZES AND BOUNDARIES(2)**

| Device | Program Memory Upper Boundary (Instruction Words) | Write Blocks(1) | Erase Blocks(1) |
|---|---|---|---|
| PIC24FJ256GA70X | 02AFFEh (88,064 x 24) | 1376 | 172 |
| PIC24FJ128GA70X | 015FFEh (45,056 x 24) | 704 | 88 |
| PIC24FJ64GA70X | 00AFFEh (22,528 x 24) | 352 | 44 |

**Note 1:** 1 Write Block = 128 Instruction Words; 1 Erase Block (Page) = 1024 Instruction Words.

**2:** To maintain integer page sizes, the memory sizes are not exactly half of each other.

**TABLE 8-2: INTERRUPT VECTOR DETAILS**

| Interrupt Source | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|
| | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | |
| INT0 – External Interrupt 0 | 0 | 000014h | IFS0<0> | IEC0<0> | INT0Interrupt |
| IC1 – Input Capture 1 | 1 | 000016h | IFS0<1> | IEC0<1> | IC1Interrupt |
| OC1 – Output Compare 1 | 2 | 000018h | IFS0<2> | IEC0<2> | OC1Interrupt |
| T1 – Timer1 | 3 | 00001Ah | IFS0<3> | IEC0<3> | T1Interrupt |
| DMA0 – Direct Memory Access 0 | 4 | 00001Ch | IFS0<4> | IEC0<4> | DMA0Interrupt |
| IC2 – Input Capture 2 | 5 | 00001Eh | IFS0<5> | IEC0<5> | IC2Interrupt |
| OC2 – Output Compare 2 | 6 | 000020h | IFS0<6> | IEC0<6> | OC2Interrupt |
| T2 – Timer2 | 7 | 000022h | IFS0<7> | IEC0<7> | T2Interrupt |
| T3 – Timer3 | 8 | 000024h | IFS0<8> | IEC0<8> | T3Interrupt |
| SPI1 – SPI1 General | 9 | 000026h | IFS0<9> | IEC0<9> | SPI1Interrupt |
| SPI1TX – SPI1 Transfer Done | 10 | 000028h | IFS0<10> | IEC0<10> | SPI1TXInterrupt |
| U1RX – UART1 Receiver | 11 | 00002Ah | IFS0<11> | IEC0<11> | U1RXInterrupt |
| U1TX – UART1 Transmitter | 12 | 00002Ch | IFS0<12> | IEC0<12> | U1TXInterrupt |
| ADC1 – A/D Converter 1 | 13 | 00002Eh | IFS0<13> | IEC0<13> | ADC1Interrupt |
| DMA1 – Direct Memory Access 1 | 14 | 000030h | IFS0<14> | IEC0<14> | DMA1Interrupt |
| NVM – NVM Program/Erase Complete | 15 | 000032h | IFS0<15> | IEC0<15> | NVMInterrupt |
| SI2C1 – I2C1 Slave Events | 16 | 000034h | IFS1<0> | IEC1<0> | SI2C1Interrupt |
| MI2C1 – I2C1 Master Events | 17 | 000036h | IFS1<1> | IEC1<1> | MI2C1Interrupt |
| Comp – Comparator | 18 | 000038h | IFS1<2> | IEC1<2> | CompInterrupt |
| IOC – Interrupt-on-Change Interrupt | 19 | 00003Ah | IFS1<3> | IEC1<3> | IOCInterrupt |
| INT1 – External Interrupt 1 | 20 | 00003Ch | IFS1<4> | IEC1<4> | INT1Interrupt |
| — | 21 | — | — | — | — |
| — | 22 | — | — | — | — |
| — | 23 | — | — | — | — |
| DMA2 – Direct Memory Access 2 | 24 | 000044h | IFS1<8> | IEC1<8> | DMA2Interrupt |
| OC3 – Output Compare 3 | 25 | 000046h | IFS1<9> | IEC1<9> | OC3Interrupt |
| — | 26 | — | — | — | — |
| — | 27 | — | — | — | — |
| — | 28 | — | — | — | — |
| INT2 – External Interrupt 2 | 29 | 00004Eh | IFS1<13> | IEC1<13> | INT2Interrupt |
| U2RX – UART2 Receiver | 30 | 000050h | IFS1<14> | IEC1<14> | U2RXInterrupt |
| U2TX – UART2 Transmitter | 31 | 000052h | IFS1<15> | IEC1<15> | U2TXInterrupt |
| SPI2 – SPI2 General | 32 | 000054h | IFS2<0> | IEC2<0> | SPI2Interrupt |
| SPI2TX – SPI2 Transfer Done | 33 | 000056h | IFS2<1> | IEC2<1> | SPI2TXInterrupt |
| — | 34 | — | — | — | — |
| — | 35 | — | — | — | — |
| DMA3 – Direct Memory Access 3 | 36 | 00005Ch | IFS2<4> | IEC2<4> | DMA3Interrupt |
| IC3 – Input Capture 3 | 37 | 00005Eh | IFS2<5> | IEC2<5> | IC3Interrupt |
| — | 38 | — | — | — | — |
| — | 39 | — | — | — | — |
| — | 40 | — | — | — | — |
| CCT3 – Capture/Compare Timer3 | 43 | 00006Ah | IFS2<11> | IEC2<11> | CCT3Interrupt |

**REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | REFOMD | CTMUMD | LVDMD | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **REFOMD:** Reference Output Clock Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **CTMUMD:** CTMU Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **LVDMD:** High/Low-Voltage Detect Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **Unimplemented:** Read as ‘0’

## 11.0 I/O PORTS

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSCI/CLKI) are shared between the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger (ST) inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/Os and one register associated with their operation as analog inputs. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Output Latch register (LATx), read the latch; writes to the latch, write the latch. Reads from the PORTx register, read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin, will read as zeros. Table 11-3 through Table 11-5 show ANSELx bits and ports availability for device variants. When a pin is shared with another peripheral or function that is defined as an input only, it is regarded as a dedicated port because there is no other competing source of inputs.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**

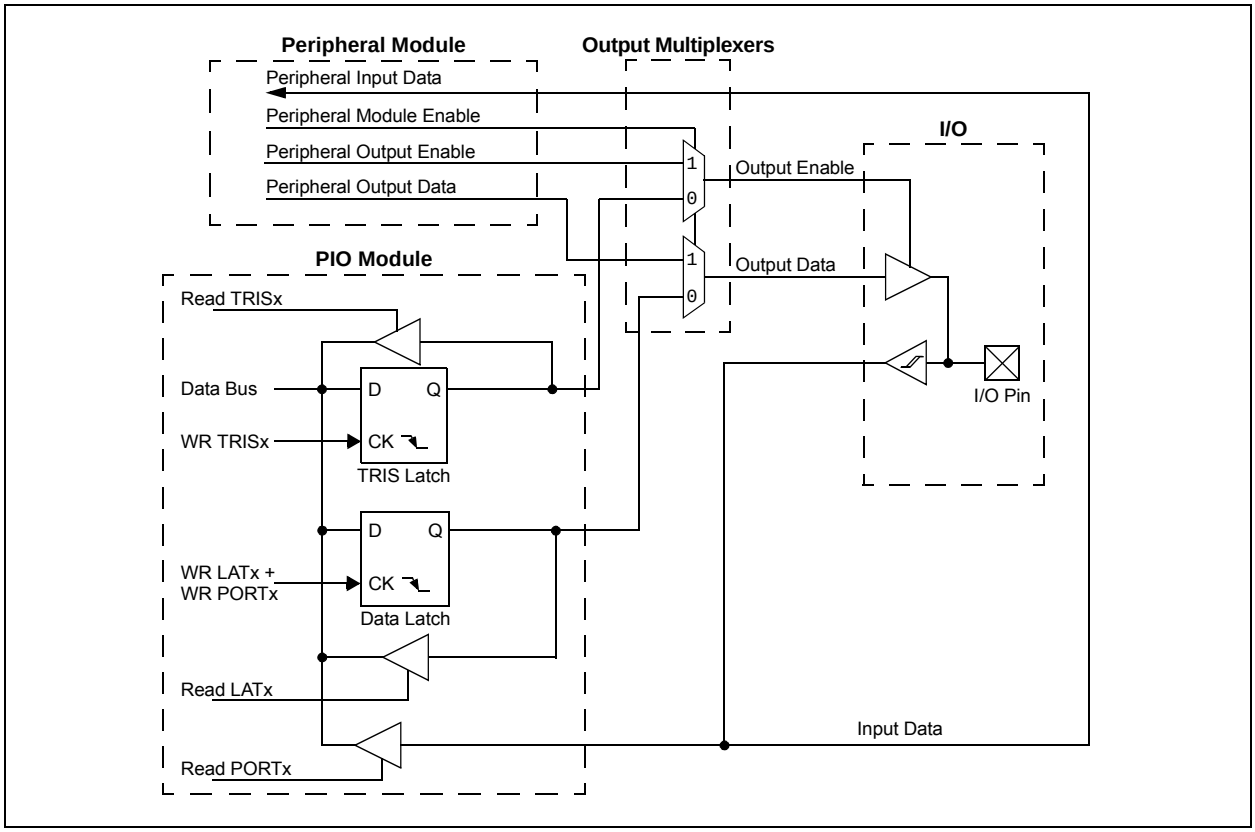


**TABLE 11-3: PORTA PIN AND ANSELx AVAILABILITY**

| Device | PORTA I/O Pins | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RA15 | RA14 | RA13 | RA12 | RA11 | RA10 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| PIC24FJXXXGA705 | — | X | X | X | X | X | X | X | X | — | — | X | X | X | X | X |
| PIC24FJXXXGA704 | — | — | — | — | — | X | X | X | X | — | — | X | X | X | X | X |
| PIC24FJXXXGA702 | — | — | — | — | — | — | — | — | — | — | — | X | X | X | X | X |
| ANSELA bit present | — | — | — | — | — | — | — | — | — | — | — | — | X | X | X | X |

**TABLE 11-4: PORTB PIN AND ANSELx AVAILABILITY**

| Device | PORTB I/O Pins | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| PIC24FJXXXGA705 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| PIC24FJXXXGA704 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| PIC24FJXXXGA702 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ANSELB bit present | X | X | X | X | — | — | X | — | — | — | — | — | X | X | X | X |

**TABLE 11-5: PORTC PIN AND ANSELx AVAILABILITY**

| Device | PORTC I/O Pins | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RC15 | RC14 | RC13 | RC12 | RC11 | RC10 | RC9 | RC8 | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 |
| PIC24FJXXXGA705 | — | — | — | — | — | — | X | X | X | X | X | X | X | X | X | X |
| PIC24FJXXXGA704 | — | — | — | — | — | — | X | X | X | X | X | X | X | X | X | X |
| PIC24FJXXXGA702 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| ANSELC bit present | — | — | — | — | — | — | — | — | — | — | — | — | X | X | X | X |

**REGISTER 11-3: TRISx: OUTPUT ENABLE FOR PORTx REGISTER(1)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| TRISx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| TRISx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **TRISx<15:0>:** Output Enable for PORTx bits
1 = LATx[n] is not driven on the PORTx[n] pin
0 = LATx[n] is driven on the PORTx[n] pin

**Note 1:** See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

**REGISTER 11-4: PORTx: INPUT DATA FOR PORTx REGISTER(1)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PORTx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PORTx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PORTx<15:0>:** PORTx Data Input Value bits

**Note 1:** See Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

#### 11.5.3.2 Output Mapping

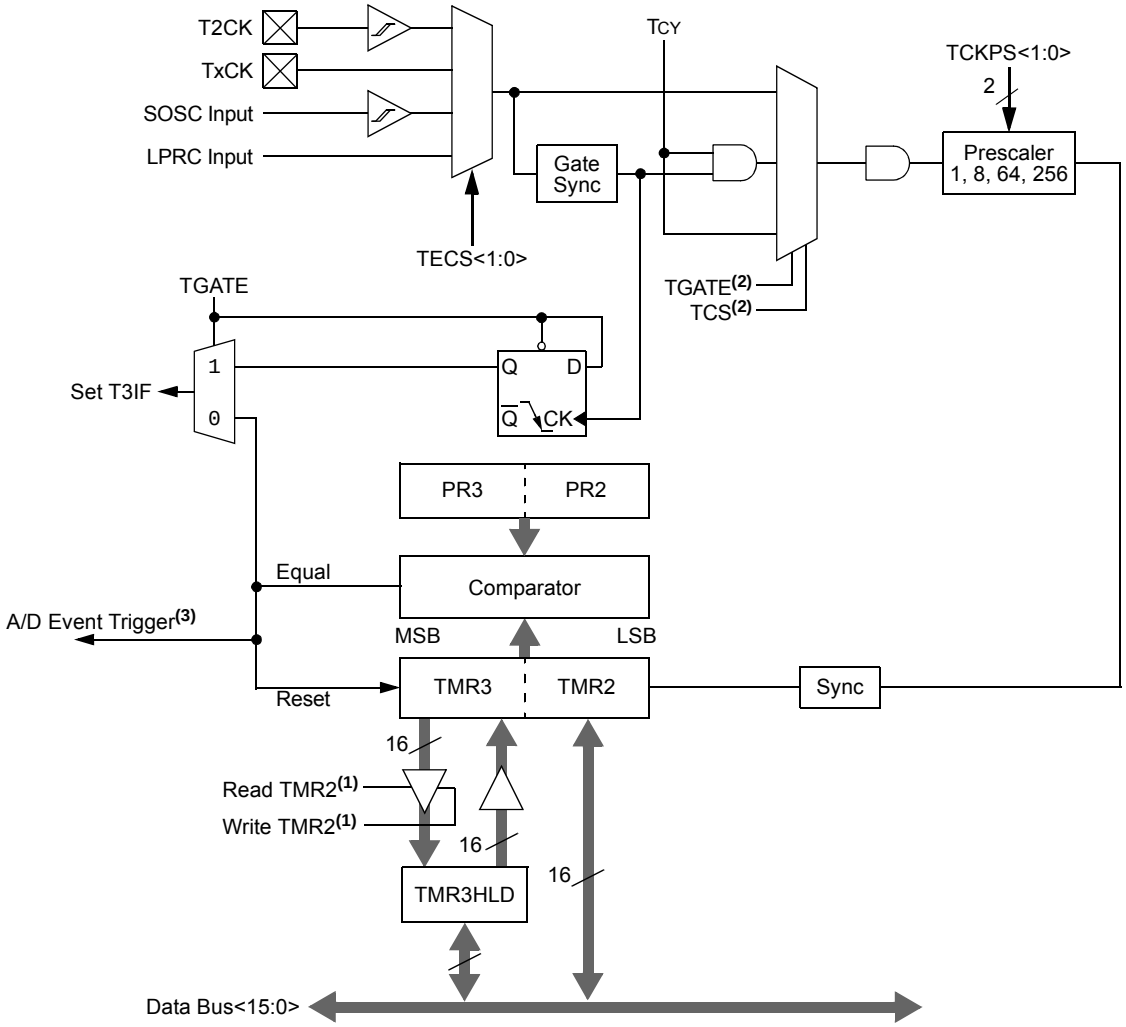
In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains two 6-bit fields, with each field being associated with one RPn pin (see Register 11-32 through Register 11-46). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-7).

Because of the mapping technique, the list of peripherals for output mapping also includes a null value of '000000'. This permits any given pin to remain disconnected from the output of any of the pin-selectable peripherals.

**TABLE 11-7: SELECTABLE OUTPUT SOURCES (MAPS FUNCTION TO OUTPUT)**

| Output Function Number | Function | Output Name |
|---|---|---|
| 0 | None (Pin Disabled) | — |
| 1 | C1OUT | Comparator 1 Output |
| 2 | C2OUT | Comparator 2 Output |
| 3 | U1TX | UART1 Transmit |
| 4 | $\overline{\text{U1RTS}}$ | UART1 Request-to-Send |
| 5 | U2TX | UART2 Transmit |
| 6 | $\overline{\text{U2RTS}}$ | UART2 Request-to-Send |
| 7 | SDO1 | SPI1 Data Output |
| 8 | SCK1OUT | SPI1 Clock Output |
| 9 | SS1OUT | SPI1 Slave Select Output |
| 10 | SDO2 | SPI2 Data Output |
| 11 | SCK2OUT | SPI2 Clock Output |
| 12 | SS2OUT | SPI2 Slave Select Output |
| 13 | OC1 | Output Compare 1 |
| 14 | OC2 | Output Compare 2 |
| 15 | OC3 | Output Compare 3 |
| 16 | OCM2A | CCP2A Output Compare |
| 17 | OCM2B | CCP2B Output Compare |
| 18 | OCM3A | CCP3A Output Compare |
| 19 | OCM3B | CCP3B Output Compare |
| 20 | OCM4A | CCP4A Output Compare |
| 21 | OCM4B | CCP4B Output Compare |
| 22 | Reserved | — |
| 23 | SDO3 | SPI3 Data Output |
| 24 | SCK3OUT | SPI3 Clock Output |
| 25 | SS3OUT | SPI3 Slave Select Output |
| 26 | C3OUT | Comparator 3 Output |
| 27 | PWRGT | RTCC Power Control |
| 28 | REFO | Reference Clock Output |
| 29 | CLC1OUT | CLC1 Output |
| 30 | CLC2OUT | CLC2 Output |
| 31 | RTCC | RTCC Clock Output |

**FIGURE 13-1: TIMER2/3 (32-BIT) BLOCK DIAGRAM**




**Note 1:** The 32-Bit Timer Configuration bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the T2CON register.

**2:** The timer clock input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

**3:** The A/D event trigger is available only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode.

## 14.0 INPUT CAPTURE WITH DEDICATED TIMERS

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Input Capture with Dedicated Timer"** (DS70000352), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ256GA705 family contain three independent input capture modules. Each of the modules offers a wide range of configuration and operating options for capturing external pulse events and generating interrupts.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in All modes by Cascading Two Adjacent modules
- Synchronous and Trigger modes of Output Compare Operation with up to 31 User-Selectable Sync/Trigger Sources Available
- A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to 6 Clock Sources Available for Each module, Driving a Separate Internal 16-Bit Counter

The module is controlled through two registers: ICxCON1 (Register 14-1) and ICxCON2 (Register 14-2). A general block diagram of the module is shown in Figure 14-1.

### 14.1 General Operating Modes

#### 14.1.1 SYNCHRONOUS AND TRIGGER MODES

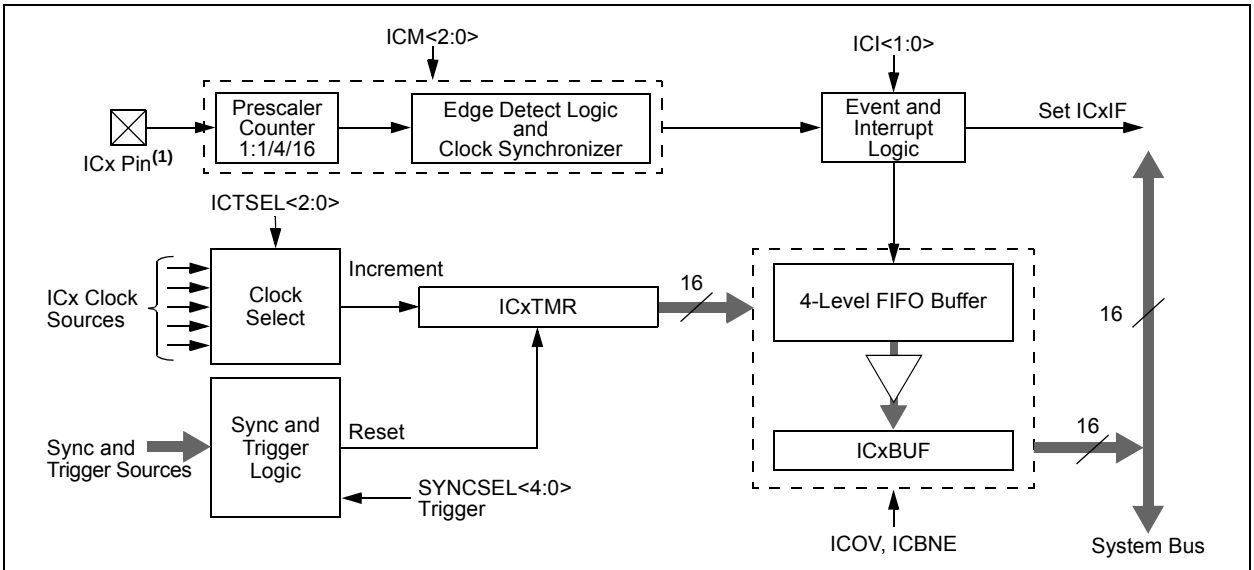
When the input capture module operates in a Free-Running mode, the internal 16-bit counter, ICxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow. Its period is synchronized to the selected external clock source. When a capture event occurs, the current 16-bit value of the internal counter is written to the FIFO buffer.

In Synchronous mode, the module begins capturing events on the ICx pin as soon as its selected clock source is enabled. Whenever an event occurs on the selected Sync source, the internal counter is reset. In Trigger mode, the module waits for a Sync event from another internal module to occur before allowing the internal counter to run.

Standard, free-running operation is selected by setting the SYNCSEL<4:0> bits (ICxCON2<4:0>) to '00000' and clearing the ICTRIG bit (ICxCON2<7>). Synchronous and Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The ICTRIG bit selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the Sync/Trigger source.

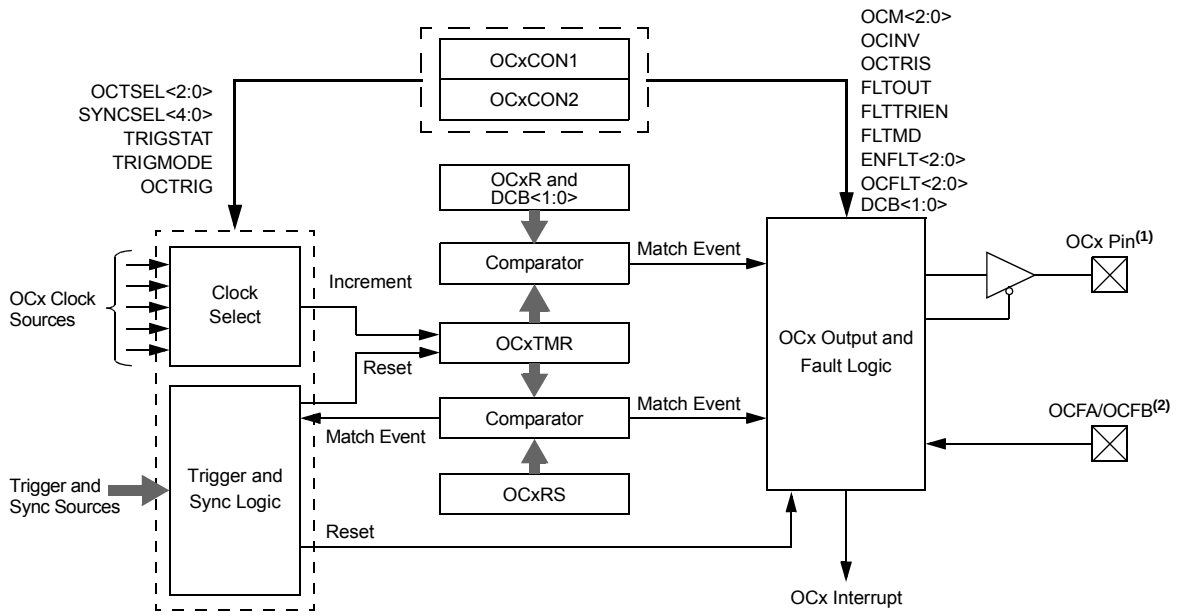
When the SYNCSELx bits are set to '00000' and ICTRIG is set, the module operates in Software Trigger mode. In this case, capture operations are started by manually setting the TRIGSTAT bit (ICxCON2<6>).

**FIGURE 14-1: INPUT CAPTURE x BLOCK DIAGRAM**




**Note 1:** The ICx input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

**FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)**




**Note 1:** The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

**2:** The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

## 15.2 Compare Operations

In Compare mode (Figure 15-1), the output compare module can be configured for Single-Shot or Continuous mode pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins if available on the OCx module you are using. Otherwise, configure the dedicated OCx output pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate the time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= `0xx`).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure Trigger mode operation and TRIGSTAT to select a hardware or software trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the Trigger or Sync source. If free-running timer operation is required, set the SYNCSELx bits to '`00000`' (no Sync/Trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bit for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a Trigger source event occurs.

### 15.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 15-1 for PWM mode timing details. Table 15-1 and Table 15-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

**EQUATION 15-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)**

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{CY}}{F_{PWM} \bullet (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

**Note 1:** Based on FCY = FOSC/2; Doze mode and PLL are disabled.

**EXAMPLE 15-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS(1)**

1. Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where FOSC = 32 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.

   TCY = 2 • TOSC = 62.5 ns

   PWM Period = 1/PWM Frequency = 1/52.08 kHz = 19.2 µS

   PWM Period = (PR2 + 1) • TCY • (Timer2 Prescale Value)

   19.2 µS = (PR2 + 1) • 62.5 ns • 1

   PR2 = 306

2. Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:

   PWM Resolution = $\log_{10}(F_{CY}/F_{PWM})/\log_{10}2)$ bits

   = $(\log_{10}(16\text{ MHz}/52.08\text{ kHz})/\log_{10}2)$ bits

   = 8.3 bits

**Note 1:** Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

**TABLE 15-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (FCY = 4 MHz)(1)**

| PWM Frequency | 7.6 Hz | 61 Hz | 122 Hz | 977 Hz | 3.9 kHz | 31.3 kHz | 125 kHz |
|---|---|---|---|---|---|---|---|
| Timer Prescaler Ratio | 8 | 1 | 1 | 1 | 1 | 1 | 1 |
| Period Register Value | FFFFh | FFFFh | 7FFFh | 0FFFh | 03FFh | 007Fh | 001Fh |
| Resolution (bits) | 16 | 16 | 15 | 12 | 10 | 7 | 5 |

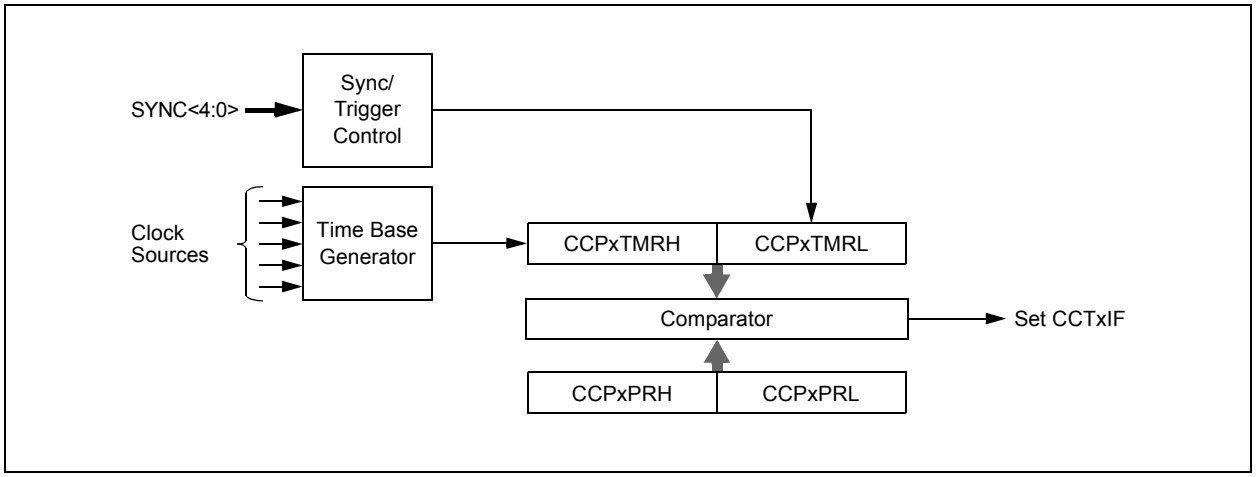
**Note 1:** Based on FCY = FOSC/2; Doze mode and PLL are disabled.

**TABLE 15-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (FCY = 16 MHz)(1)**

| PWM Frequency | 30.5 Hz | 244 Hz | 488 Hz | 3.9 kHz | 15.6 kHz | 125 kHz | 500 kHz |
|---|---|---|---|---|---|---|---|
| Timer Prescaler Ratio | 8 | 1 | 1 | 1 | 1 | 1 | 1 |
| Period Register Value | FFFFh | FFFFh | 7FFFh | 0FFFh | 03FFh | 007Fh | 001Fh |
| Resolution (bits) | 16 | 16 | 15 | 12 | 10 | 7 | 5 |

**Note 1:** Based on FCY = FOSC/2; Doze mode and PLL are disabled.

**FIGURE 16-4: 32-BIT TIMER MODE**




## 16.3 Output Compare Mode

Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The Output Compare x module, on compare match events, has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the Output Compare x module can also generate interrupts on a compare match event.

Table 16-2 shows the various modes available in Output Compare modes.

**TABLE 16-2: OUTPUT COMPARE/PWM MODES**

| MOD<3:0> (CCPxCON1L<3:0>) | T32 (CCPxCON1L<5>) | Operating Mode | |
|---|---|---|---|
| 0001 | 0 | Output High on Compare (16-bit) | Single Edge Mode |
| 0001 | 1 | Output High on Compare (32-bit) | |
| 0010 | 0 | Output Low on Compare (16-bit) | |
| 0010 | 1 | Output Low on Compare (32-bit) | |
| 0011 | 0 | Output Toggle on Compare (16-bit) | |
| 0011 | 1 | Output Toggle on Compare (32-bit) | |
| 0100 | 0 | Dual Edge Compare (16-bit) | Dual Edge Mode |
| 0101 | 0 | Dual Edge Compare (16-bit buffered) | PWM Mode |
| 0110 | 0 | Center-Aligned Pulse (16-bit buffered) | Center PWM Mode |
| 0111 | 0 | Variable Frequency Pulse (16-bit) | |
| 1111 | 0 | External Input Source Mode (16-bit) | |

**REGISTER 16-3: CCPxCON2L: CCPx CONTROL 2 LOW REGISTERS**

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PWMRSEN | ASDGM | — | SSDG | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
- 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
- 0 = ASEVT bit must be cleared in software to resume PWM activity on output pins

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
- 1 = Waits until the next Time Base Reset or rollover for shutdown to occur
- 0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
- 1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
- 0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
- 1 = ASDGx Source n is enabled (see Table 16-6 for auto-shutdown/gating sources)
- 0 = ASDGx Source n is disabled

**TABLE 16-6: AUTO-SHUTDOWN SOURCES**

| ASDG<7:0> | Auto-Shutdown Source | | | |
|---|---|---|---|---|
| | MCCP1 | MCCP2 | MCCP3 | MCCP4 |
| 1xxx xxxx | OCFB | | | |
| x1xx xxxx | OCFA | | | |
| xx1x xxxx | CLC1 | CLC2 | Not Used | |
| xxx1 xxxx | Not Used | | | |
| xxxx 1xxx | Not Used | | | |
| xxxx x1xx | CMP3 Out | | | |
| xxxx xx1x | CMP2 Out | | | |
| xxxx xxx1 | CMP1 Out | | | |

## 21.2 RTCC Module Registers

The RTCC module registers are organized into four categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers
- Timestamp Registers

### 21.2.1 REGISTER MAPPING

Previous RTCC implementations used a Register Pointer to access the RTCC Time and Date registers, as well as the Alarm Time and Date registers. These Registers are now mapped to memory and are individually addressable.

### 21.2.2 WRITE LOCK

To prevent spurious changes to the Time Control or Time Value registers, the WRLOCK bit (RTCCON1L1<11>) must be cleared (‘0’). The POR default state is when the WRLOCK bit is ‘0’ and is cleared on any device Reset (POR, BOR, $\overline{\text{MCLR}}$). It is recommended that the WRLOCK bit be set to ‘1’ after the Date and Time registers are properly initialized, and after the RTCEN bit (RTCCON1L<15>) has been set.

Any attempt to write to the RTCEN bit, the RTCCON2L/H registers, or the Date or Time registers, will be ignored as long as WRLOCK is ‘1’. The Alarm, Power Control and Timestamp registers can be changed when WRLOCK is ‘1’.

Clearing the WRLOCK bit requires an unlock sequence after it has been written to a ‘1’, writing two bytes consecutively to the NVMKEY register. A sample assembly sequence is shown in Example 21-1. If WRLOCK is already cleared, it can be set to ‘1’ without using the unlock sequence.

| | |
|---|---|
| **Note:** | To avoid accidental writes to the timer, it is recommended that the WRLOCK bit (RTCCON1L<11>) is kept clear at any other time. For the WRLOCK bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of WRLOCK; therefore, it is recommended that code follow the procedure in Example 21-1. |

### 21.2.3 SELECTING RTCC CLOCK SOURCE

The clock source for the RTCC module can be selected using the CLKSEL<1:0> bits in the RTCCON2L register. When the bits are set to ‘00’, the Secondary Oscillator (SOSC) is used as the reference clock and when the bits are ‘01’, LPRC is used as the reference clock. When CLKSEL<1:0> = 10, the external power-line (50 Hz and 60 Hz) is used as the clock source. When CLKSEL<1:0> = 11, the system clock is used as the clock source.

**EXAMPLE 21-1: SETTING THE WRLOCK BIT**

```
DISI    #6                    ;disable interrupts for 6 instructions
MOV     #NVKEY, W1
MOV     #0x55, W2             ; first unlock code
MOV     W2, [W1]              ; write first unlock code
MOV     #0xAA, W3             ; second unlock sequence
MOV     W3, [W1]              ; write second unlock sequence
BCLR    RTCCON1L, #WRLOCK     ; clear the WRLOCK bit
```

**REGISTER 29-5: FOSC CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 |
|---|---|---|---|---|---|---|---|
| FCKSM1 | FCKSM0 | IOL1WAY | PLLSS | SOSCSEL | OSCIOFCN | POSCMD1 | POSCMD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-6 **FCKSM<1:0>:** Clock Switching and Monitor Selection bits
1x = Clock switching and the Fail-Safe Clock Monitor are disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching and the Fail-Safe Clock Monitor are enabled

bit 5 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = The IOLOCK bit can be set only once (with unlock sequence).
0 = The IOLOCK bit can be set and cleared as needed (with unlock sequence)

bit 4 **PLLSS:** PLL Secondary Selection Configuration bit
This Configuration bit only takes effect when the PLL is NOT being used by the system (i.e., not selected as part of the system clock source). Used to generate an independent clock out of REFO.
1 = PLL is fed by the Primary Oscillator
0 = PLL is fed by the on-chip Fast RC (FRC) Oscillator

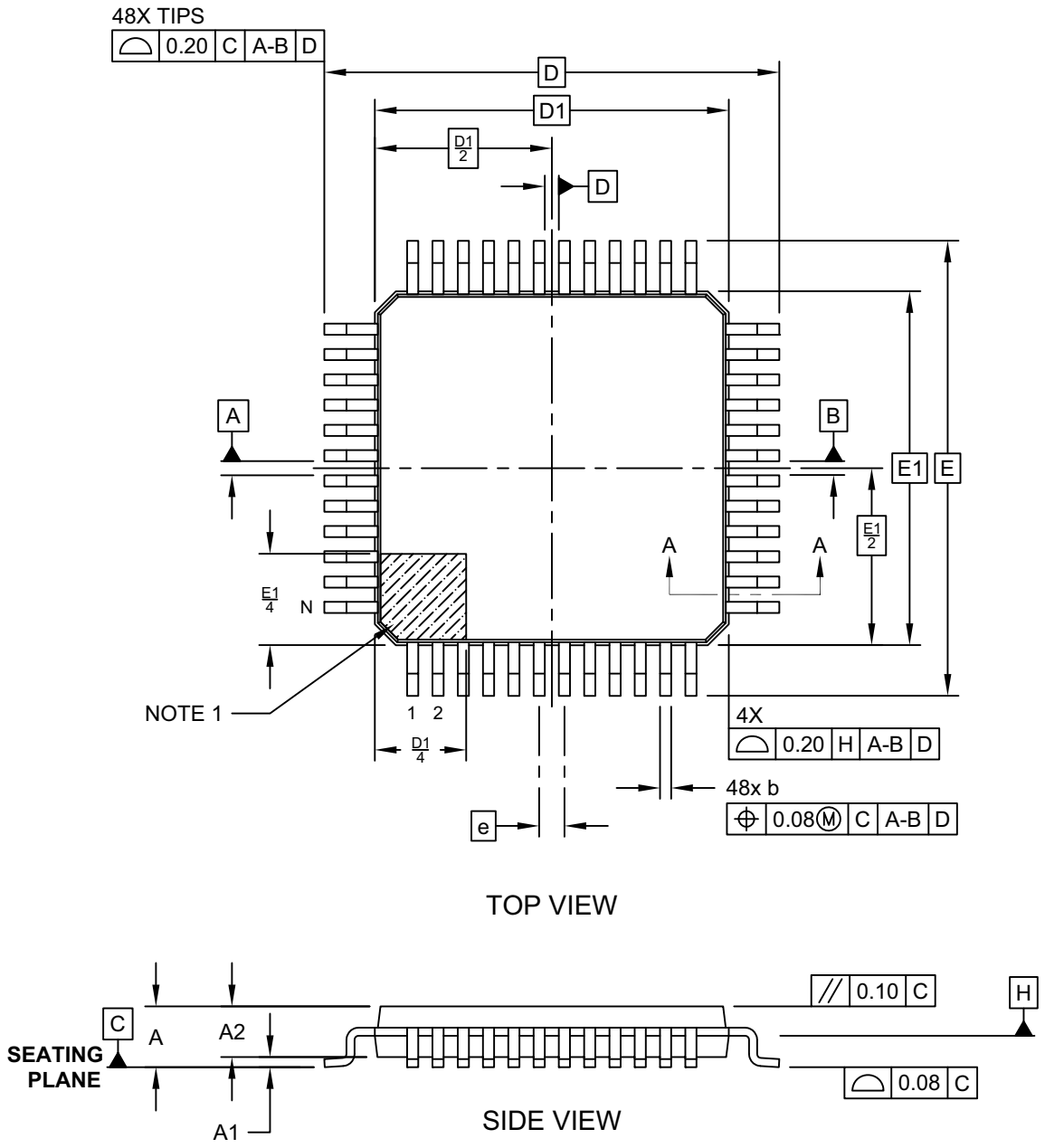
bit 3 **SOSCSEL:** SOSC Selection Configuration bit
1 = Crystal (SOSCI/SOSCO) mode
0 = Digital (SOSCI) Externally Supplied Clock mode

bit 2 **OSCIOFCN:** CLKO Enable Configuration bit
1 = CLKO output signal is active on the OSCO pin (when the Primary Oscillator is disabled or configured for EC mode)
0 = CLKO output is disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator mode is disabled
10 = HS Oscillator mode is selected (10 MHz-32 MHz)
01 = XT Oscillator mode is selected (1.5 MHz-10 MHz)
00 = External Clock mode is selected

### 48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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