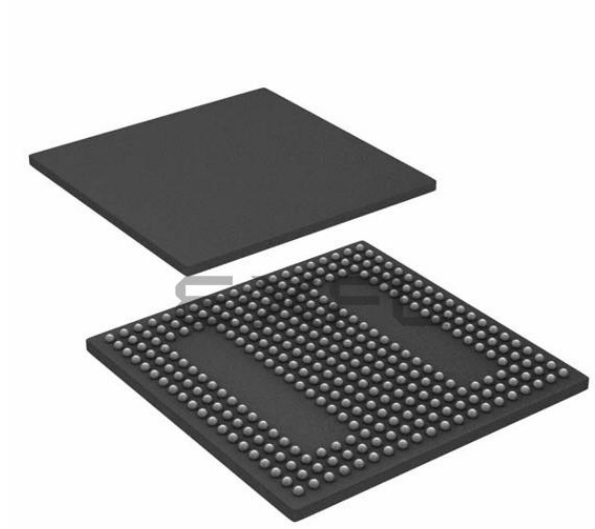

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	316-LFBGA, CSPBGA
Supplier Device Package	316-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf539wbbcz405

general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

Table 3. System and Core Event Mapping

Event Source	Core Event Name
PLL Wake-Up Interrupt	IVG7
DMA Controller 0 Error	IVG7
DMA Controller 1 Error	IVG7
PPI Error Interrupt	IVG7
SPORT0 Error Interrupt	IVG7
SPORT1 Error Interrupt	IVG7
SPORT2 Error Interrupt	IVG7
SPORT3 Error Interrupt	IVG7
MXVR Synchronous Data Interrupt	IVG7
SPI0 Error Interrupt	IVG7
SPI1 Error Interrupt	IVG7
SPI2 Error Interrupt	IVG7
UART0 Error Interrupt	IVG7
UART1 Error Interrupt	IVG7
UART2 Error Interrupt	IVG7
CAN Error Interrupt	IVG7
Real-Time Clock Interrupt	IVG8
DMA0 Interrupt (PPI)	IVG8
DMA1 Interrupt (SPORT0 Rx)	IVG9
DMA2 Interrupt (SPORT0 Tx)	IVG9
DMA3 Interrupt (SPORT1 Rx)	IVG9
DMA4 Interrupt (SPORT1 Tx)	IVG9
DMA8 Interrupt (SPORT2 Rx)	IVG9
DMA9 Interrupt (SPORT2 Tx)	IVG9
DMA10 Interrupt (SPORT3 Rx)	IVG9
DMA11 Interrupt (SPORT3 Tx)	IVG9
DMA5 Interrupt (SPI0)	IVG10
DMA14 Interrupt (SPI1)	IVG10
DMA15 Interrupt (SPI2)	IVG10
DMA6 Interrupt (UART0 Rx)	IVG10
DMA7 Interrupt (UART0 Tx)	IVG10
DMA16 Interrupt (UART1 Rx)	IVG10
DMA17 Interrupt (UART1 Tx)	IVG10
DMA18 Interrupt (UART2 Rx)	IVG10
DMA19 Interrupt (UART2 Tx)	IVG10
Timer0, Timer1, Timer2 Interrupts	IVG11
TWI0 Interrupt	IVG11
TWI1 Interrupt	IVG11
CAN Receive Interrupt	IVG11
CAN Transmit Interrupt	IVG11
MXVR Status Interrupt	IVG11
MXVR Control Message Interrupt	IVG11
MXVR Asynchronous Packet Interrupt	IVG11
Programmable Flags Interrupts	IVG12
MDMA0 Stream 0 Interrupt	IVG13
MDMA0 Stream 1 Interrupt	IVG13
MDMA1 Stream 0 Interrupt	IVG13
MDMA1 Stream 1 Interrupt	IVG13
Software Watchdog Timer	IVG13

DMA CONTROLLERS

The processors have multiple, independent DMA controllers that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the ADSP-BF539/ADSP-BF539F processor internal memories and any of its DMA capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA capable peripherals include the SPORTs, SPI ports, UARTs, and PPI. Each individual DMA capable peripheral has at least one dedicated DMA channel. In addition, the MXVR peripheral has its own dedicated DMA controller, which supports its own unique set of operating modes.

The DMA controllers support both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be deinterleaved on the fly.

Examples of DMA types supported by the processor's DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are four memory DMA channels provided for transfers between the various memories of the ADSP-BF539/ADSP-BF539F processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The ADSP-BF539/ADSP-BF539F processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the Blackfin processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

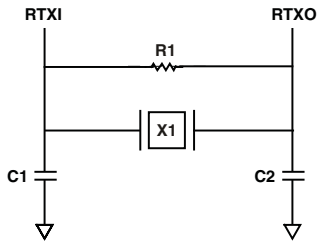
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: the first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wake-up event. Additionally, an RTC wake-up event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 5.



SUGGESTED COMPONENTS:
ECLIPTEK EC38J (THROUGH-HOLE PACKAGE)
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22pF
C2 = 22pF
R1 = 10MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3pF.

Figure 5. External Components for RTC

WATCHDOG TIMER

The processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. Programs initialize the count value of the timer, enable the appropriate interrupt, and then enable the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF539/ADSP-BF539F processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to

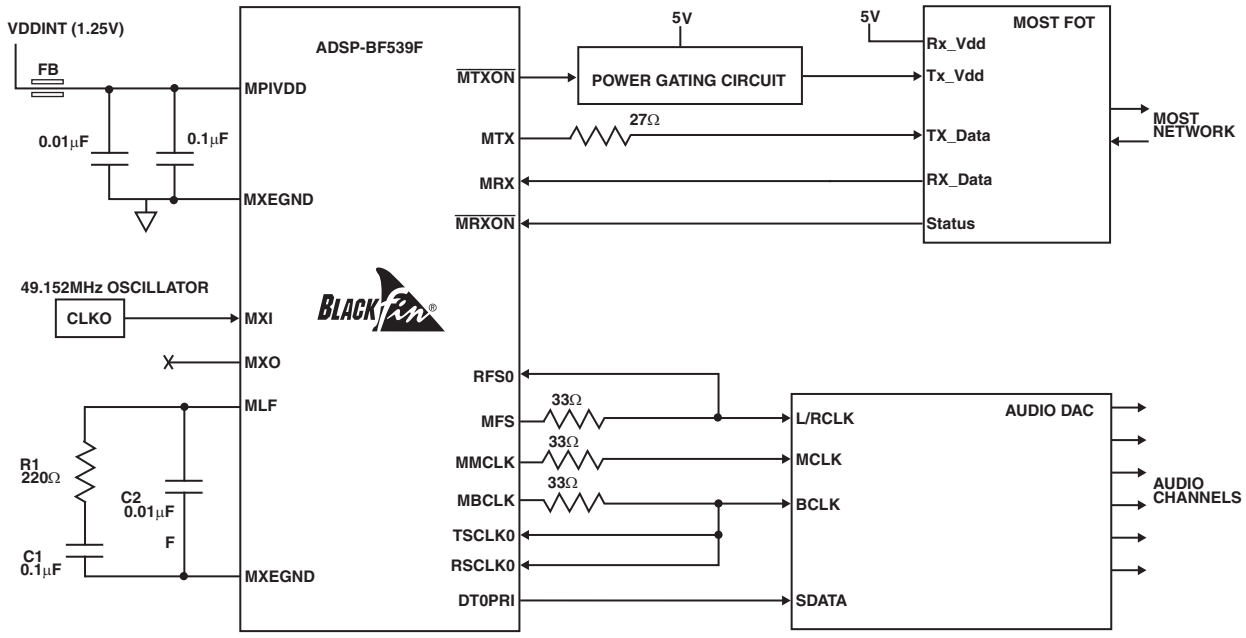


Figure 9. Example Connections of ADSP-BF539/ADSP-BF539F to MOST Network

MXEVDD–MXVR crystal oscillator 3.3 V power

- Should be routed with wide traces or as power plane.
- Locally bypass MXEVDD with 0.1 µF and 0.01 µF decoupling capacitors to MXEGND.
- Avoid routing other switching signals near to MXEVDD to avoid crosstalk.

MPIVDD–MXVR PLL 1.25 V power

- Should be routed with wide traces or as power plane.
- A ferrite bead should be placed between the 1.25 V V_{DDINT} power plane and the MPIVDD pin for noise isolation.
- Locally bypass MPIVDD with 0.1 µF and 0.01 µF decoupling capacitors to MXEGND.
- Avoid routing other switching signals near to MPIVDD to avoid crosstalk.

Fiber optic transceiver (FOT) connections

- The traces between the ADSP-BF539/ADSP-BF539F processor and the FOT should be kept as short as possible.
- The receive data trace connecting the FOT receive data output pin to the ADSP-BF539/ADSP-BF539F MRX input pin should not have a series termination resistor. The edge rate of the FOT receive data signal driven by the FOT is typically very slow, and further degradation of the edge rate is not desirable.
- The transmit data trace connecting the processor's MTX output pin to the FOT Transmit Data input pin should have a 27 W series termination resistor placed close to the ADSP-BF539/ADSP-BF539F MTX pin.
- The receive data trace and the transmit data trace between the processor and the FOT should not be routed close to each other in parallel over long distances to avoid crosstalk.

VOLTAGE REGULATOR LAYOUT GUIDELINES

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1-0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the ADSP-BF539/ADSP-BF539F as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices website (www.analog.com)—use site search on "EE-228".

Table 10. Pin Descriptions (Continued)

Pin Name	Type	Description	Driver Type[1]
Parallel Peripheral Interface Port/GPIO			
PF0/*SPI0SS*	I/O	Programmable Flag 0/*SPI0 Slave Select Input*	C
PF1/*SPI0SEL1*/*TACLK*	I/O	Programmable Flag 1/*SPI0 Slave Select Enable 1/Timer Alternate Clock*	C
PF2/*SPI0SEL2*	I/O	Programmable Flag 2/*SPI0 Slave Select Enable 2*	C
PF3/*SPI0SEL3*/*PPI_FS3*	I/O	Programmable Flag 3/*SPI0 Slave Select Enable 3/PPI Frame Sync 3*	C
PF4/*SPI0SEL4*/*PPI15*	I/O	Programmable Flag 4/*SPI0 Slave Select Enable 4/PPI 15*	C
PF5/*SPI0SEL5*/*PPI14*	I/O	Programmable Flag 5/*SPI0 Slave Select Enable 5/PPI 14*	C
PF6/*SPI0SEL6*/*PPI13*	I/O	Programmable Flag 6/*SPI0 Slave Select Enable 6/PPI 13*	C
PF7/*SPI0SEL7*/*PPI12*	I/O	Programmable Flag 7/*SPI0 Slave Select Enable 7/PPI 12*	C
PF8/*PPI11*	I/O	Programmable Flag 8/*PPI 11*	C
PF9/*PPI10*	I/O	Programmable Flag 9/*PPI 10*	C
PF10/*PPI9*	I/O	Programmable Flag 10/*PPI 9*	C
PF11/*PPI8*	I/O	Programmable Flag 11/*PPI 8*	C
PF12/*PPI7*	I/O	Programmable Flag 12/*PPI 7*	C
PF13/*PPI6*	I/O	Programmable Flag 13/*PPI 6*	C
PF14/*PPI5*	I/O	Programmable Flag 14/*PPI 5*	C
PF15/*PPI4*	I/O	Programmable Flag 15/*PPI 4*	C
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	
Controller Area Network			
CANTX/*PC0*	I/O 5 V	CAN Transmit/*GPIO*	C
CANRX/*PC1*	I/OD 5 V	CAN Receive/*GPIO*	C[2]
Media Transceiver (MXVR)/General-Purpose I/O			
MTX/*PC5*	I/O	MXVR Transmit Data/*GPIO*	C
MTXON/*PC9*	I/O	MXVR Transmit FOT On/*GPIO*	C
MRX/*PC4*	I/OD 5 V	MXVR Receive Data/*GPIO* (This pin should be pulled low when not used.)	C[2]
MRXON	I 5 V	MXVR FOT Receive On (This pin should be pulled high when not used.)	C
MXI	I	MXVR Crystal Input (This pin should be pulled low when not used.)	
MXO	O	MXVR Crystal Output (This pin should be left unconnected when not used.)	
MLF	A I/O	MXVR Loop Filter (This pin should be pulled low when not used.)	
MMCLK/*PC6*	I/O	MXVR Master Clock/*GPIO*	C
MBCLK/*PC7*	I/O	MXVR Bit Clock/*GPIO*	C
MFS/*PC8*	I/O	MXVR Frame Sync/*GPIO*	C
GP	I	GPIO PC4–9 Enable (This pin should be pulled low when MXVR is used.)	
2-Wire Interface Ports These pins are open-drain and require a pull-up resistor. See version 2.1 of the I^2C specification for proper resistor values.			
SDA0	I/O 5 V	TWI0 Serial Data	E
SCL0	I/O 5 V	TWI0 Serial Clock	E
SDA1	I/O 5 V	TWI1 Serial Data	E
SCL1	I/O 5 V	TWI1 Serial Clock	E

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nom	Max	Unit
V_{DDINT}	Internal Supply Voltage[1, 2]		0.95	1.25	1.375	V
V_{DDEXT}	External Supply Voltage[3]		2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4]	V_{DDEXT} = Maximum	2.0			V
V_{IH5V}	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[4, 7]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	Low Level Input Voltage[5]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	316-Ball Chip Scale Ball Grid Array Package (CSP_BGA) 533 MHz @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+110	°C

[1] Parameter value applies also to MPIVDD.
[2] The regulator can generate V_{DDINT} at levels of 1.0 V to 1.2 V with –5% to +10% tolerance and 1.25 V with –4% to +10% tolerance.
[3] Parameter value applies also to MXEVDD.
[4] The 3.3 V tolerant pins are capable of accepting up to 3.6 V maximum V_{IH} The following bidirectional pins are 3.3 V tolerant: DATA15–0, SCK2–0, MISO2–0, MOSI2–0, PF15–0, PPI3–0, $\overline{MTXON}$, MMCLK, MBCLK, MFS, MTX, $\overline{SPI1SS}$, $\overline{SPI1SEL1}$, $\overline{SPI2SS}$, $\overline{SPI2SEL1}$, RX2–1, TX2–1, DT2PRI, DT2SEC, TSCLK3–0, DR2PRI, DR2SEC, DT3PRI, DT3SEC, RSCLK3–0, TFS3–0, RFS3–0, DR3PRI, DR3SEC, and TMR2–0. The following input-only pins are 3.3 V tolerant: $\overline{RESET}$, RX0, TCK, TDI, TMS, $\overline{TRST}$, ARDY, BMODE1–0, $\overline{BR}$, DR0PRI, DR0SEC, DR1PRI, DR1SEC, $\overline{NMI}$, PPI_CLK, RTXI, and GP.
[5] The 5 V tolerant pins are capable of accepting up to 5.5 V maximum V_{IH}. The following bidirectional pins are 5 V tolerant: SCL0, SCL1, SDA0, SDA1, and CANTX. The following input-only pins are 5 V tolerant: CANRX, MRX, $\overline{MRXON}$.
[6] Parameter value applies to the CLKIN and MXI input pins.
[7] Parameter value applies to all input and bidirectional pins.

The following tables describe the voltage/frequency requirements for the ADSP-BF538/ADSP-BF538F processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 11. Core Clock (CCLK) Requirements

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.2 V Minimum)	1.25 V	533	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	133[2]	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}
[2] Guaranteed to t_{SCLK} = 7.5 ns. See Table 26 on Page 36.

System designers should refer to *Estimating Power for the ADSP-BF538/BF539 Blackfin Processors (EE-298)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-298. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 27 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 16).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 15).

Table 14. Static Current (mA)[1]

	V_{DDINT} (V)												
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V
–40	6.4	7.7	8.8	10.4	12.0	14.0	16.1	18.9	21.9	25.2	28.7	30.6	35.9
–25	9.2	10.9	12.5	14.5	16.7	19.3	22.1	25.6	29.5	33.7	38.1	40.5	47.2
0	16.8	18.9	21.5	24.4	27.7	31.7	35.8	40.5	45.8	51.6	58.2	61.0	69.8
25	32.9	37.2	41.4	46.2	51.8	57.4	64.2	72.3	80.0	89.3	98.9	103.3	116.4
40	48.4	54.8	60.5	67.1	74.7	82.9	91.6	101.5	112.4	123.2	136.2	142.0	158.7
55	71.2	78.6	86.5	95.8	104.9	115.7	127.1	139.8	153.6	168.0	183.7	191.0	211.8
70	102.3	112.2	122.1	133.5	146.1	159.2	173.9	189.8	206.7	225.5	245.6	254.1	279.6
85	140.7	153.0	167.0	182.5	198.0	216.0	234.3	254.0	276.0	299.1	324.3	334.8	366.6
100	190.6	207.1	224.6	244.0	265.6	285.7	309.0	333.7	360.0	387.8	417.3	431.1	469.3
105	210.2	228.1	245.1	265.6	285.8	309.2	334.0	360.1	385.6	417.2	448.0	461.5	501.1

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 15. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK-MXVR}$	1.36
$I_{DD-HIGH-MXVR}$	1.32
$I_{DD-PEAK}$	1.30
$I_{DD-HIGH}$	1.28
$I_{DD-TYP-MXVR}$	1.07
I_{DD-TYP}	1.00
$I_{DD-APP-MXVR}$	0.92
I_{DD-APP}	0.88
$I_{DD-NOP-MXVR}$	0.76
I_{DD-NOP}	0.74
$I_{DD-IDLE-MXVR}$	0.50
$I_{DD-IDLE}$	0.48

[1] See EE-298 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 17 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})[1]	–0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DDEXT})[2]	–0.3 V to +3.8 V
Input Voltage[3, 4]	–0.5 V to +3.8 V
Input Voltage[4, 5]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Junction Temperature While Biased	+125°C
Storage Temperature Range	–65°C to +150°C

[1] Parameter value applies also to MPIVDD.
[2] Parameter value applies also to MXEVDD and V_{DDRTC}.
[3] Applies to 100% transient duty cycle. For other duty cycles, see Table 18.
[4] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.
[5] Applies to pins designated as 5 V tolerant only.

Table 18. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, MXI, MXO, MLF, VROUT1–0, XTAL, RTXI, and RTXO.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. The is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 19 provides information about how to read the package brand and relate it to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 60.

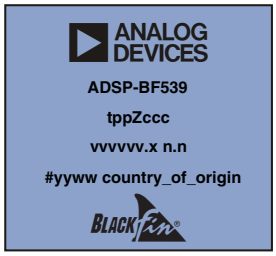


Figure 10. Product Information on Package

Table 19. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.xw	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

TIMING SPECIFICATIONS

Component specifications are subject to change with PCN notice.

Clock and Reset Timing

Table 20 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 30, combinations of CLKIN and clock multipliers must not select core/peripheral clocks that exceed maximum operating conditions.

Table 20. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency (Commercial/ Industrial Models) [1, 2, 3, 4]	10	50	MHz
	CLKIN Frequency (Automotive Models) [1, 2, 3, 4]	10	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	8		ns
t_{CKINH}	CLKIN High Pulse[1]	8		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 12 on Page 26 through Table 16 on Page 29.
[3] The t_{CKIN} period (see Figure 11) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.
[5] Applies after power-up sequence is complete. See Table 21 and Figure 12 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

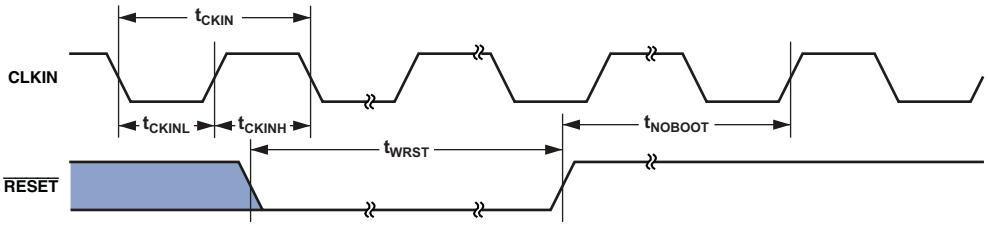
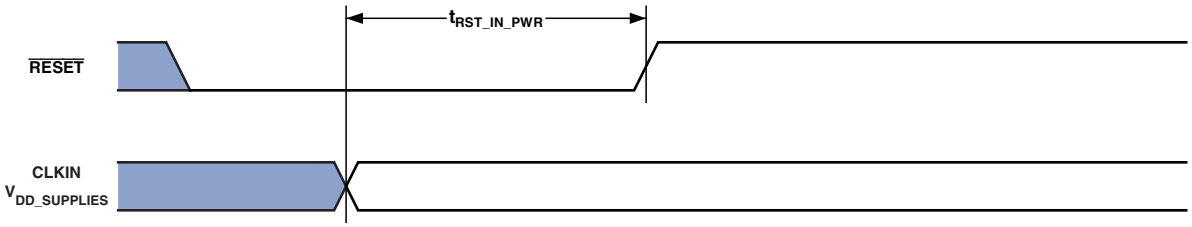


Figure 11. Clock and Reset Timing

Table 21. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, MPIVDD, MXEVDD, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}, MPIVDD, MXEVDD

Figure 12. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 22 and Table 23 on Page 33 and Figure 13 and Figure 14 on Page 33 describe asynchronous memory read cycle operations for synchronous and for asynchronous ARDY.

Table 22. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

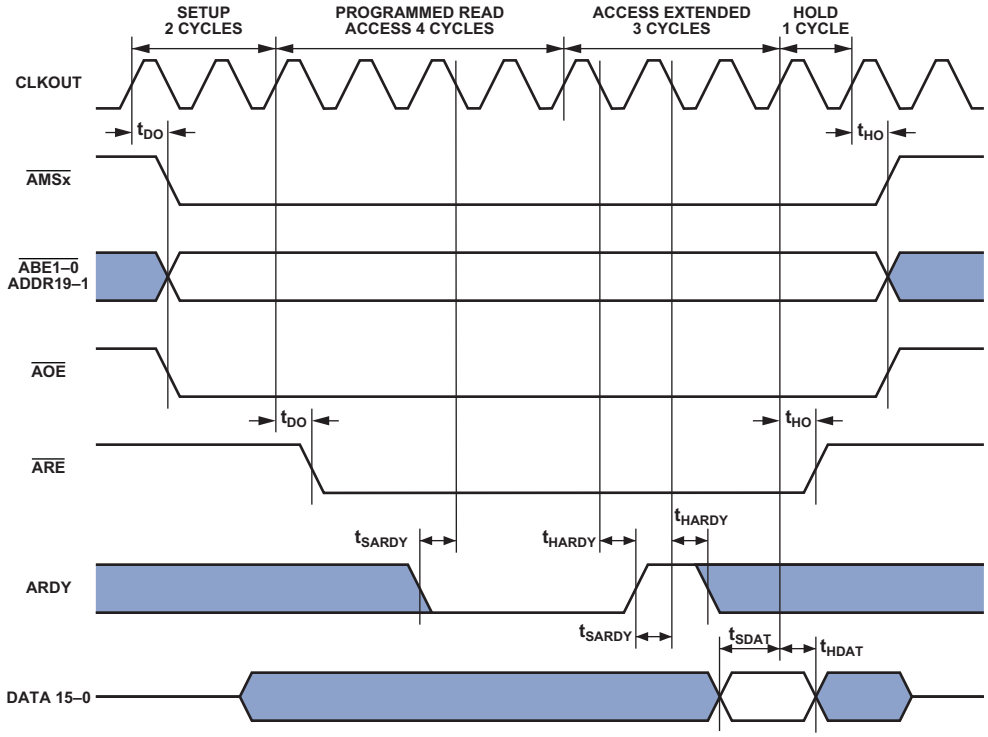


Figure 13. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Table 23. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{DANR}	ARDY Negated Delay from $\overline{AMSx}$ Asserted[1]		$(S + RA - 2) \times t_{SCLK}$	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[2]		6.0	ns
t_{HO}	Output Hold After CLKOUT[2]	0.8		ns

[1] S = number of programmed setup cycles, RA = number of programmed read access cycles.
[2] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

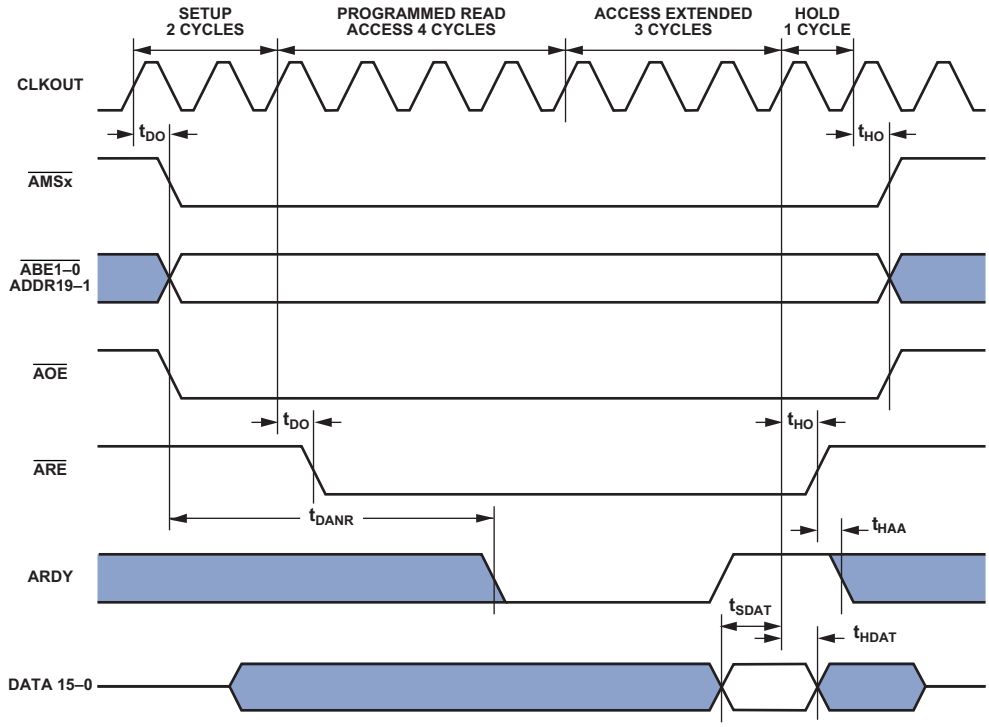


Figure 14. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

SDRAM Interface Timing

Table 26. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{SCLK}	CLKOUT Period[1]	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[2]		6.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[2]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns

[1] SDRAM timing for $T_{JUNCTION}$ = 125°C is limited to 100 MHz.
[2] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

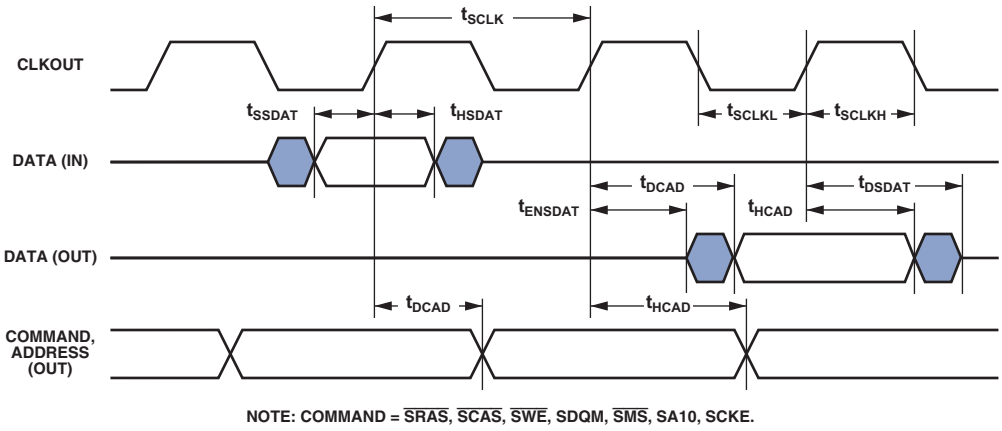


Figure 17. SDRAM Interface Timing

Table 28. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulse Width	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ High Setup		3.6	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		3.6	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ High Setup		3.6	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		3.6	ns

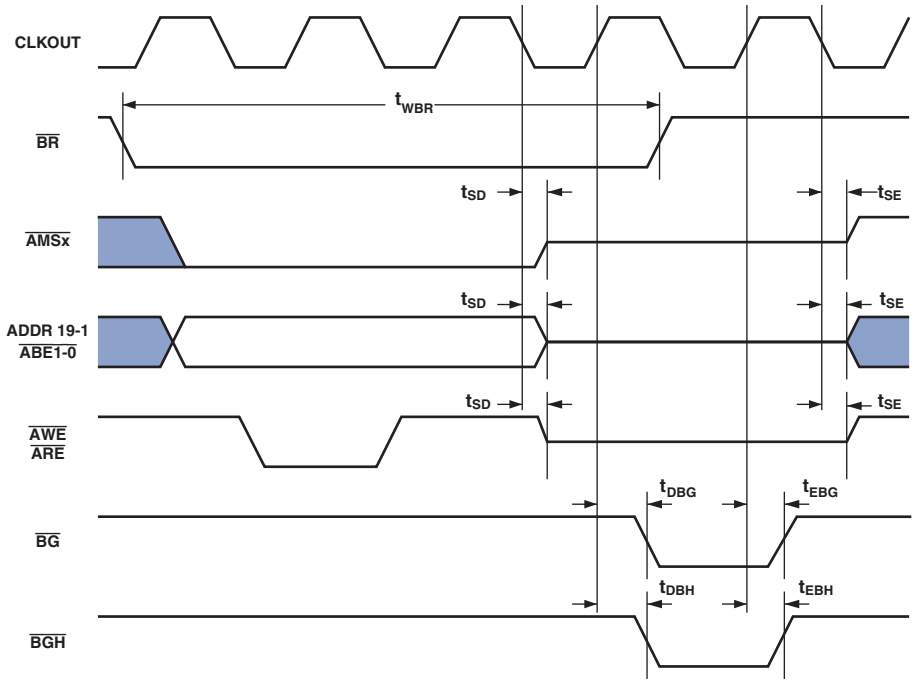


Figure 19. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parallel Peripheral Interface Timing

Table 29 and Figure 20, Figure 21, Figure 22, and Figure 23 describe Parallel Peripheral Interface operations.

Table 29. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width	6.0		ns
t_{PCLK}	PPI_CLK Period[1]	15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK	5.0		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	2.0		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	4.0		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		10.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	0.0		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		10.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	0.0		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

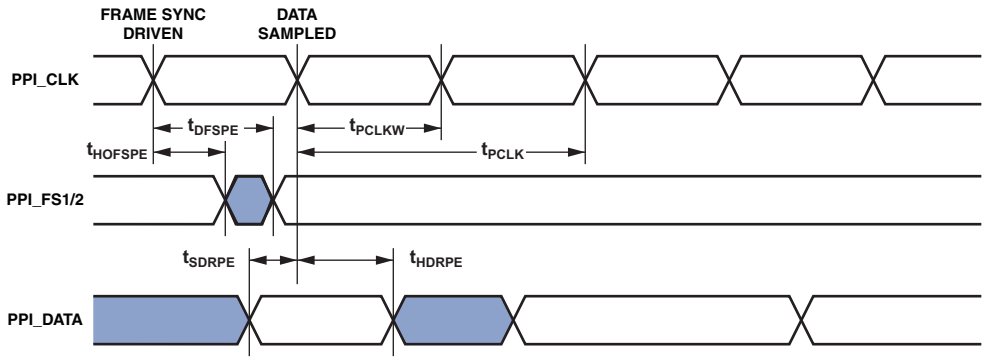


Figure 20. PPI GP Rx Mode with Internal Frame Sync Timing

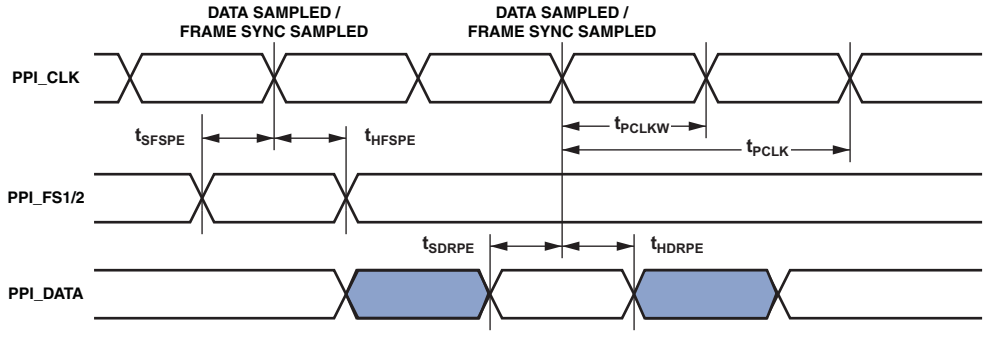


Figure 21. PPI GP Rx Mode with External Frame Sync Timing

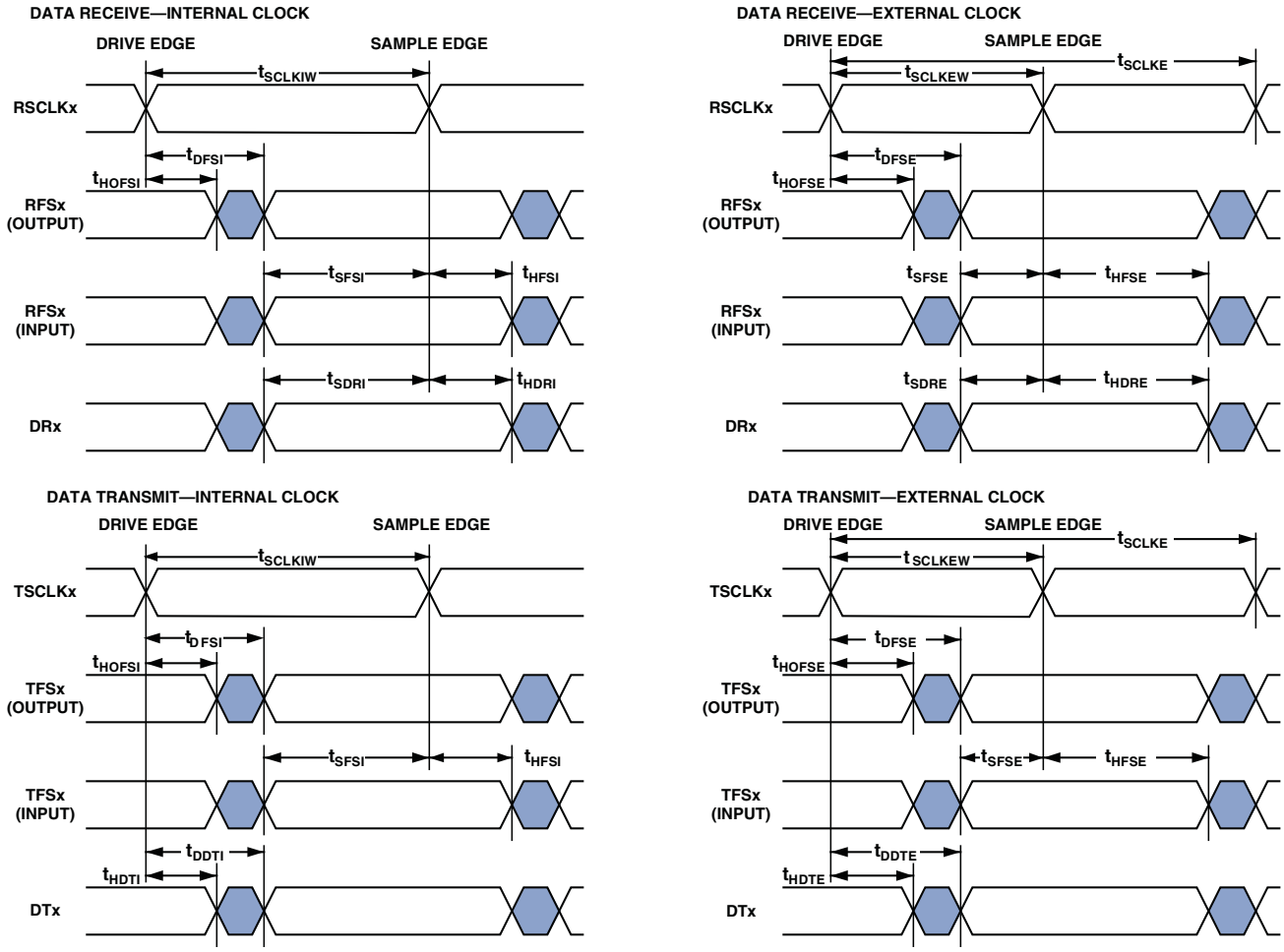


Figure 24. Serial Ports

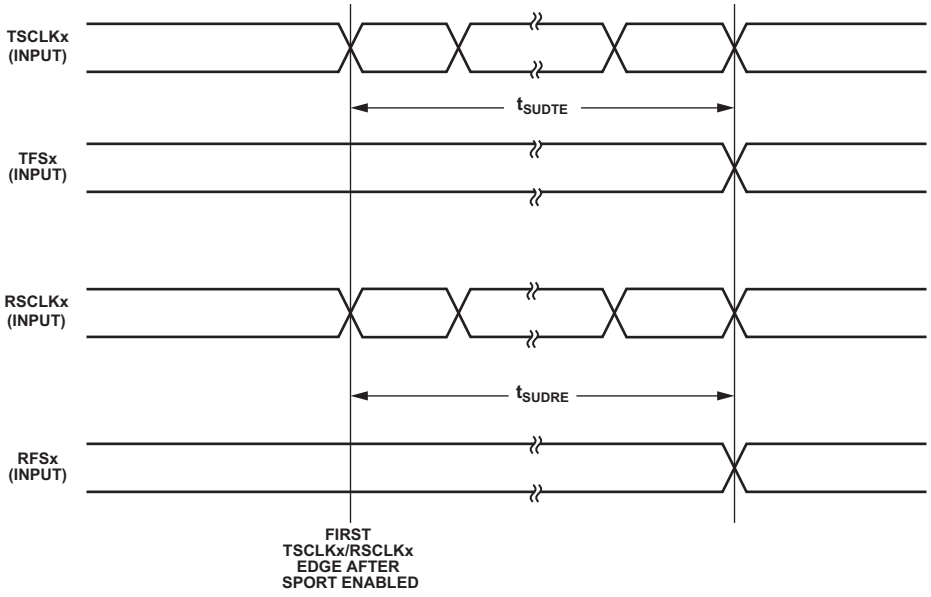


Figure 25. Serial Port Start Up with External Clock and Frame Sync

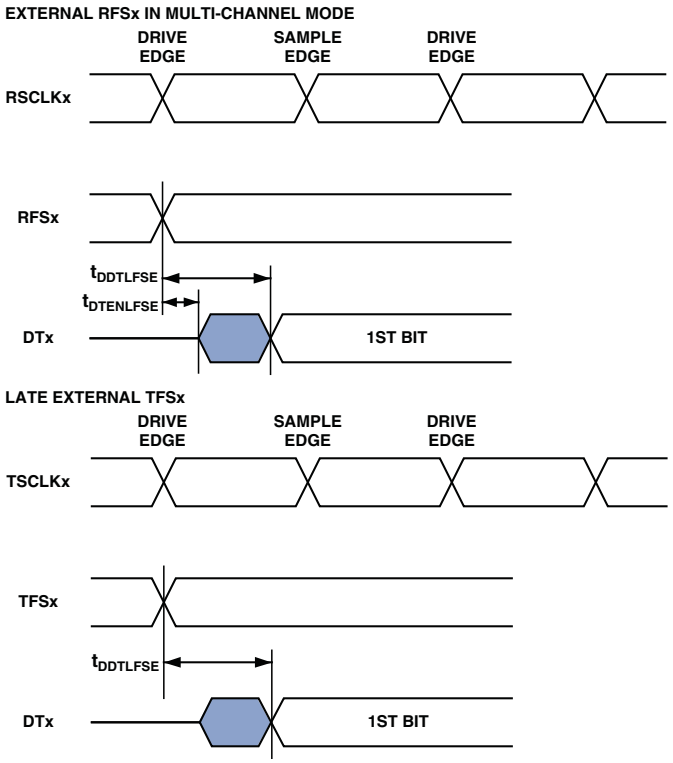


Figure 27. External Late Frame Sync

Serial Peripheral Interface Ports—Master Timing

Table 34 and Figure 28 describe SPI ports master operations.

Table 34. Serial Peripheral Interface (SPI) Ports—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCKx Edge (Data Input Setup)	9.0		ns
t_{HSPIDM}	SCKx Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPIxSELy}$ Low to First SCKx edge	$2t_{SCLK}$ –1.5		ns
t_{SPICHM}	Serial Clock High Period	$2t_{SCLK}$ – 1.5		ns
t_{SPICLM}	Serial Clock Low Period	$2t_{SCLK}$ – 1.5		ns
t_{SPICLK}	Serial Clock Period	$4t_{SCLK}$ –1.5		ns
t_{HDSM}	Last SCKx Edge to $\overline{SPIxSELy}$ High	$2t_{SCLK}$ – 1.5		ns
t_{SPITDM}	Sequential Transfer Delay	$2t_{SCLK}$ – 1.5		ns
$t_{DDSPIDM}$	SCKx Edge to Data Out Valid (Data Out Delay)		5	ns
$t_{HDSPIDM}$	SCKx Edge to Data Out Invalid (Data Out Hold)	–1.0		ns

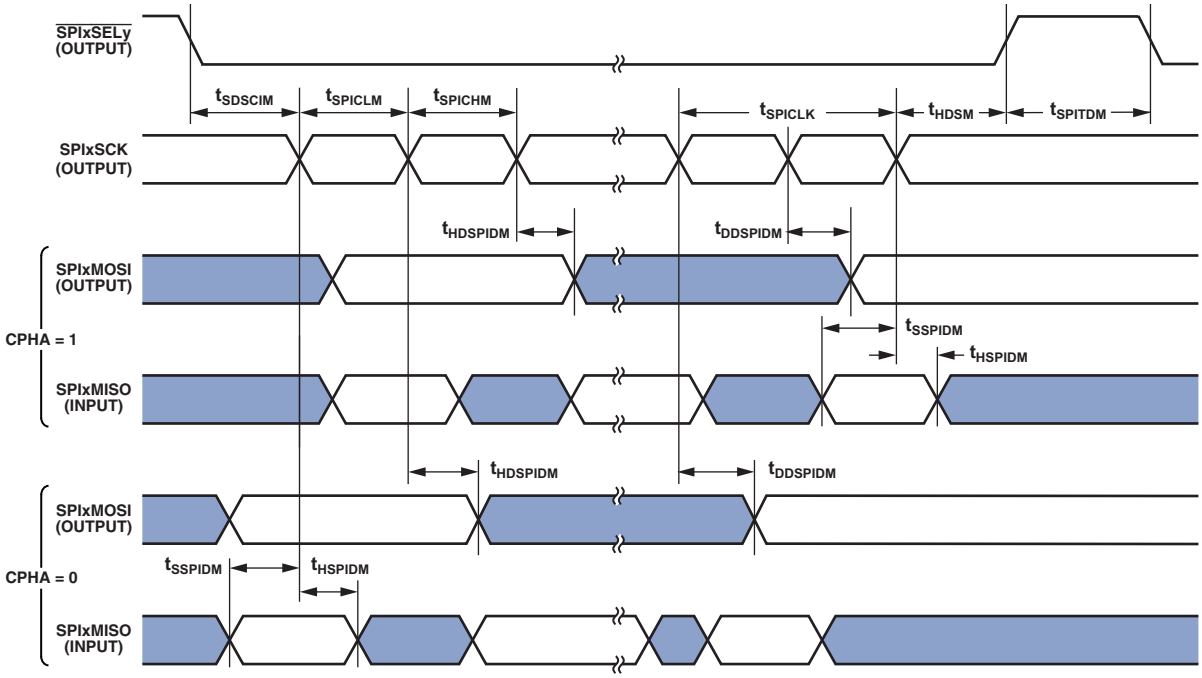


Figure 28. Serial Peripheral Interface (SPI) Ports—Master Timing

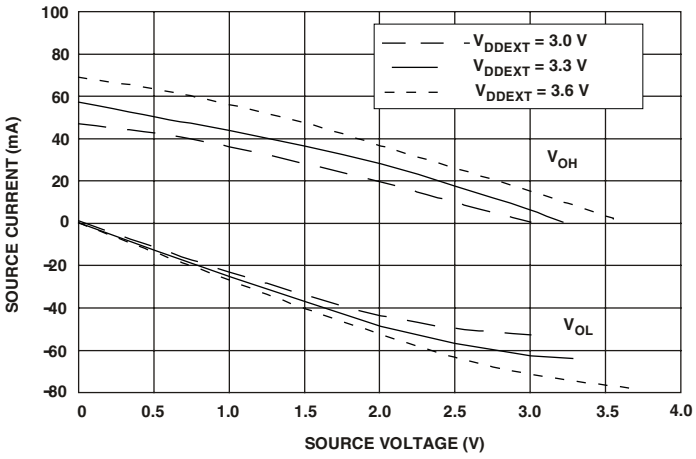


Figure 39. Drive Current C (High V_{DDEXT})

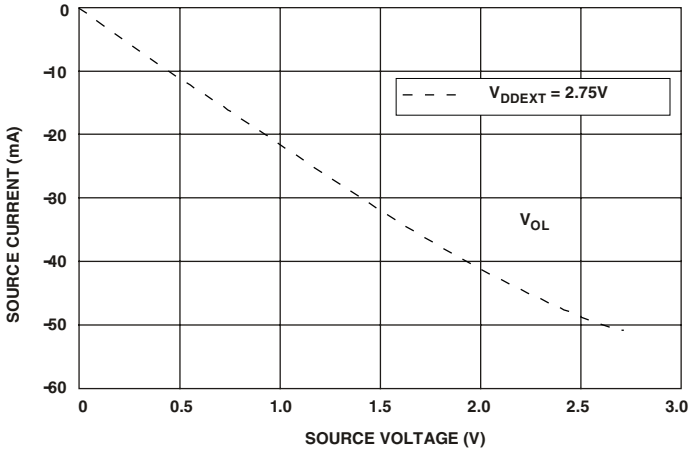


Figure 42. Drive Current E (Low V_{DDEXT})

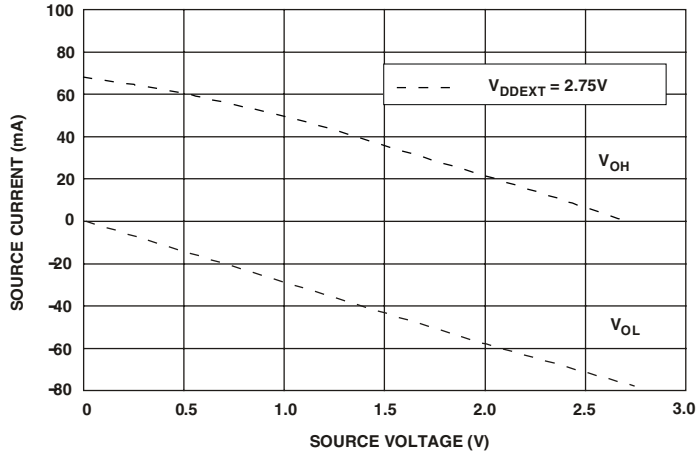


Figure 40. Drive Current D (Low V_{DDEXT})

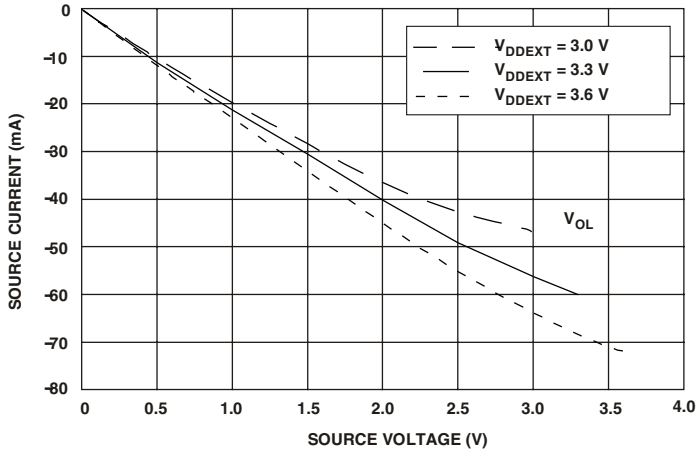


Figure 43. Drive Current E (High V_{DDEXT})

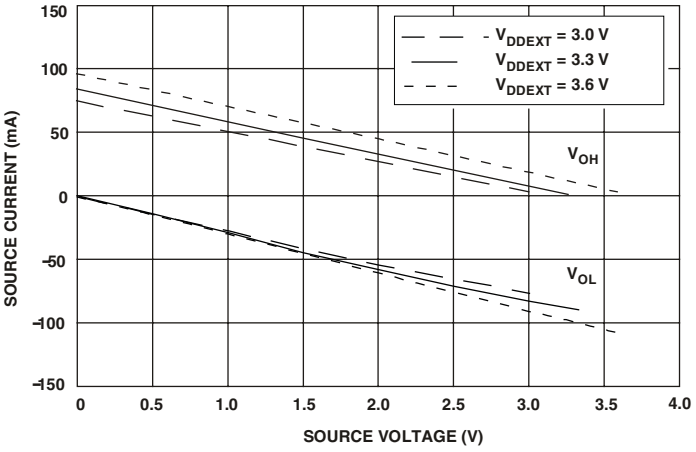


Figure 41. Drive Current D (High V_{DDEXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 44 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 1.5 V for V_{DDEXT} (nominal) = 3.3 V.

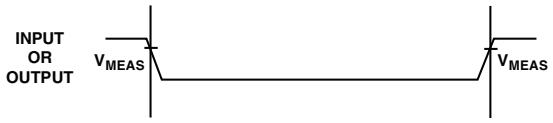


Figure 44. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 45 on Page 52.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). V_{TRIP}(high) is 2.0 V and V_{TRIP}(low) is 1.0 V for V_{DDEXT} (nominal) = 3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 45.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V for V_{DDEXT} (nominal) = 3.3 V.

The time $t_{DIS+\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

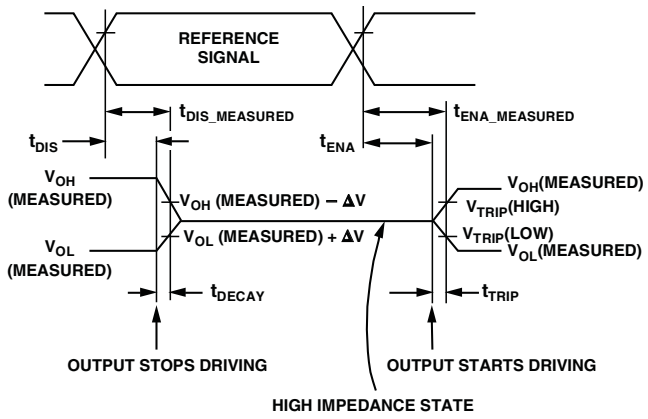


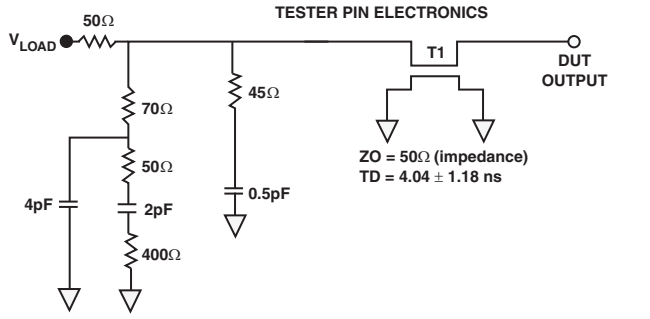
Figure 45. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF539/ADSP-BF539F processor output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 31 (for example, t_{DSDAT} for an SDRAM write cycle as shown in Table 26 on Page 36).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 46). V_{LOAD} is 1.5 V for V_{DDEXT} (nominal) = 3.3 V. Figure 47 on Page 53 through Figure 56 on Page 54 show how output rise and fall times vary with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 46. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

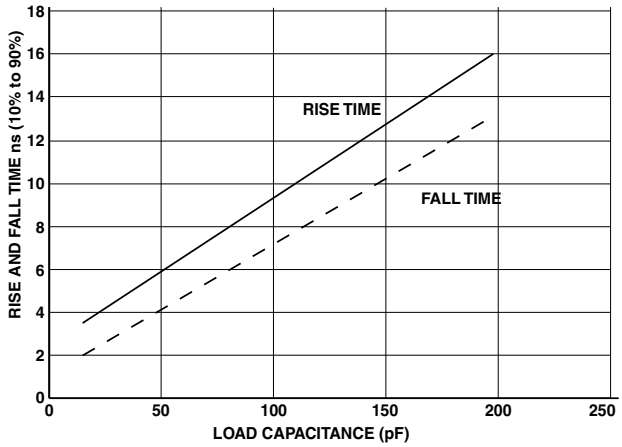


Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.7 V (Min)

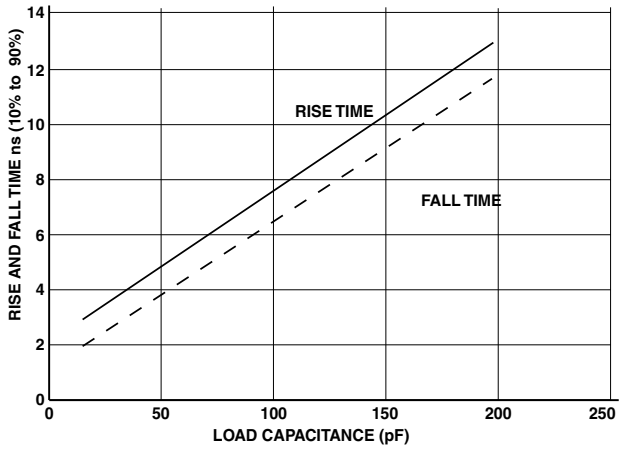


Figure 54. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.65 V (Max)

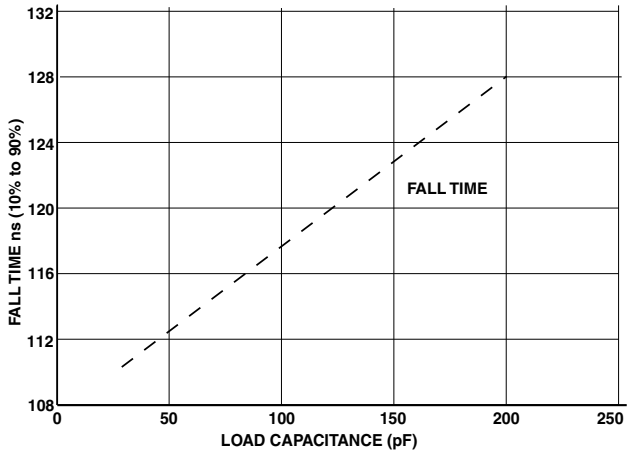


Figure 55. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 2.7 V (Min)

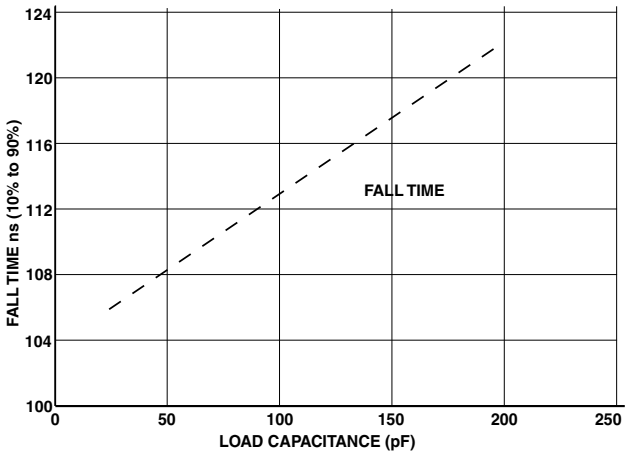


Figure 56. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 3.65 V (Max)

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 42 or Table 43

P_D = power dissipation (see Electrical Characteristics on Page 27 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 42 and Table 43, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 42. Thermal Characteristics BC-316 Without Flash

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	25.4	°C/W
θ_{JMA}	1 linear m/s air flow	22.8	°C/W
θ_{JMA}	2 linear m/s air flow	22.0	°C/W
θ_{JC}		6.7	°C/W
Ψ_{JT}	0 linear m/s air flow	0.18	°C/W
Ψ_{JT}	1 linear m/s air flow	0.38	°C/W
Ψ_{JT}	2 linear m/s air flow	0.40	°C/W

Table 43. Thermal Characteristics BC-316 With Flash

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	24.3	°C/W
θ_{JMA}	1 linear m/s air flow	21.8	°C/W
θ_{JMA}	2 linear m/s air flow	21.0	°C/W
θ_{JC}		6.3	°C/W
Ψ_{JT}	0 linear m/s air flow	0.17	°C/W
Ψ_{JT}	1 linear m/s air flow	0.36	°C/W
Ψ_{JT}	2 linear m/s air flow	0.38	°C/W