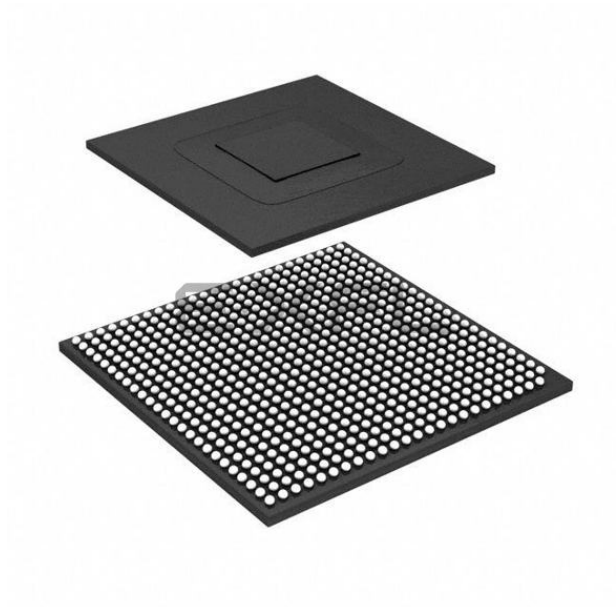

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s7cvm08ab

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 6 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6 shows the absolute maximum operating ratings.

Table 6. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.4	V
VDD_HIGH_IN supply voltage (LDO enabled)	VDD_HIGH_IN	-0.3	3.7	V
VDD_HIGH_IN supply voltage (LDO bypass)	VDD_HIGH_IN	-0.3	2.85	V
VDD_HIGH_CAP supply output voltage	VDD_HIGH_CAP	-0.3	2.6	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI and PCIe high PHY VPH supply voltage	HDMI_VPH PCIE_VPH	-0.3	2.85	V
HDMI and PCIe low PHY VP supply voltage	HDMI_VP PCIE_VP	-0.3	1.4	V
LVDS and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMII I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 9 shows the interface frequency requirements.

Table 9. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 9 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For XTALOSC_RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is used

The choice of a clock source must be based on real-time clock use and precision timeout.

only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals must not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have three basic modes:

- Bypass. The regulation FET is switched fully on passing the external voltage, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, LVDS Phy, HDMI Phy, MIPI Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual (IMX6SDLRM).

Table 32 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 32. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 33 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 33. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

[1] t is the maximum EIM logic (ACLK_EXSC) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 104 MHz.

—Variable latency for read only is 104 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz ACLK_EXSC, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 13 to Figure 16 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

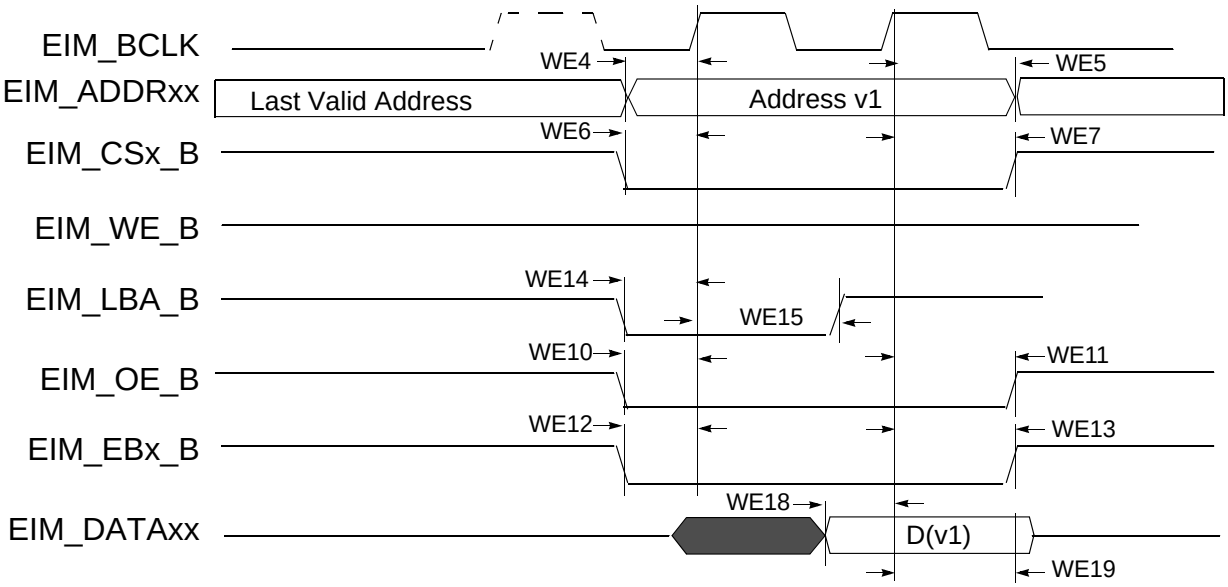

Figure 13. Synchronous Memory Read Access, WSC=1

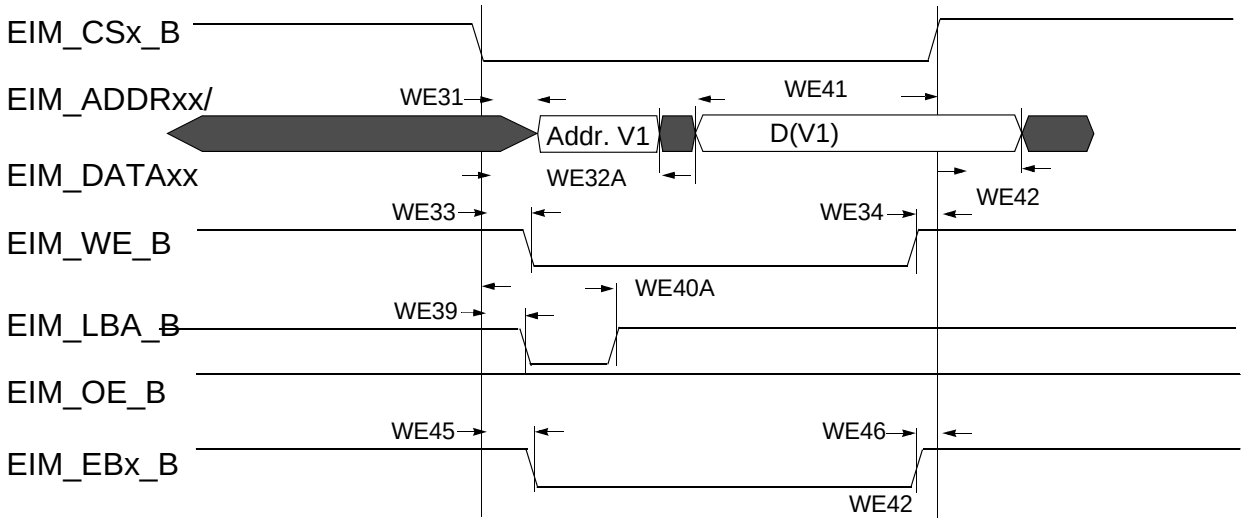

Figure 20. Asynchronous A/D Muxed Write Access

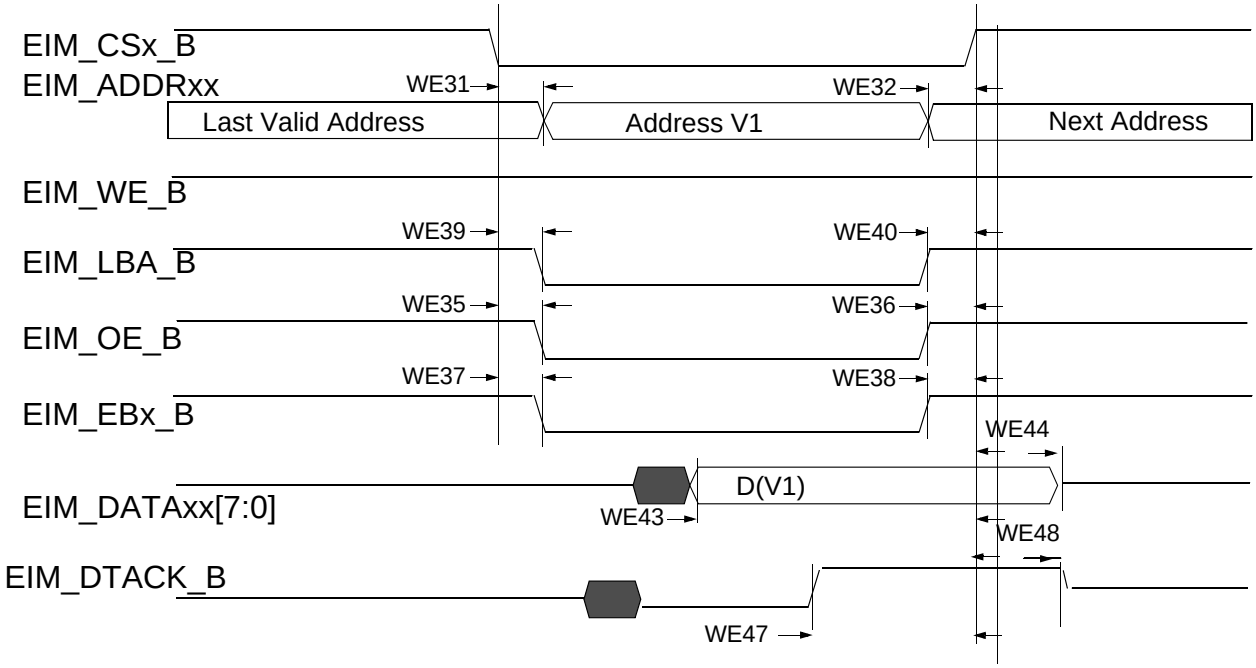

Figure 21. DTACK Mode Read Access (DAP=0)

Table 40. i.MX 6DualLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2 (Dual channel)	LPDDR2 (Single channel)	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz	400 MHz
Bus width	32-bit per channel	16/32-bit	16/32/64-bit	16/32/64-bit
Channel	Dual	Single	Single	Single
Chip selects	2 per channel	2	2	2

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 23 through Figure 26 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 41 describes the timing parameters (NF1–NF17) that are shown in the figures.

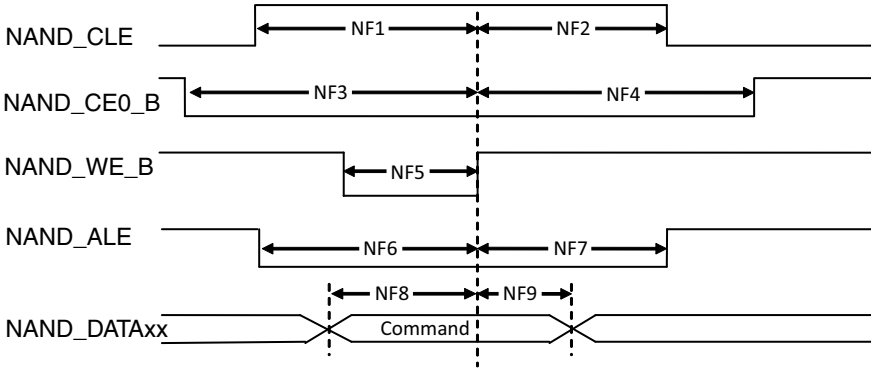

Figure 23. Command Latch Cycle Timing Diagram

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible),” for details.

4.10.3.2 Read and Write Timing

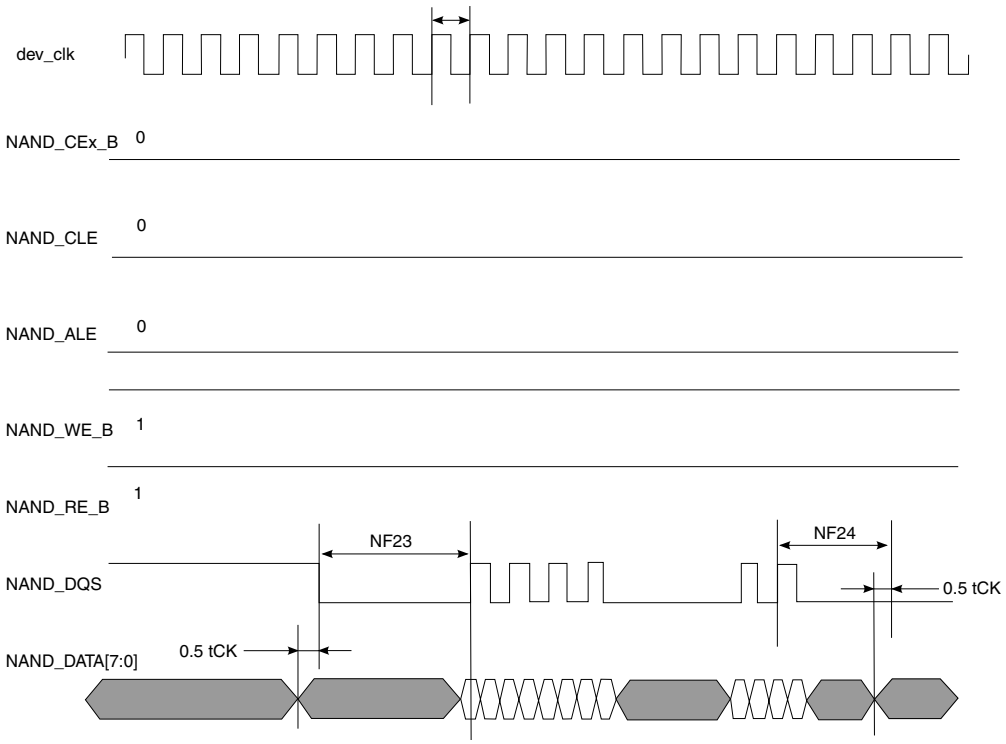

Figure 32. Samsung Toggle Mode Data Write Timing

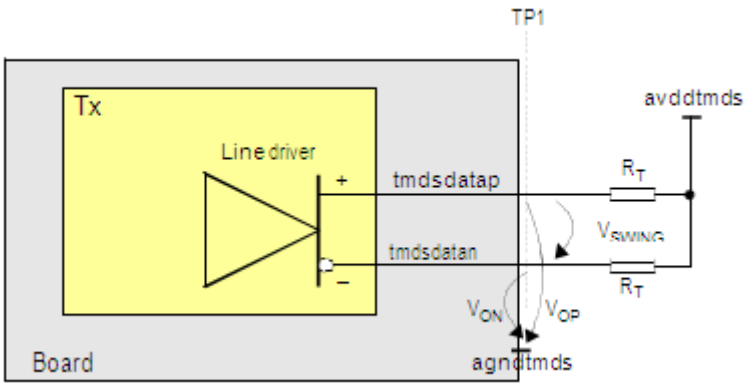

Figure 49. Driver Measuring Conditions

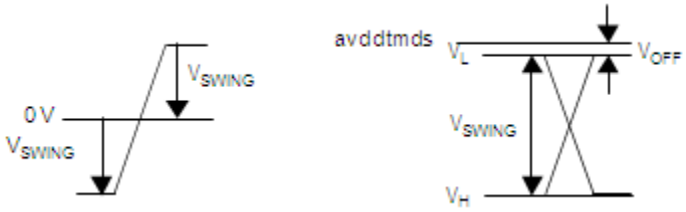

Figure 50. Driver Definitions

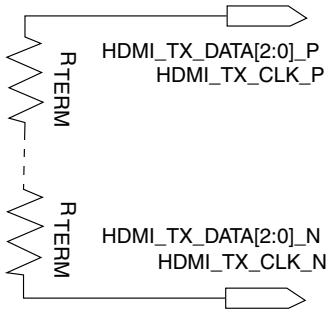

Figure 51. Source Termination

Table 56. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V
R_T	Termination resistance	—	45	50	55	Ω

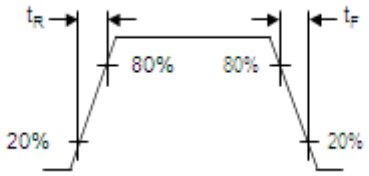

Figure 56. TMDS Output Signals Rise and Fall Time Definition

Table 57. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 52.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 52.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 52.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 52.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 54.	—	—	0.15	UI[1]
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 55.	—	—	1	UI[1]
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 56.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 56.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%

1 UI means TMDS clock unit.

2 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 59 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 59. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_ DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_ DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_ DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_ DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPUx_CSIx_ DATA05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_ DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_ DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_ DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_ DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_ DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_ DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_ DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]

4.11.10.3 Electrical Characteristics

Figure 60 depicts the sensor interface timing. IPUx_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 60 lists the sensor interface timing characteristics.

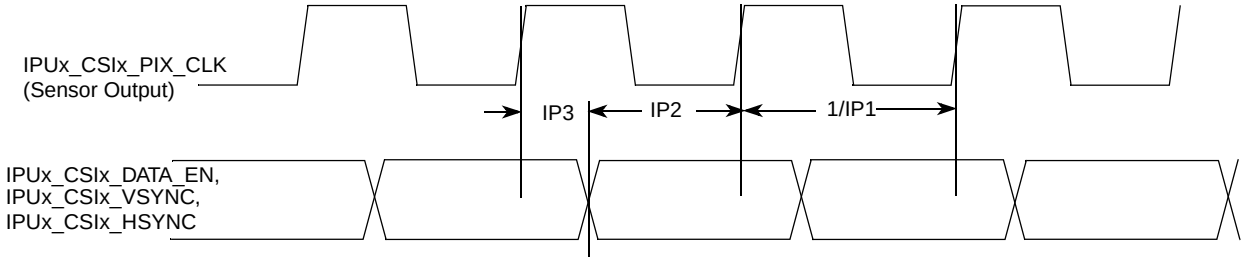

Figure 60. Sensor Interface Timing Diagram

Table 60. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 61 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 61. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

Table 61. Video Signal Cross-Reference (continued)

i.MX 6Solo/6DualLite	LCD						Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)					
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
DIx_PIN4	—						Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—						
DIx_PIN6	—						
DIx_PIN7	—						
DIx_PIN8	—						
DIx_D0_CS	—						—
DIx_D1_CS	—						Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—						—
DIx_PIN12	—						—
DIx_PIN13	—						Register select signal
DIx_PIN14	—						Optional RS2
DIx_PIN15	DRDY/DV						Data validation/blank, data enable
DIx_PIN16	—						Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q						

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 61 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

Table 69. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.11.17 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 70 and Figure 85 and Figure 86 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 70. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

4.11.19 UART I/O Configuration and Timing Parameters

4.11.19.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Solo/6DualLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 76 shows the UART I/O configuration based on the enabled mode.

Table 76. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_ B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.19.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.19.2.1 UART Transmitter

Figure 91 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 77 lists the UART RS-232 serial mode transmit timing characteristics.

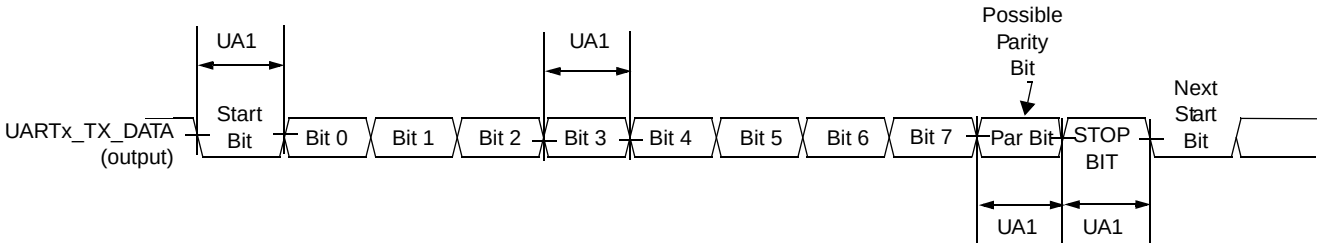

Figure 91. UART RS-232 Serial Mode Transmit Timing Diagram

Table 77. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

6.2.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 86 shows supplies contact assignments for the 21 x 21 mm package.

Table 86. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	—
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	—
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 87. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	EIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	EIM_CS0	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	EIM_CS1	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	GPIO3_IO16	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	GPIO3_IO17	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	GPIO3_IO18	Input	100 kΩ pull-up
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	GPIO3_IO19	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	GPIO3_IO20	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	GPIO3_IO21	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	GPIO3_IO22	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	GPIO3_IO23	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	GPIO3_IO24	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	GPIO3_IO25	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	GPIO3_IO26	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	GPIO3_IO27	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	GPIO3_IO28	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	GPIO3_IO29	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	GPIO3_IO30	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	GPIO3_IO31	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	EIM_AD00	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	EIM_AD01	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	EIM_AD10	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	EIM_AD11	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	EIM_AD12	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	EIM_AD13	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	EIM_AD14	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	EIM_AD15	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	EIM_AD02	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	EIM_AD03	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	EIM_AD04	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	EIM_AD05	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	EIM_AD06	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	EIM_AD07	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	EIM_AD08	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	EIM_AD09	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	EIM_EB0	Output	High

Table 87. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	100 kΩ pull-down
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	100 kΩ pull-up
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	100 kΩ pull-up

Table 90. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

	AE	AD	AC	AB	AA	
1	GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	1
2	DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	2
3	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N	3
4	DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P	4
5	DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3	5
6	DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10	6
7	DRAM_D11	GND	DRAM_D15	DRAM_D16	GND	7
8	DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17	8
9	DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23	9
10	DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND	10
11	DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1	11
12	DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14	12
13	DRAM_A5	GND	DRAM_A6	DRAM_A8	GND	13
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2	14
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10	15
16	DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND	16
17	ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32	17
18	DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33	18
19	DRAM_D35	GND	DRAM_D39	DRAM_D38	GND	19
20	DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45	20
21	DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57	21
22	DRAM_D49	GND	DRAM_D48	DRAM_D52	GND	22
23	DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61	23
24	DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B	24
25	GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7	25
	AE	AD	AC	AB	AA	

Table 92. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
Rev. 4	12/2014	• Figure 1, “Part Number Nomenclature—i.MX 6Solo and 6DualLite”: Added Silicon Rev 1.3. to diagram • Table 2, Modules List, UART 1–5 Description changed: baud rate up from 5MHz to 5Mbps. • Added Figure 2, "Example Part Marking for Revision 1.2/1.3 Devices," on page 4. • Section 1.2, “Features”: under, *Miscellaneous IPs and interfaces*: Changed *UARTs* bullet, from “up to 4.0 Mbps”, to “up to 5.0 Mbps”. • Table 8, “Operating Ranges,” on page 29: — Changed *Run mode: VDD_ARM_IN* minimum value from 1.05 to 1.125V; for operation up to 396 MHz. and changed *LDO bypassed* maximum value from 1.225V to 1.21V; for *VDD_SOC_IN*. — Changed *PCIe supply voltages; PCIE_VP/PCIE_VPTX* maximum value from 1.225V to 1.21V • Table 10, "Maximum Supply Currents," on page 28; — Changed *VDD_ARM_IN* from single condition to include DualLite and Solo conditions with Maximum current values of 2200 and 1320 mA, respectively. — Added footnote for NVCC_LVDS2P5 supply. • Table 38, “Reset Timing Parameters”: Removed footnote regarding SRC_POR_B rise and fall times. • Section 4.9.3, “External Interface Module (EIM)”: Changed first paragraph to describe two systems clocks used with EIM: ACLK_EIM_SLOW_CLK_ROOT and ACLK_EXSC (for synchronous mode). • Table 31, “DDR I/O DDR3/DDR3L Mode AC Parameters”; Added footnote about extended range for Vix. • Table 48, “DDR3/DDR3L Timing Parameter Table,” on page 76; Added DDR0, tCK(avg) and parameter values. Changed symbol names DDR1 through DDR7 to include avg or base; changed minimum parameter values for DDR4–DDR7. Added footnote about tIS and tIH base values. • Figure 25, “DDR3 Command and Address Timing Parameters,” on page 76; Added DDR0. • Table 49, “DDR3/DDR3L Write Cycle,” on page 77; Changed symbol names of DDR17 and DDR18 to include base(AC150/DC100); Changed Units from tCK to tCK(avg). • Table 46, “LPDDR2 Write Cycle,” on page 64; Changed LP21 min/max parameter values from -0.25/+0.25 to 0.75/1.25. • Table 37, "EIM Bus Timing Parameters," on page 51: Changed footnotes regarding the system clocks used with EIM: from *axi_clk* to *ACLK_EXSC* or *ACLK_EIM_SLOW_CLK_ROOT.* • Table 49, “DDR3/DDR3L Write Cycle,” on page 77: Changed *DDR17* minimum value from 420 ps to 125 ps and *DDR18* from 345 ps to 150 ps. • Table 49, “DDR3/DDR3L Write Cycle,” on page 77: Added footnote 4. • Table 64, "LVDS Display Bridge (LDB) Electrical Specification," on page 101: Corrected Units for Output Voltage High and Output Voltage Low from mV to V. • Table 66, "Electrical and Timing Information," on page 104: Moved rows *tSETUP[RX]* and *tHOLD[RX]* to be directly under *HS Line Receiver AC Specifications* heading row. • Table 86, "21 x 21 mm Supplies Contact Assignments," on page 132: Removed A1 pin. • Table 87, "21 x 21 mm Functional Contact Assignments," on page 134: Moved rows *DRAM_4*, *DRAM_5,* and *DRAM_6* out of the i.MX 6DualLite section (shaded gray) to the i.MX 6Solo section above DRAM_7 and (unshaded). • Table 89, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo," on page 147: Removed “NC” from A1 pin location. • Table 90, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite," on page 150: Removed “NC” from A1 pin location.