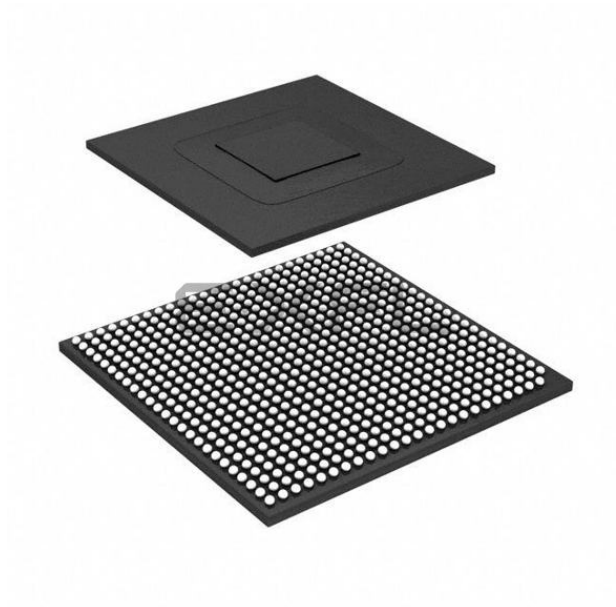

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s7cvm08ac

The i.MX 6Solo/6DualLite processors are specifically useful for applications such as:

- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Video processing and display
- Portable medical
- Home energy management systems
- Industrial control and automation

The i.MX 6Solo/6DualLite applications processors feature:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), a programmable smart DMA (SDMA) controller, and an asynchronous sample rate converter.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller two CAN ports, ESAI audio interface, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6Solo/6DualLite Security Reference Manual* (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on the web page nxp.com/imx6series. If the desired part number is not listed in Table 1, go to nxp.com/imx6series or contact a NXP representative for details.

Table 1. Example Orderable Part Numbers

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade[1]	Temperature Grade	Package
MCIMX6U7CVM08AB	DualLite	With VPU, GPU, no EPDC, no MLB 2x ARM Cortex-A9 64-bit DDR	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U7CVM08AC	DualLite	With VPU, GPU, no EPDC, no MLB 2x ARM Cortex-A9 64-bit DDR	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S7CVM08AB	Solo	With VPU, GPU, no EPDC, no MLB 1x ARM Cortex-A9 32-bit DDR	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S7CVM08AC	Solo	With VPU, GPU, no EPDC, no MLB 1x ARM Cortex-A9 32-bit DDR	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

1 If a 24 MHz clock is used (required for USB), then the maximum SoC speed is limited to 792 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of a specific part number (for example, cores, frequency, temperature grade, fuse options, and silicon revision).

The primary characteristic that differentiates which data sheet applies to a specific part is the temperature grade (junction) field. The following list describes the correct data sheet to use for a specific part:

- The *i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors* data sheet (IMX6SDLAEC) covers parts listed with an “A (Automotive temp)”
- The *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* data sheet (IMX6SDLCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”
- The *i.MX 6Solo/6DualLite Applications Processors for Industrial Products* data sheet (IMX6SDLIEC) covers parts listed with “C (Industrial temp)”

For more information go to nxp.com/imx6series or contact a NXP representative for details.

4.1.3 Operating Ranges

Table 8 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (*IMX6SDLRM*)*.

Table 8. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN	1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.150 V minimum for operation up to 792MHz.
		1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.125 V minimum for operation up to 396MHz.
	VDD_SOC_IN	1.275[3,4]	—	1.5	V	VPU ≤ 328 MHz, VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) = 1.225 V[5] maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.125	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDD_SOC_IN	1.150[6]	—	1.21[5]	V	LDO bypassed for operation VPU ≤ 328 MHz
Standby/DSM mode	VDD_ARM_IN	0.9	—	1.3	V	Refer to Table 11, "Stop Mode Current and Power Consumption," on page 29.
	VDD_SOC_IN	0.9	—	1.225[5]	V	—
VDD_HIGH internal regulator	VDD_HIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[7]	2.9	—	3.3	V	Must be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
Supply for RGMII I/O power group[8]	NVCC_RGMII	1.15	—	2.625	V	1.15 V–1.30 V in HSIC 1.2 V mode 1.43 V–1.58 V in RGMII 1.5 V mode 1.70 V–1.90 V in RGMII 1.8 V mode 2.25 V–2.625 V in RGMII 2.5 V mode

Table 13. PCIe PHY Current Drain (continued)

Mode	Test Conditions	Supply	Max Current	Unit
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.9 HDMI Power Consumption

Table 14 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 14. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 11, Figure 12, and Table 37 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

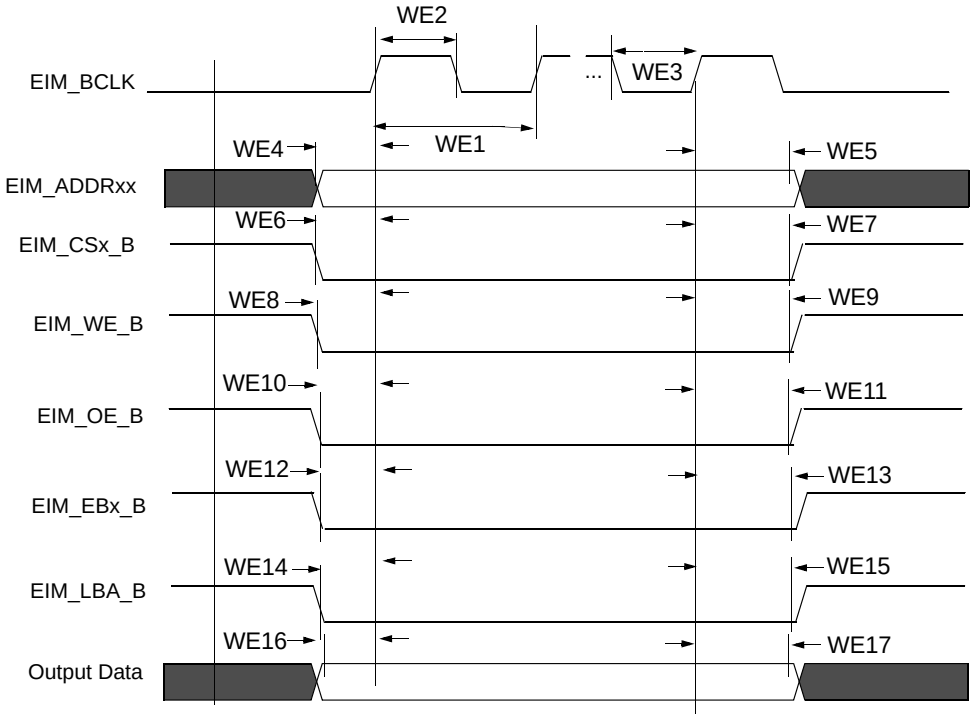

Figure 11. EIM Outputs Timing Diagram

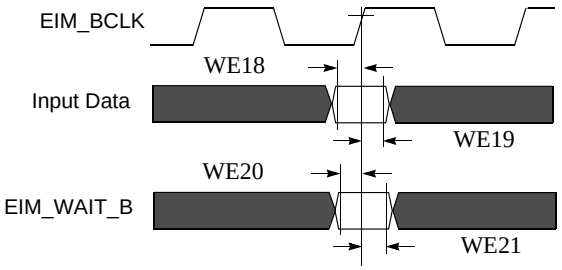

Figure 12. EIM Inputs Timing Diagram

[1] t is the maximum EIM logic (ACLK_EXSC) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 104 MHz.

—Variable latency for read only is 104 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz ACLK_EXSC, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 13 to Figure 16 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

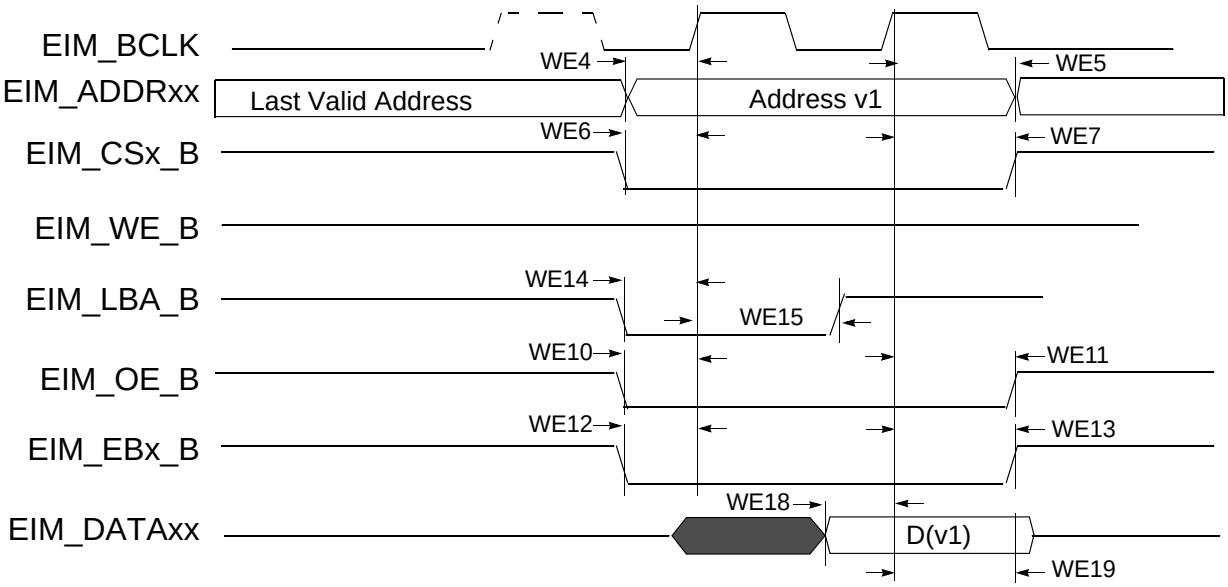

Figure 13. Synchronous Memory Read Access, WSC=1

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 46 shows the interface timing values. The number field in the table refers to timing signals found in Figure 36 and Figure 37.

Table 46. Enhanced Serial Audio Interface (ESAI) Timing Parameters

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

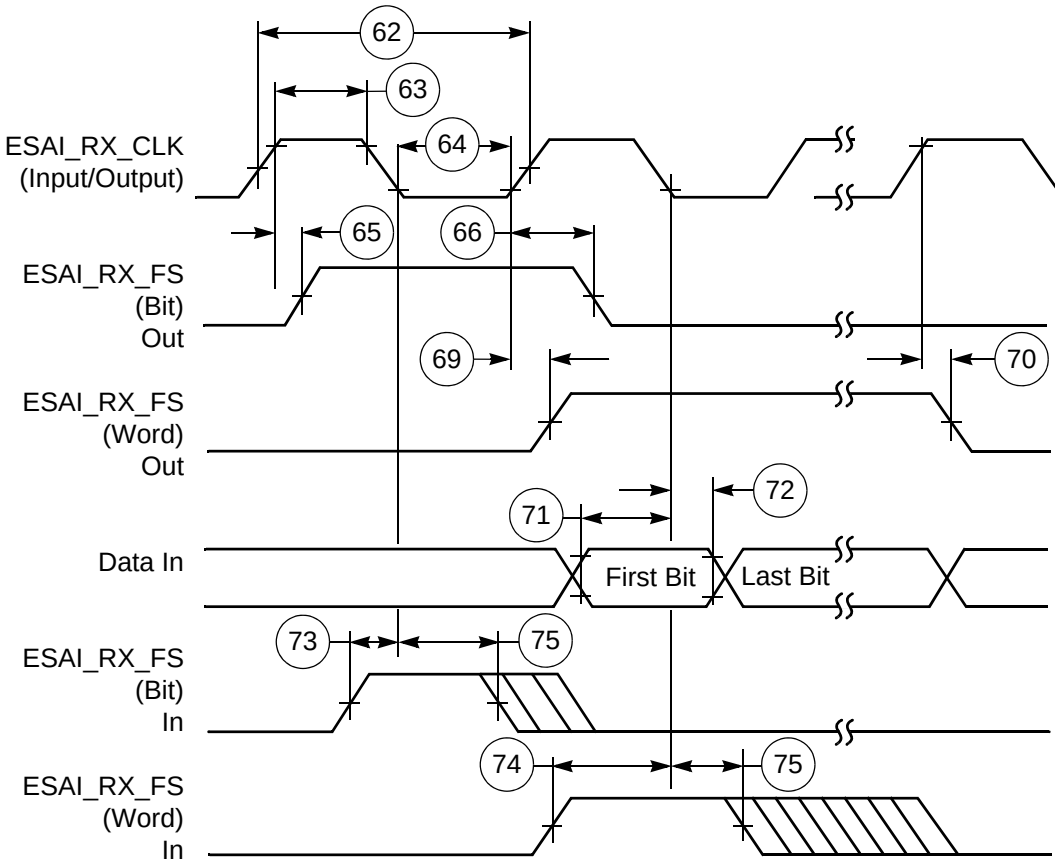

Figure 37. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 38 depicts the timing of SD/eMMC4.3, and Table 47 lists the SD/eMMC4.3 timing characteristics.

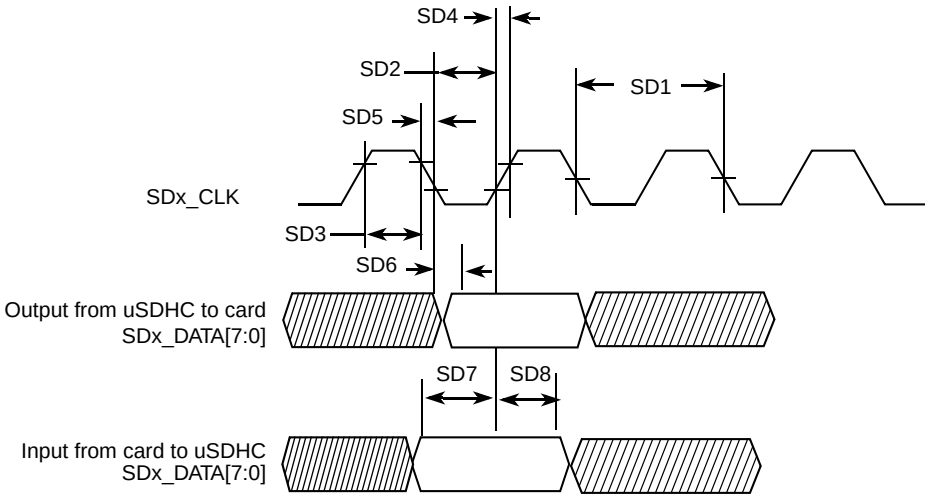

Figure 38. SD/eMMC4.3 Timing

Table 47. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 42 shows MII transmit signal timings. Table 51 describes the timing parameters (M5–M8) shown in the figure.

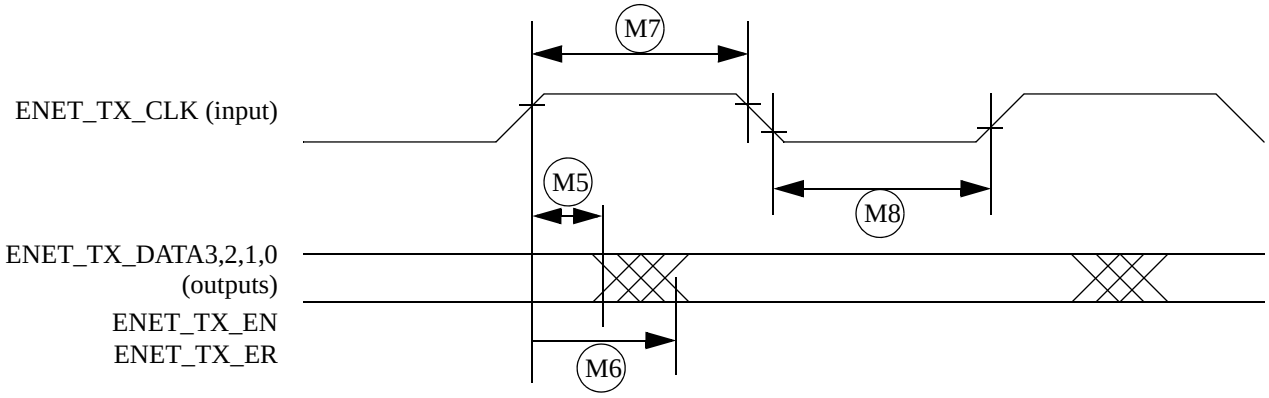

Figure 42. MII Transmit Signal Timing Diagram

Table 51. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 43 shows MII asynchronous input timings. Table 52 describes the timing parameter (M9) shown in the figure.

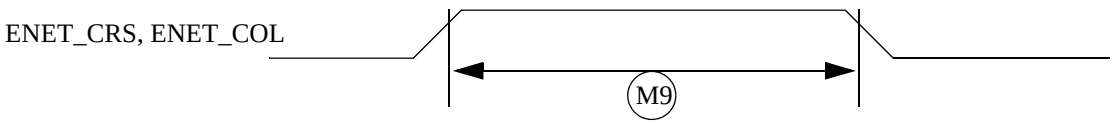

Figure 43. MII Async Inputs Timing Diagram

Table 55. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

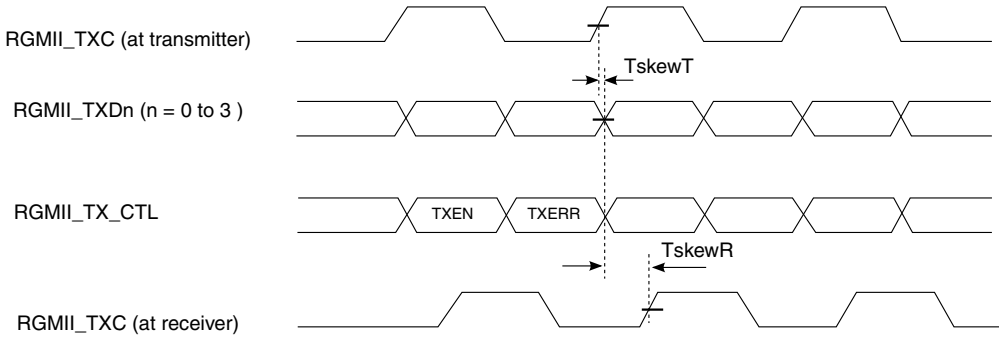

Figure 46. RGMII Transmit Signal Timing Diagram Original

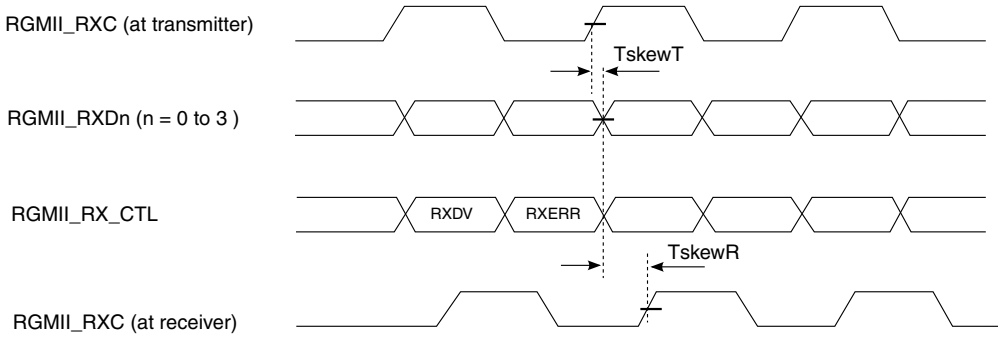

Figure 47. RGMII Receive Signal Timing Diagram Original

4.11.12.3 MIPI HS Line Driver Characteristics

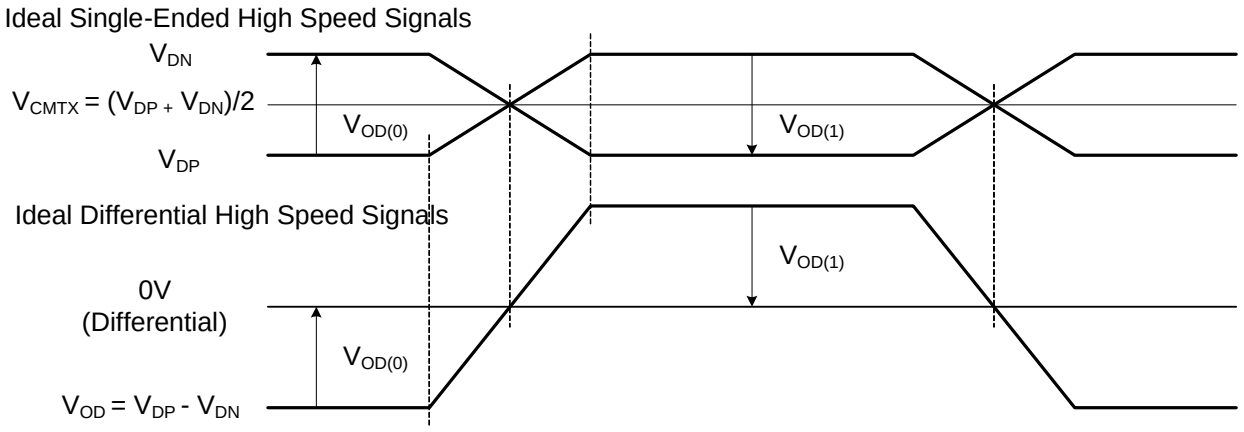

Figure 66. Ideal Single-ended and Resulting Differential HS Signals

4.11.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

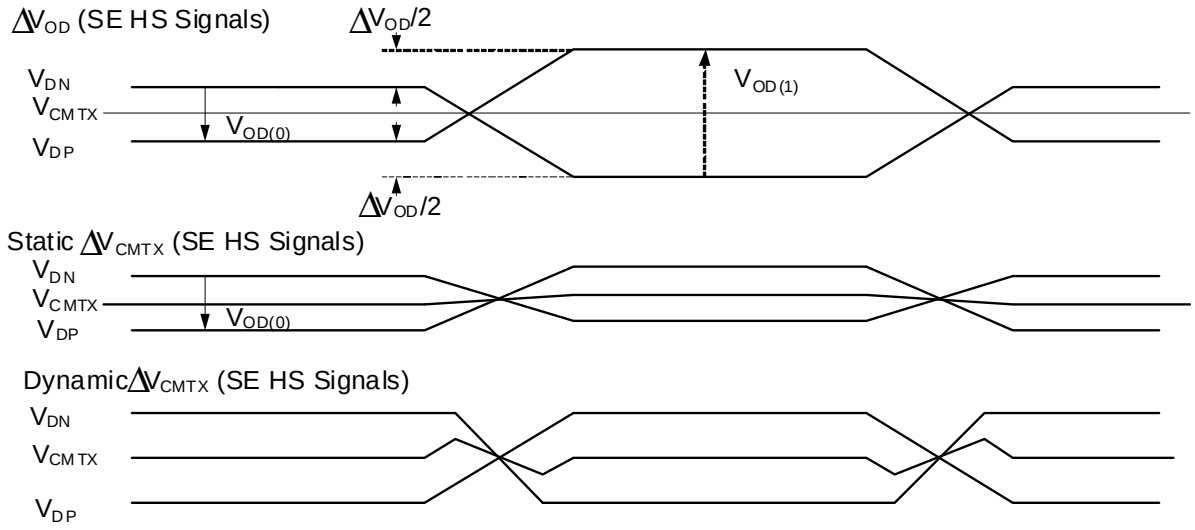

Figure 67. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 66. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps

4.11.13.2 Pipelined Data Flow

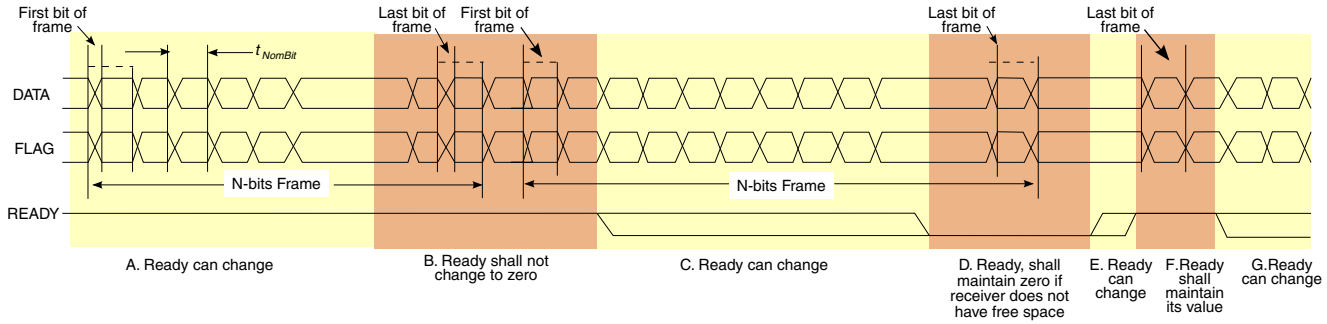

Figure 73. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

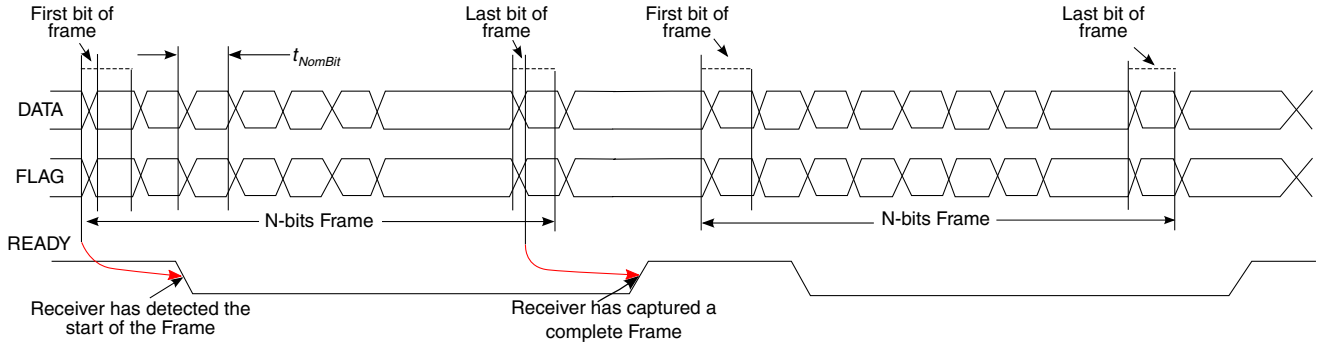

Figure 74. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

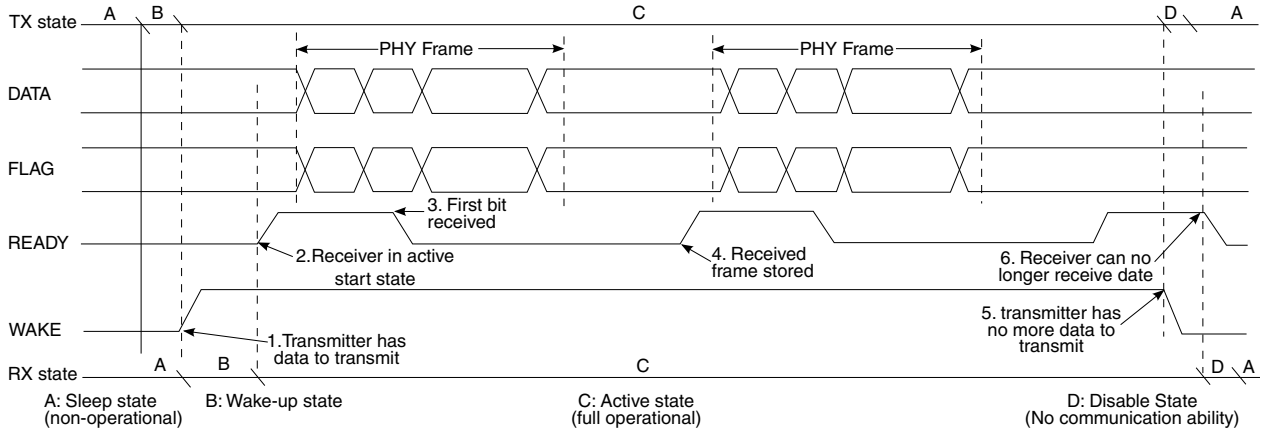

Figure 75. Synchronized Data Flow Transmission with WAKE

4.11.18.1 SSI Transmitter Timing with Internal Clock

Figure 87 depicts the SSI transmitter internal clock timing and Table 72 lists the timing parameters for the SSI transmitter internal clock.

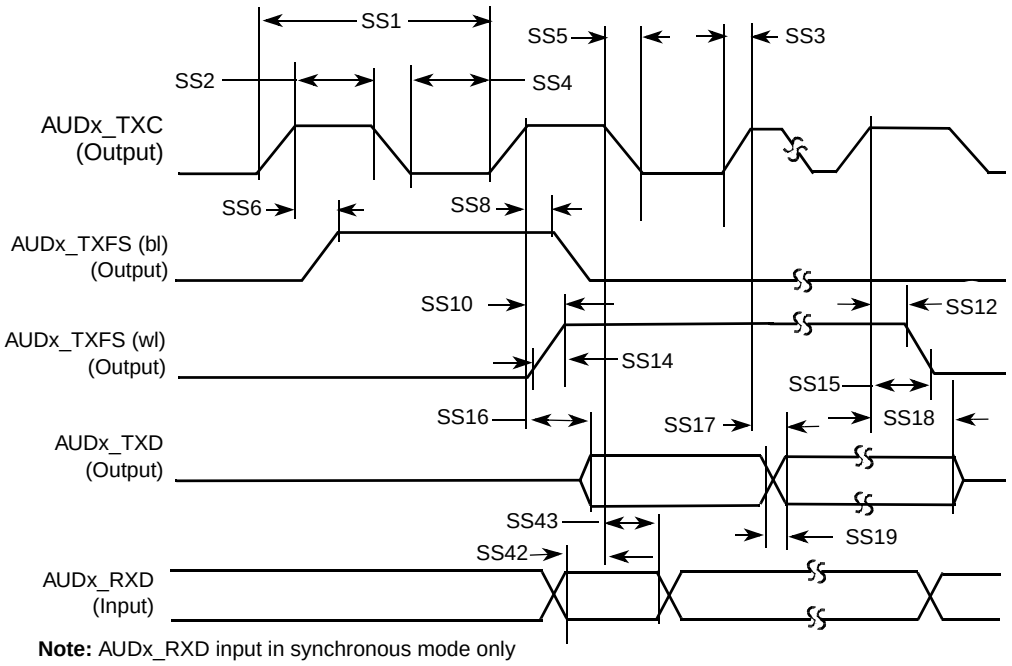

Figure 87. SSI Transmitter Internal Clock Timing Diagram

Table 72. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

4.11.18.3 SSI Transmitter Timing with External Clock

Figure 89 depicts the SSI transmitter external clock timing and Table 74 lists the timing parameters for the transmitter timing with the external clock.

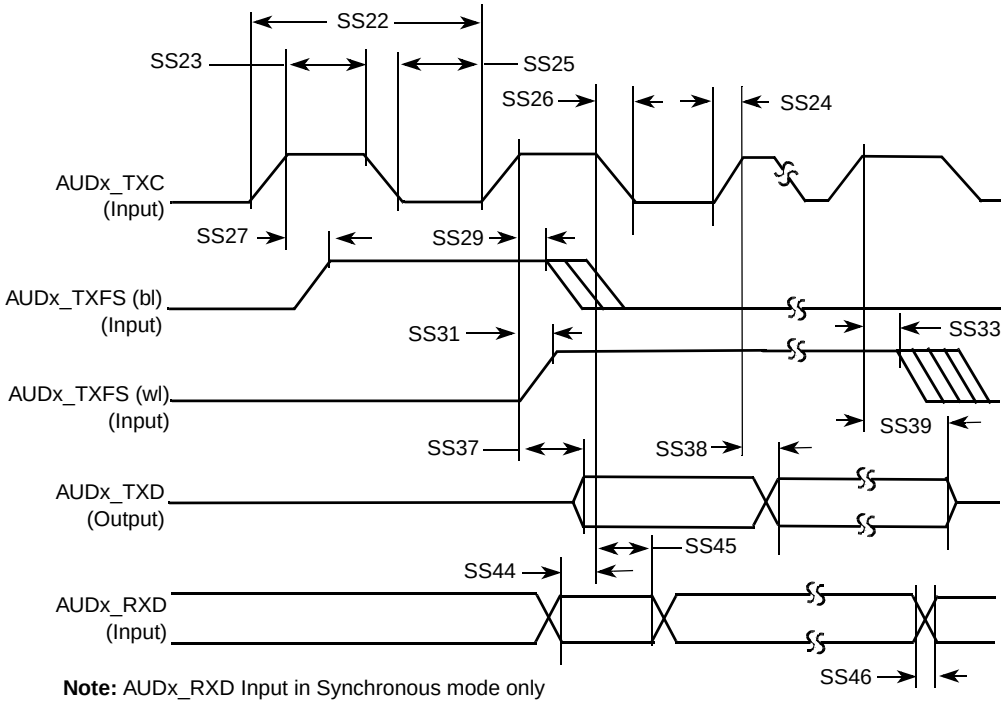

Figure 89. SSI Transmitter External Clock Timing Diagram

Table 74. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	-10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	-10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 74. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.18.4 SSI Receiver Timing with External Clock

Figure 90 depicts the SSI receiver external clock timing and Table 75 lists the timing parameters for the receiver timing with the external clock.

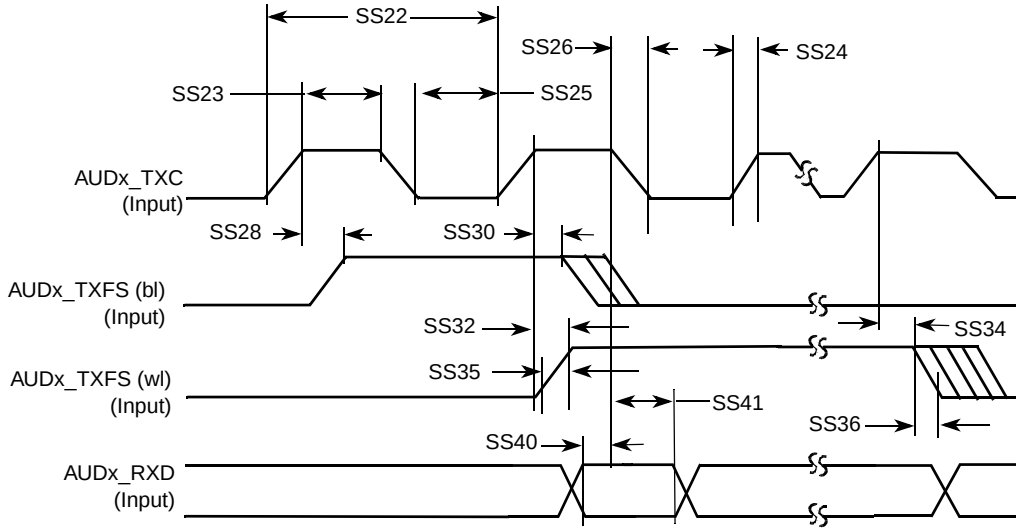

Figure 90. SSI Receiver External Clock Timing Diagram

UART IrDA Mode Receiver

Figure 94 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 80 lists the receive timing characteristics.

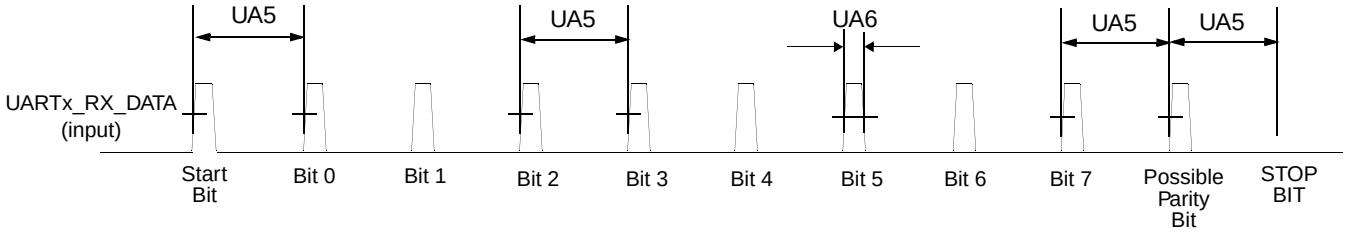

Figure 94. UART IrDA Mode Receive Timing Diagram

Table 80. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.20 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.20.1 Transmit Timing

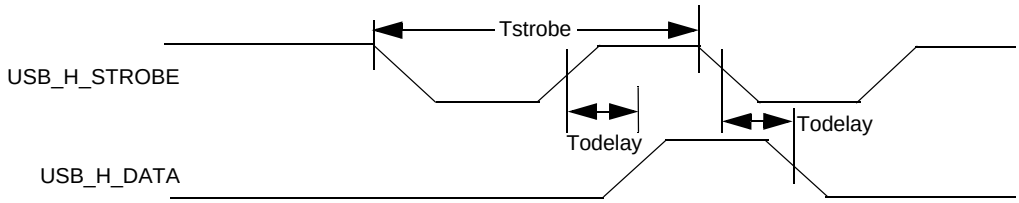

Figure 95. USB HSIC Transmit Waveform

Table 81. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

6.2.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 89 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 89. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	NC	NC	NC	NC	GND	NC	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND	A
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	NC	NC	NC	NC	SD3_CMD	NC	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC	B
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	NC	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16	C
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23	D
E	NC	NC	CSI_D0P	CSI_D0M	GND	GND	GND	NVCC_PLL_OUT	USB_OTG_VBUS	USB_H1_DP	TAMPER	TEST_MODE	SD3_DAT6	SD3_DAT0	NANDF_WP_B	SD4_CLK	NANDF_D6	SD4_DAT4	SD1_DAT2	SD2_DAT1	RGMII_TD2	EIM_EB2	EIM_D22	EIM_D26	EIM_D27	E
F	NC	NC	CSI_CLK0P	CSI_CLK0M	GND	GND	GND	GND	VDDUSB_CAP	USB_H1_DN	PMIC_STBY_REQ	BOOT_MODE1	SD3_DAT7	SD3_DAT1	NANDF_CS0	NANDF_D2	SD4_DAT2	SD1_DAT3	SD2_CMD	RGMII_TD1	EIM_D17	EIM_D24	EIM_EB3	EIM_A22	EIM_A24	F
G	DSI_D0P	DSI_D0M	GND	DSI_REXT	JTAG_TDI	JTAG_TDO	PCIE_VPH	PCIE_VPTX	VDD_SNVS_CAP	GND	VDD_SNVS_IN	NC	NC	NVCC_SD3	NVCC_NANDF	NVCC_SD1	NVCC_SD2	NVCC_RGMII	GND	EIM_D20	EIM_D19	EIM_D25	EIM_D28	EIM_A17	EIM_A19	G

Table 89. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

	AC	AB	AA	Y	W	V	U	T	
1	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	1
2	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	2
3	DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	3
4	DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	4
5	DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	5
6	DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	6
7	DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	7
8	DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND	8
9	DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	9
10	DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	10
11	DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	11
12	DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND	12
13	DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	13
14	DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	14
15	DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	15
16	DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	16
17	DRAM_A13	DRAM_SDODT1	NC	NC	GND	NVCC_DRAM	GND	GND	17
18	NC	NC	NC	NC	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	18
19	NC	NC	GND	NC	GND	GND	GND	GND	19
20	NC	NC	NC	NC	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	20
21	NC	NC	NC	NC	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	21
22	NC	NC	GND	NC	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	22
23	NC	NC	NC	NC	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	23
24	NC	GND	NC	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	24
25	NC	NC	NC	NC	NC	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	25
	AC	AB	AA	Y	W	V	U	T	

7 Revision History

Table 91 provides the current revision history for this data sheet. Table 92 provides a revision history for previous revisions.

Table 91. i.MX 6Solo/6DualLite Data Sheet Document Rev. 7 History

Rev. Number	Date	Substantive Changes
7	10/2016	• Table 1, "Example Orderable Part Numbers," on page 3: Added footnote. • Figure 1, "Part Number Nomenclature—i.MX 6Solo and 6DualLite," on page 4: Added to Silicon Revision block: Revision 1.2 and 1.3 and associated Mask ID. • Table 6, "Absolute Maximum Ratings," on page 23: – NVCC_DRAM maximum value changed to 1.975 V. – Included footnote to NVCC_DRAM maximum value regarding maximum voltage allowance. – Added row to Vin/Vout I/O supply voltage, separating DDR pins and non-DDR pins and included footnote regarding maximum voltage allowance. • Table 8, "Operating Ranges," on page 25: Added footnotes within the Comments column for the Run Mode, LDO Enabled row; VDD_SOC_IN maximum values. • Section 4.6.3, “DDR I/O DC Parameters: Added reference for more DDR details to see the MMDC section. Moved JEDEC standard information to footnote. • Section 4.7.2, “DDR I/O AC Parameters: Added reference for more DDR details to see the MMDC section. Moved JEDEC standard information to footnote. • Table 39, "i.MX 6Solo Supported DDR3/DDR3L/LPDDR2 Configurations," on page 59: Changed LPDDR2 Channel column from “Dual” to “Single.” • Table 40, "i.MX 6DualLite Supported DDR3/DDR3L/LPDDR2 Configurations," on page 60: Added LPDDR2 Dual Channel column. • Table 85, "21 x 21, 0.8 mm BGA Package Details," on page 131: Correction to package total thickness. • Table 87, "21 x 21 mm Functional Contact Assignments," on page 134: DRAM_SDCKL*n* rows, reverted to “Low” rather than “0” in the Value column.