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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	105
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpxd1005vlq64

  - As many as 38 frontplane drivers and six backplane drivers
- Stepper Motor Controller (SMC) module with high-current drivers for as many as six stepper motors driven in full dual H-Bridge configuration including full diagnostics for short circuit detection
- Stepper motor return-to-zero and stall detection module
- Sound generation and playback utilizing PWM channels and eDMA; supports monotonic and polyphonic sound
- 24 eMIOS channels providing as many as 16 PWM and 24 input capture / output compare channels
- 10-bit Analog-to-Digital Converter (ADC)
  - Maximum conversion time of 1 µs
  - As many as 16 internal channels, expandable to 23 via external multiplexing
- As many as two Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices (extendable to include up to 8 multiplexed external channels)
- QuadSPI serial flash memory controller supporting single, dual and quad modes of operation to interface to external serial flash memory. QuadSPI can be configured to function as another DSPI module.
- Two Local Interconnect Network Flexible (LINFlex) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev 2.1
- Two full CAN 2.0B controllers with 64 configurable buffers each; bit rate programmable as fast as 1 Mbit/s
- As many as four inter-integrated circuit (I^2C) internal bus controllers with master/slave bus interface
- As many as 133 configurable general purpose pins supporting input and output operations
- Real Time Counter (RTC) with multiple clock sources:
  - 128 kHz slow internal RC oscillator or 16 MHz fast internal RC oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - 32 KHz slow external crystal oscillator, supporting wakeup with 1 s resolution and maximum timeout of one hour
  - 4–16 MHz fast external crystal oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)—included in processor platform
  - Four-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status and provides an entry point for the censorship password mechanism

1.6.4 Parallel Data Interface (PDI)

The PDI is a digital interface used to receive external digital video or graphic content into the DCU.

The PDI input is directly injected into the DCU background plane FIFO. When the PDI is activated, all the DCU synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - Embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU background plane FIFO
- Synchronization generation for the DCU

1.6.5 Liquid Crystal Display (LCD) driver

The LCD driver module has two configurations allowing a maximum of 160 or 228 LCD segments:

- As many as 40 frontplane drivers and four backplane drivers
- As many as 38 frontplane drivers and six backplane drivers

Each segment is controlled and can be masked by a corresponding bit in the LCD RAM.

Four to six multiplex modes (1/1, 1/2, 1/3, 1/4, 1/5, 1/6 duty), and three bias (1/1, 1/2, 1/3) methods are available. All frontplane and backplane pins can be multiplexed with other port functions.

The LCD driver module features the following:

- Programmable frame clock generator from different clock sources:
  - System clock
  - Internal RC oscillator
- Programmable bias voltage level selector
- On-chip generation of all output voltage levels

1.6.11 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual and quad modes of operation. It features the following:

- Memory mapping of external serial flash
- Automatic serial flash read command generation by CPU, DMA or DCU read access on AHB bus
- Supports single, dual and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash
- 'Legacy' mode allowing QuadSPI to be used as a standard SPI (no DSI or CSI mode)

1.6.12 Analog-to-digital converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0 to 5 V common mode conversion range
- Supports conversions speeds of as fast as 1 µs
- 16 internal and 8 external channels support
- As many as 16 single-ended inputs channels
  - All channels configured to have alternate function as general purpose input/output pins
    - 10-bit ±3 counts accuracy (TUE)
- External multiplexer support to increase as many as 23 channels
  - Automatic 1 × 8 multiplexer control
  - External multiplexer connected to a dedicated input channel
  - Shared register between the 8 external channels
- Result register available for every non-multiplexed channel
- Configurable left- or right-aligned result format
- Supports for one-shot, scan and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  - Supports access to result and injection status with single 32-bit read
- Independently enabling of function for channels:
  - Pre-sampling
  - Offset error cancellation
  - Offset refresh
- Conversion Triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range

1.6.16 Controller Area Network (CAN) module

The PXD10 contains two CAN modules that offer the following features:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler
  - Can catch the first message sent on the CAN network while the PXD10 is stopped. This guarantees a clean startup of the system without missing messages on the CAN network.
  - The CAN sampler is connected to one of the CAN RX pins.

1.6.17 Inter-IC Communications (I^2C) module

The I^2C module features the following:

- As many as four I^2C modules supported
- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

Table 2. 16-channel eMIOS module channel configuration

Channel mode	Channel number				
	8 IC/OC Counter	9–15 IC/OC	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X	X	X
Single Action Input Capture	X	X	X	X	X
Single Action Output Compare	X	X	X	X	X
Modulus Counter Buffered[1]	X		X		X
Output Pulse Width and Frequency Modulation Buffered			X	X	X
Output Pulse Width Modulation Buffered			X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

The channel configuration options for the 8-channel eMIOS module are summarized in Table 3.

Table 3. 8-Channel eMIOS module channel configuration

Channel mode	Channel number		
	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X
Single Action Input Capture	X	X	X
Single Action Output Compare	X	X	X
Modulus Counter Buffered[1]	X		X
Output Pulse Width and Frequency Modulation Buffered	X	X	X
Output Pulse Width Modulation Buffered	X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

1.6.20 Periodic interrupt timer (PIT) module

The PIT features the following:

- Four general purpose interrupt timers
- As many as two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for Real Time Interrupt, clocked from main external oscillator

- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - — Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- External non-maskable interrupt directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.6.24 System Integration Unit (SIU)

The SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- As many as four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of as many as 132 input/output pins (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to as many as 14 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.

1.6.25 System Clocks and Clock Generation Modules

The system clock on the PXD10 can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

- The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32).
- Additional programmable peripheral bus clock divider ratio (÷1 to ÷16)
- The PXD10 has two on-chip FMPLLs—the primary module and an auxiliary module.
  - — Each features the following:
    - – Input clock frequency from 4 MHz to 16 MHz
    - – Lock detect circuitry continuously monitors lock status
    - – Loss Of Clock (LOC) detection for reference and feedback clocks
    - – On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PC[2]	PCR[32]	Option 0 Option 1 Option 2 Option 3	GPIO[32] — — —	ANS[2]	SIUL — — —	I/O	J	None, None	70	86
PC[3]	PCR[33]	Option 0 Option 1 Option 2 Option 3	GPIO[33] — — —	ANS[3]	SIUL — — —	I/O	J	None, None	69	85
PC[4]	PCR[34]	Option 0 Option 1 Option 2 Option 3	GPIO[34] — — —	ANS[4]	SIUL — — —	I/O	J	None, None	68	84
PC[5]	PCR[35]	Option 0 Option 1 Option 2 Option 3	GPIO[35] — — —	ANS[5]	SIUL — — —	I/O	J	None, None	67	83
PC[6]	PCR[36]	Option 0 Option 1 Option 2 Option 3	GPIO[36] — — —	ANS[6]	SIUL — — —	I/O	J	None, None	66	82
PC[7]	PCR[37]	Option 0 Option 1 Option 2 Option 3	GPIO[37] — — —	ANS[7]	SIUL — — —	I/O	J	None, None	65	81
PC[8]	PCR[38]	Option 0 Option 1 Option 2 Option 3	GPIO[38] — — —	ANS[8]	SIUL — — —	I/O	J	None, None	62	78
PC[9]	PCR[39]	Option 0 Option 1 Option 2 Option 3	GPIO[39] — — —	ANS[9]	SIUL — — —	I/O	J	None, None	61	77

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] — SOUND —	ANS[10]	SIUL — SGL —	I/O	J	None, None	60	76
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] — MA0 PCS2_1	ANS[11]	SIUL — ADC DSPI_1	I/O	J	None, None	59	75
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] — MA1 PCS1_1	ANS[12]	SIUL — ADC DSPI_1	I/O	J	None, None	58	74
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 PCS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	57	73
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	56	72
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	55	71
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOSB[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	73	89
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOSB[22]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	74	90

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PD[10]	PCR[56]	Option 0 Option 1 Option 2 Option 3	GPIO[56] M2C1M SSD2_2 —	—	SIUL SMC SSD —	I/O	SMD	None, None	85	101
PD[11]	PCR[57]	Option 0 Option 1 Option 2 Option 3	GPIO[57] M2C1P SSD2_3 —	—	SIUL SMC SSD —	I/O	SMD	None, None	86	102
PD[12]	PCR[58]	Option 0 Option 1 Option 2 Option 3	GPIO[58] M3C0M SSD3_0 —	—	SIUL SMC SSD —	I/O	SMD	None, None	89	105
PD[13]	PCR[59]	Option 0 Option 1 Option 2 Option 3	GPIO[59] M3C0P SSD3_1 —	—	SIUL SMC SSD —	I/O	SMD	None, None	90	106
PD[14]	PCR[60]	Option 0 Option 1 Option 2 Option 3	GPIO[60] M3C1M SSD3_2 —	—	SIUL SMC SSD —	I/O	SMD	None, None	91	107
PD[15]	PCR[61]	Option 0 Option 1 Option 2 Option 3	GPIO[61] M3C1P SSD3_3 —	—	SIUL SMC SSD —	I/O	SMD	None, None	92	108
PE[0]	PCR[62]	Option 0 Option 1 Option 2 Option 3	GPIO[62] M4C0M SSD4_0 eMIOSA[15]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	93	109
PE[1]	PCR[63]	Option 0 Option 1 Option 2 Option 3	GPIO[63] M4C0P SSD4_1 eMIOSA[14]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	94	110

Table 7. Pad type descriptions

Abbreviation[1]	Description
F	Fast (with GPIO and digital alternate function)
J	Slow pads with analog muxing (built for ADC channels)
M1	Medium (with GPIO and digital alternate function)
M2	Programmable medium/slow pad (programmed via the slew rate control in the PCR): Slew rate disabled: Slow driver configuration (AC/DC parameters same as for a slow pad) Slew rate enabled: Medium driver configuration (AC/DC parameters same as for a medium pad)
S	Slow (with GPIO and digital alternate function)
SMD	Stepper motor driver (with slew rate control)
X	Oscillator

NOTES:
1 The pad descriptions refer to the different Pad Configuration Register (PCR) types. Refer to the SIUL chapter in the device reference manual for the features available for each pad type.

2.8.1 Signal details

Table 8. Signal details

Signal	Peripheral	Description
ABS[0]	BAM	Alternate Boot Select. Gives an option to boot by downloading code via CAN or LIN.
ANS[0:15]	ADC	Inputs used to bring into the device sensor-based signals for A/D conversion. ANS[0:15] connect to ATD channels [32:47].
MA[0:2]	ADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels. The available 8 multiplexed channels connect to ATD channels [64:71].
FABM		Force Alternate Boot mode. Forces the device to boot from the external bus (Can or LIN). If not asserted, the device boots up from the lowest flash sector containing a valid boot signature.
DCU_DE	DCU	Indicates that valid pixels are present.
DCU_HSYNC	DCU	Horizontal sync pulse for TFT-LCD display
DCU_PCLK	DCU	Output pixel clock for TFT-LCD display
DCU_R[0:7], DCU_G[0:7], DCU_B[0:7]	DCU	Red, green and blue color 8-bit Pixel values for TFT-LCD displays
DCU_TAG	DCU	Indicates when a tagged pixel is present in safety mode
DCU_VSYNC	DCU	Vertical sync pulse for TFT-LCD display
PCS[0..2]_0, PCS[0..2]_1	DSPI	Peripheral chip selects when device is in Master mode; not used in slave modes.
SCK_0, SCK_1	DSPI	SPI clock signal—bidirectional

3.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Nonvolatile User Options (NVUSRO) register. For a detailed description of the NVUSRO register, please see the chip reference manual.

3.3.1 NVUSRO[PAD3V5V] field description

Table 10 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 10. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’ (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 11. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’

The 4–16 MHz fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.4 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SSA})	—	–0.3	6.0	V
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})	—	-0.1	1.4	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	V_{SS12} – 0.1	V_{SS12} + 0.1	V
V_{DDR}	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	–0.3	6.0	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})	—	-0.1	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDE_A}[1]	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	–0.3	6.0	V
V_{DDE_B}[1]	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	–0.3	6.0	V
V_{DDE_C}[1]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	–0.3	6.0	V
V_{DDE_E}[1]	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	–0.3	6.0	V
V_{DDMA}[1]	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	–0.3	6.0	V
V_{DDMB}[1] V_{DDMC}[1]	SR	C	Voltage on VDDMB/C (stepper motor supply) pin with respect to ground (V_{SSMB})	—	–0.3	6.0	V
V_{SS}[2]	SR	C	I/O supply ground	—	0	0	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
V_{IN}	SR	C	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
		C		Relative to V_{DD}	–0.3	V_{DD} + 0.3[3]	

Table 13. Recommended operating conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up	—	5×10^{-6}	0.25	V/µs
T_A	SR	C	Ambient temperature under bias	—	−40	105	°C
T_J	SR	C	Junction temperature under bias		−40	150	

NOTES:
1. 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.
2. At least 10 µF capacitance must be connected between V_{DDR} and V_{SS}. This is required because of sharp surge due to external ballast.
3. V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.
4. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
   When voltage drops below V_{LVDHVL} device is reset.
6. V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

Table 14. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DDE_C}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[3]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD}[4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	4.5	5.5	V

3.4.2 Connecting power supply pins: What to do and what not to do

- Do:
  - Have all power/ground supplies connected on the board from a strong supply source rather than weak voltage divider sources unless there is “NO IO activity” in the section
  - Meet the supply specifications for max / typical operating conditions to guarantee correct operation
  - Place the decoupling near the supply/ground pin pair for EMI emissions reduction
  - Route high-noise supply/ground away from sensitive signals (for example, ADC channels must be away from SMD supply/motor pads)
  - Use star routing for the ballast supply from the VDDR supply to avoid ballast startup noise injected to VDDR supply of the device
  - Use LC inductive filtering for ADC, OSC, and PLL supplies if these are generated from common board regulators
- Do not:
  - Violate injection current limit per IO/All IO pins as per specifications
  - Connect sensitive supplies/ground on noisy supplies/ground (that is, ADC, PLL, and OSC)
  - Use SMD supply for generation of noise free supply as these are most noisy lines in the system
  - Connect different VDD pins (connected together inside the device) to different potentials.

3.5 Thermal characteristics

Table 15. LQFP thermal characteristics

Symbol		C	Parameter	Conditions	Value		Unit
					144-pin	176-pin	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[1]	Single layer board—1s	50	43	°C/W
	CC			Four layer board—2s2p	41	35	°C/W
$R_{\theta JMA}$	CC	D	Thermal resistance, junction-to-moving-air ambient[2]	@ 200 ft./min., single layer board—1s	41	35	°C/W
	CC			@ 200 ft./min., four layer board—2s2p	35	30	°C/W
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[2]	—	29	24	°C/W
$R_{\theta JCtop}$	CC	D	Thermal resistance, junction-to-case (top)[3]	—	10	9	°C/W
Ψ_{JT}	CC	D	Junction-to-package top thermal characterization parameter, natural convection[4]	—	2	2	°C/W

NOTES:
1 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

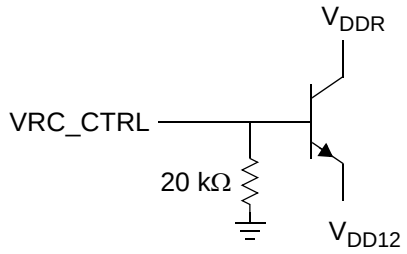

Figure 5. External NPN ballast connections

Table 19. Allowed ballast components

Part	Manufacturer	Recommended derivative
BCP68	ON, IFX, NXP, Fairchild, ST, etc.	BCP68
BCX68	IFX	BCX68-10 BCX68-16
BC817	ON, IFX, NXP, Fairchild, etc.	BC817Su BC817-25
BCP56	ON, IFX, NXP, Fairchild, ST, etc.	BCP68-10 BCP68-16

Table 20. Ballast component parameters

Parameter	Specification
Capacitance on VDDR	10 μF (minimum) Place close to NPN collector
Stability capacitance on VDD12	40 μF (minimum) Place close to NPN emitter
Decoupling capacitance on VDD12	100 nF × number of pins (minimum) Place on each VDD12/VSS12 pair and on the PLL supply/ground pair
Base resistor	20 kΩ

The capacitor values listed in Table 20 include a de-rating factor of 40%, covering tolerance, temperature, and aging effects. These factors are taken into account to assure proper operation under worst-case conditions. X7R type materials are recommended for all capacitors, based on ESR characteristics.

Large capacitors are for regulator stability and should be located near the external ballast transistor. The number of capacitors is not important — only the overall capacitance value and the overall ESR value are important.

Small capacitors are for power supply decoupling, although they do contribute to the overall capacitance values. They should be located close to the device pin.

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 11. Start-up reset requirements

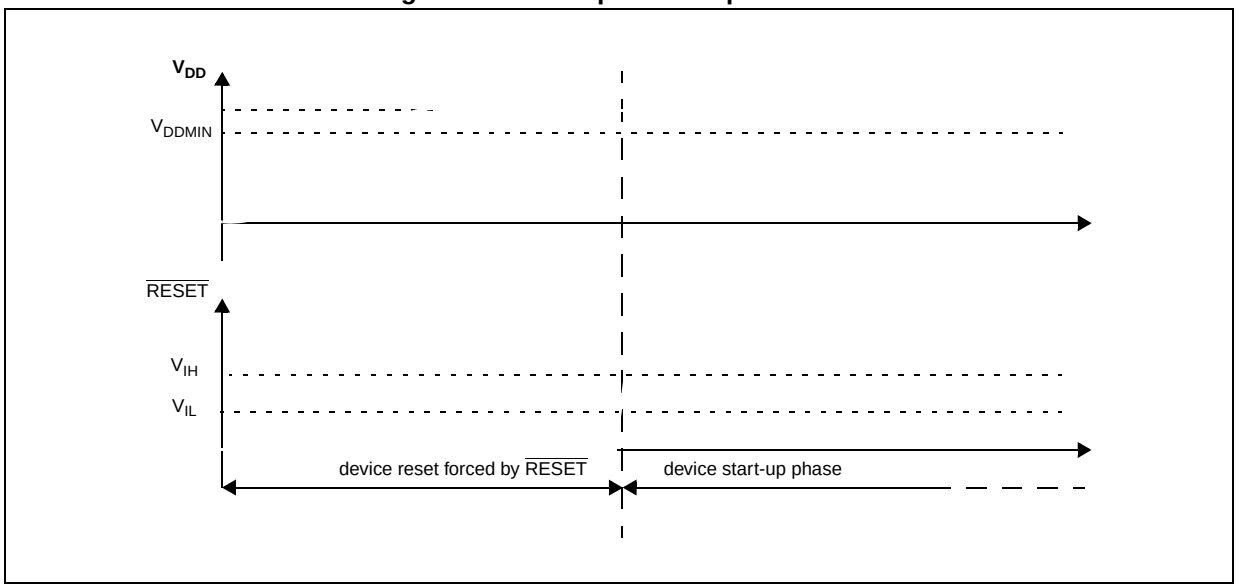

Figure 12. Noise filtering on reset signal

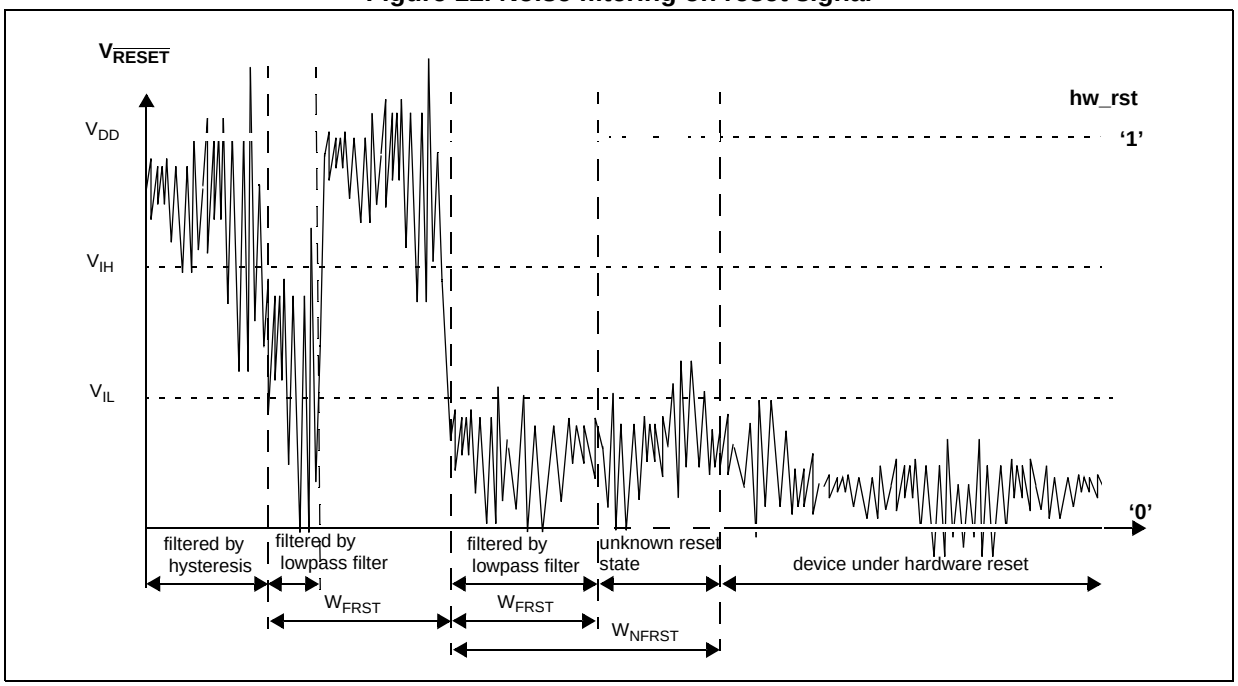

Table 51. Pad AC specifications (3.3 V, PAD3V5V = 1)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

NOTES:
1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition
2 Slope at rising/falling edge

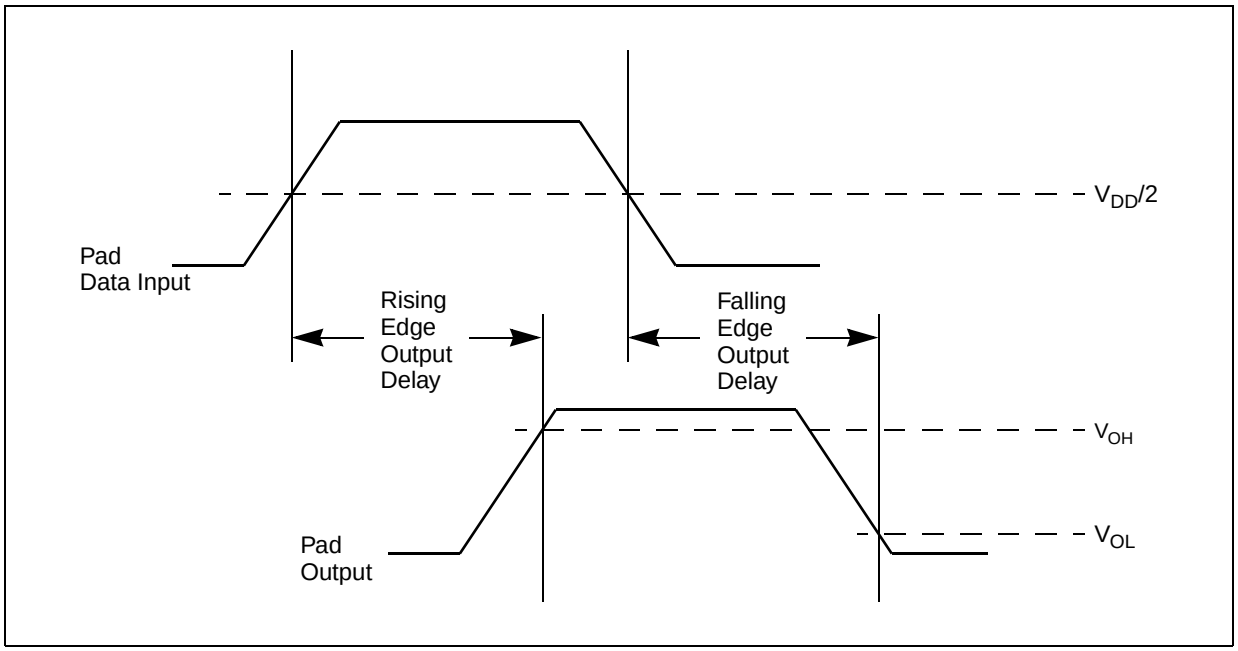

Figure 22. Pad output delay

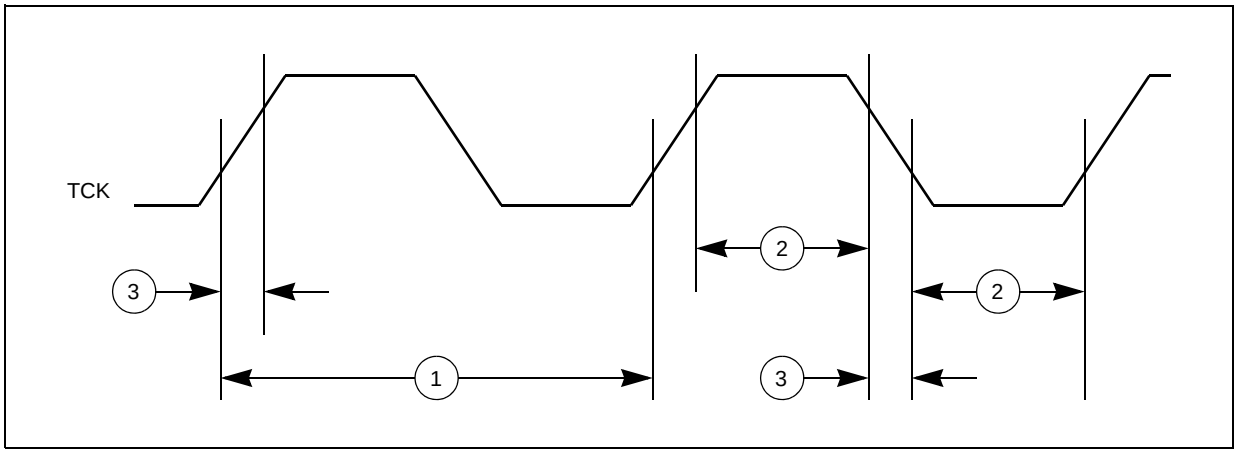

Figure 23. JTAG test clock input timing

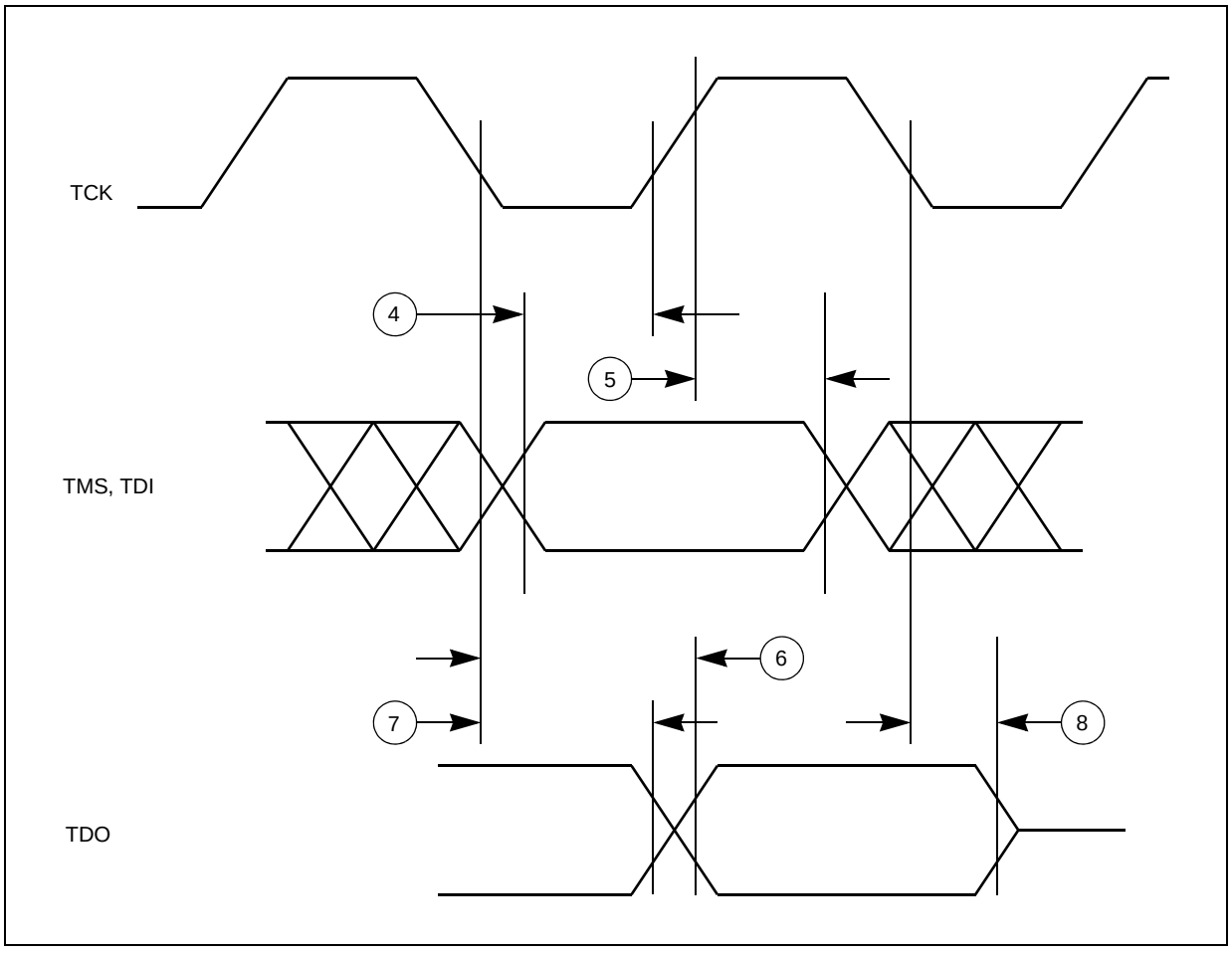

Figure 24. JTAG test access port timing

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

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TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 48. LQFP144 mechanical drawing (Part 3 of 3)

NOTES:

1 DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2 DIMENSIONS IN MILLIMETERS.

3 DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4 DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5 THIS DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.

6 THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. THIS DIMENSIONS INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7 THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 51. LQFP176 mechanical drawing (Part 3 of 3)