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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
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  - 4–16 MHz fast external crystal oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)—included in processor platform
  - Four-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status and provides an entry point for the censorship password mechanism

- The description of the pad configuration registers in Chapter 37, System Integration Unit Lite (SIUL)
- The device data sheet

2.6 System pins

The system pins are listed in Table 3.

Table 3. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET config	Pin No.		
					144 LQFP	176 LQFP	208 MAPBGA
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull up	24	24	J1
EXTAL	Analog output of the oscillator amplifier circuit. Input for the clock generator in bypass mode.		X	—	29	29	M1
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	—	27	27	K1
VRC_CTRL	VREG ballast control gain	—	—	—	25	25	P1
VREG_BYPASS[1]	Pin used for factory testing	I	X	—	32	32	M4

NOTES:
1 VREG_BYPASS should be pulled down externally.

2.7 Debug pins

The debug pins are listed in Table 4 and Table 5.

Table 4. Debug pin descriptions

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP [1]	208 MAPBGA
EVTI	Nexus event input	M	I/O	None	—	37	A11
EVTO	Nexus event output	M	I/O	None	—	35	D12
MCKO	Nexus message clock output	F	I/O	None	—	33	B12
MDO0	Nexus message clock output	M	I/O	None	—	38	B11

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 PDI1 —	—	SIUL FlexCAN_0 PDI —	I/O	M1	None, None	106	130
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option3	GPIO[17] CANRX_0 PDI0 —	—	SIUL FlexCAN_0 PDI —	I/O	S	None, None	105	129
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	112	140
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	111	139
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	M1	None, None	48	62
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	M1	Input, Pulldown	49	63
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, Pullup	50	66
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOSB[22] —	—	SIUL DSPI_0 PWM/Timer —	I/O	S	None, None	46	56

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOSB[21] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	45	55
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOSB[20] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	44	54
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 PDI2 eMIOSA[23]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	S	None, None	107	131
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 PDI3 eMIOSA[16]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	M1	None, None	108	132
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_1 eMIOSB[19] PCS2_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	40	48
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_1 eMIOSB[18] PCS1_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	41	49
PB[14]	—	—	Reserved	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—
PC[0]	PCR[30]	Option 0 Option 1 Option 2 Option 3	GPIO[30] — — —	ANS[0]	SIUL — — —	I/O	J	None, None	72	88
PC[1]	PCR[31]	Option 0 Option 1 Option 2 Option 3	GPIO[31] — — —	ANS[1]	SIUL — — —	I/O	J	None, None	71	87

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] — SOUND —	ANS[10]	SIUL — SGL —	I/O	J	None, None	60	76
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] — MA0 PCS2_1	ANS[11]	SIUL — ADC DSPI_1	I/O	J	None, None	59	75
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] — MA1 PCS1_1	ANS[12]	SIUL — ADC DSPI_1	I/O	J	None, None	58	74
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 PCS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	57	73
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	56	72
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	55	71
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOSB[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	73	89
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOSB[22]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	74	90

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PG[0]	PCR[86]	Option 0 Option 1 Option 2 Option 3	GPIO[86] DCU_B0 SCL_3 SOUND	FP7	SIUL DCU I^2C_3 SGL	I/O	M2	None, None	9	9
PG[1]	PCR[87]	Option 0 Option 1 Option 2 Option 3	GPIO[87] DCU_B1 SDA_3 —	FP6	SIUL DCU I^2C_3 —	I/O	M1	None, None	10	10
PG[2]	PCR[88]	Option 0 Option 1 Option 2 Option 3	GPIO[88] DCU_B2 eMIOSB[19] —	FP5	SIUL DCU PWM/Timer —	I/O	M2	None, None	11	11
PG[3]	PCR[89]	Option 0 Option 1 Option 2 Option 3	GPIO[89] DCU_B3 eMIOSB[21] —	FP4	SIUL DCU PWM/Timer —	I/O	M1	None, None	12	12
PG[4]	PCR[90]	Option 0 Option 1 Option 2 Option 3	GPIO[90] DCU_B4 eMIOSB[17] —	FP3	SIUL DCU PWM/Timer —	I/O	M2	None, None	13	13
PG[5]	PCR[91]	Option 0 Option 1 Option 2 Option 3	GPIO[91] DCU_B5 eMIOSA[8] —	FP2	SIUL DCU PWM/Timer —	I/O	M1	None, None	14	14
PG[6]	PCR[92]	Option 0 Option 1 Option 2 Option 3	GPIO[92] DCU_B6 — —	FP1	SIUL DCU — —	I/O	M2	None, None	15	15
PG[7]	PCR[93]	Option 0 Option 1 Option 2 Option 3	GPIO[93] DCU_B7 — —	FP0	SIUL DCU — —	I/O	M1	None, None	16	16

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PJ[9]	PCR[114]	Option 0 Option 1 Option 2 Option 3	GPIO[114] PDI[5] — —	—	SIUL PDI — —	I/O	S	None, None	—	126
PJ[10]	PCR[115]	Option 0 Option 1 Option 2 Option 3	GPIO[115] PDI[6] — —	—	SIUL PDI — —	I/O	S	None, None	—	127
PJ[11]	PCR[116]	Option 0 Option 1 Option 2 Option 3	GPIO[116] PDI[7] — —	—	SIUL PDI — —	I/O	S	None, None	—	128
PJ[12]	PCR[117]	Option 0 Option 1 Option 2 Option 3	GPIO[117] PDI[8] eMIOSB[17] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	135
PJ[13]	PCR[118]	Option 0 Option 1 Option 2 Option 3	GPIO[118] PDI[9] eMIOSB[20] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	136
PJ[14]	PCR[119]	Option 0 Option 1 Option 2 Option 3	GPIO[119] PDI[10] eMIOSA[20] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	137
PJ[15]	PCR[120]	Option 0 Option 1 Option 2 Option 3	GPIO[120] PDI[11] eMIOSA[19] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	138
PK[0]	PCR[121]	Option 0 Option 1 Option 2 Option 3	GPIO[121] PDI[12] eMIOSA[18] DCU_TAG	—	SIUL PDI PWM/Timer DCU	I/O	M1	None, None	—	141

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PK[1]	PCR[122]	Option 0 Option 1 Option 2 Option 3	GPIO[122] PDI[13] eMIOSA[17] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	142
PK[2]	PCR[123]	Option 0 Option 1 Option 2 Option 3	GPIO[123] MCKO PDI[10] —	—	SIUL Nexus PDI —	I/O	F	None, None	—	33
PK[3]	PCR[124]	Option 0 Option 1 Option 2 Option 3	GPIO[124] MSEO PDI[11] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	34
PK[4]	PCR[125]	Option 0 Option 1 Option 2 Option 3	GPIO[125] EVTO PDI[12] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	35
PK[5]	PCR[126]	Option 0 Option 1 Option 2 Option 3	GPIO[126] EVTI PDI[13] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	37
PK[6]	PCR[127]	Option 0 Option 1 Option 2 Option 3	GPIO[127] MDO0 PDI[14] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	38
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] MDO1 PDI[15] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	40
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] MDO2 PDI[16] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	42

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] MDO3 PDI[17] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	44
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOSA[15] —	—	SIUL I^2C_1 PWM/Timer —	I/O	S	None, None	—	52
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOSA[14] —	—	SIUL I^2C_1 PWM/Timer —	I/O	S	None, None	—	53
PK[12]	—	—	Reserved	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—

NOTES:

1 Alternate functions are chosen by setting the values of the PCR[*n*].PA bitfields inside the SIUL module. PCR[*n*].PA = 00 → Option 0; PCR[n*n*.PA = 01 → Option 1; PCR[*n*].PA = 10 → Option 2; PCR[*n*].PA = 11→ Option 3. This is intended to select the output functions; to use one of the input functions, the PCR[*n*].IBE bit must be written to '1', regardless of the values selected in the PCR[*n*].PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Special functions are enabled independently from the standard digital pin functions. Enabling standard I/O functions in the PCR registers may interfere with their functionality. ADC functions are enabled using the PCR[APC] bit; other functions are enabled by enabling the respective module.

3 Using the PSMI registers in the System Integration Unit Lite (SIUL), different pads can be multiplexed to the same peripheral input. Please see the SIUL chapter of the *PXD10 Microcontroller Reference Manual* for details.

4 See Table 7.

5 Reset configuration is given as I/O direction and pull, e.g., "Input, Pullup".

6 This option on this pin has alternate functions that depend on whether the QuadSPI is in SPI mode or in serial flash mode (SFM).

7 Out of reset pins PH[0:3] are available as JTAG pins (TCK, TDI, TDO and TMS respectively). It is up to the user to configure pins PH[0:3] when needed.

8 This pin can be used for LCD supply pin VLCD. Refer to the voltage supply pin descriptions in the PXD10 data sheet for details.

3.4.1 Recommended operating conditions

NOTE

Maximum slew time for the supplies to ramp up should be 1 second, which is slowest ramp-up time.

V_{DDE_C} and V_{DDA} must be the same voltage.

V_{DDMB} and V_{DDMC} must be the same voltage.

Table 13. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	3.0	3.6	V
		C		Relative to V_{DDE_C}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[2]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	3.0	3.6	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}[4]	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[3,4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS}[6]	SR	C	I/O supply ground	—	0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	3.0	3.6	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	3.0	3.6	V
V_{DDE_C}	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	3.0	3.6	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	3.0	3.6	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	3.0	3.6	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})	—	3.0	3.6	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})	—	3.0	3.6	V

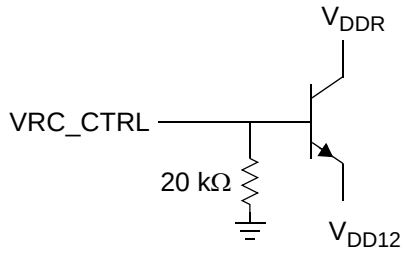


Figure 5. External NPN ballast connections

Table 19. Allowed ballast components

Part	Manufacturer	Recommended derivative
BCP68	ON, IFX, NXP, Fairchild, ST, etc.	BCP68
BCX68	IFX	BCX68-10 BCX68-16
BC817	ON, IFX, NXP, Fairchild, etc.	BC817Su BC817-25
BCP56	ON, IFX, NXP, Fairchild, ST, etc.	BCP68-10 BCP68-16

Table 20. Ballast component parameters

Parameter	Specification
Capacitance on VDDR	10 μF (minimum) Place close to NPN collector
Stability capacitance on VDD12	40 μF (minimum) Place close to NPN emitter
Decoupling capacitance on VDD12	100 nF × number of pins (minimum) Place on each VDD12/VSS12 pair and on the PLL supply/ground pair
Base resistor	20 kΩ

The capacitor values listed in Table 20 include a de-rating factor of 40%, covering tolerance, temperature, and aging effects. These factors are taken into account to assure proper operation under worst-case conditions. X7R type materials are recommended for all capacitors, based on ESR characteristics.

Large capacitors are for regulator stability and should be located near the external ballast transistor. The number of capacitors is not important — only the overall capacitance value and the overall ESR value are important.

Small capacitors are for power supply decoupling, although they do contribute to the overall capacitance values. They should be located close to the device pin.

[2] Values provided for reference only. The permitted temperature range of the chip is specified separately.

3.7.4 Recommended power-up and power-down order

Figure 6 shows the recommended order for powering up the power supplies on this device.

The 1.2 V regulator output starts after the device's internal POR (VDDREG HV) is deasserted at approximately 2.7 V on VDDREG.

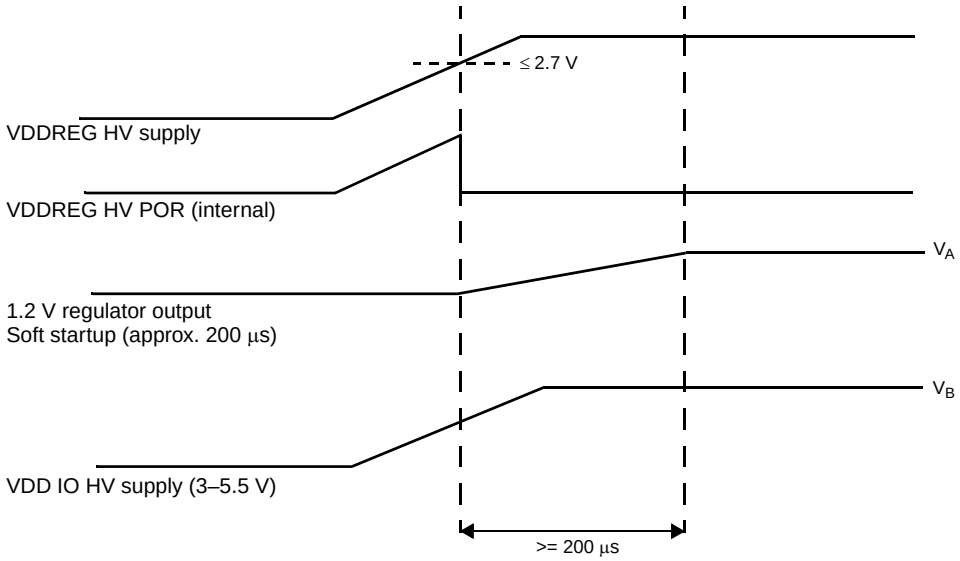


Figure 6. Recommended order for powering up the power supplies

The voltages V_A and V_B in Figure 6 must always obey the relation $V_B \geq V_A - 0.7$ V. Otherwise, currents from the 1.2 V supply to the 3.3 V supply may result.

Figure 7 shows the recommended order for powering down the power supplies on this device.

It is acceptable for the VDD IO HV supply to ramp down faster than the 1.2 V regulator output, even if the latter takes time to discharge the high 40 µF capacitance. (The capacitor will ultimately discharge.)

Table 33. SMD pad electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL}	CC	P	Low level input voltage	—	–0.4	—	$0.35 \times V_{DDM}$	V
V_{IH}	CC	P	High level input voltage	—	$0.65 \times V_{DDM}$	—	$V_{DDM}+0.4$	
V_{HYST}	CC	C	Schmitt trigger hysteresis	—	$0.1 \times V_{DDM}$	—	—	
V_{OL}	CC	P	Low level output voltage	I_{OL} = 20 mA[1]	—	—	0.32	
				I_{OL} = 30 mA[2]	—	—	0.48	
V_{OH}	CC	P	High level output voltage	I_{OH} = –20 mA[1]	V_{DDM}–0.32	—	—	
				I_{OH} = –30 mA[2]	V_{DDM}–0.48	—	—	
I_{PU}	CC	P	Internal pull-up device current	$V_{in}=V_{IL}$	–130	—	—	µA
				$V_{in}=V_{IH}$	—	—	–10	
I_{PD}	CC	P	Internal pull-down device current	$V_{in}=V_{IL}$	10	—	—	
				$V_{in}=V_{IH}$	—	—	130	
I_{IN}	CC	P	Input leakage current	—	-1	—	1	
R_{DSONH}	CC	C	SMD pad driver active high impedance	IOH ≤ –30 mA[2]	—	—	16	Ω
R_{DSONL}	CC	C	SMD pad driver active low impedance	IOL ≤ 30 mA[2]	—	—	16	Ω
V_{OMATCH}	CC	P	Output driver matching V_{OH} / V_{OL}	I_{OH} / I_{OL} ≤ 30 mA[2]	—	—	90	mV

NOTES:
1 VDD = 5.0 V ±10%, Tj = -40 to 150 °C.
2 VDD = 5.0 V ±10%, Tj = -40 to 130 °C.

3.8.4 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 34.

Table 35 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 44. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100		150	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation across temperature (T_A = -40°C to 105°C) and supply with respect to f_{SIRC} at T_A = 25 °C in high frequency configuration	Trimmed	-10%		+10%	kHz
I_{SIRC}	CC	D	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	C	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

3.16 Flash memory electrical characteristics

Table 45. Program and erase specifications

Symbol		C	Parameter	Value			Unit
				Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	22	50	500	µs
$T_{16kpperase}$	CC	C	16 KB block pre-program and erase time	300	500	5000	ms
$T_{32kpperase}$	CC	C	32 KB block pre-program and erase time	400	600	5000	ms
$T_{128kpperase}$	CC	C	128 KB block pre-program and erase time	800	1300	7500	ms
T_{eslat}	CC	D	Erase suspend latency	—	30	30	µs

NOTES:
1 Typical program and erase times assume nominal supply values and operation at 25 °C.
2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4 Actual hardware programming times. This does not include software overhead.

(since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 8

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 8 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 9

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 10:

Eqn. 10

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 11

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 12

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 13 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 13

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal

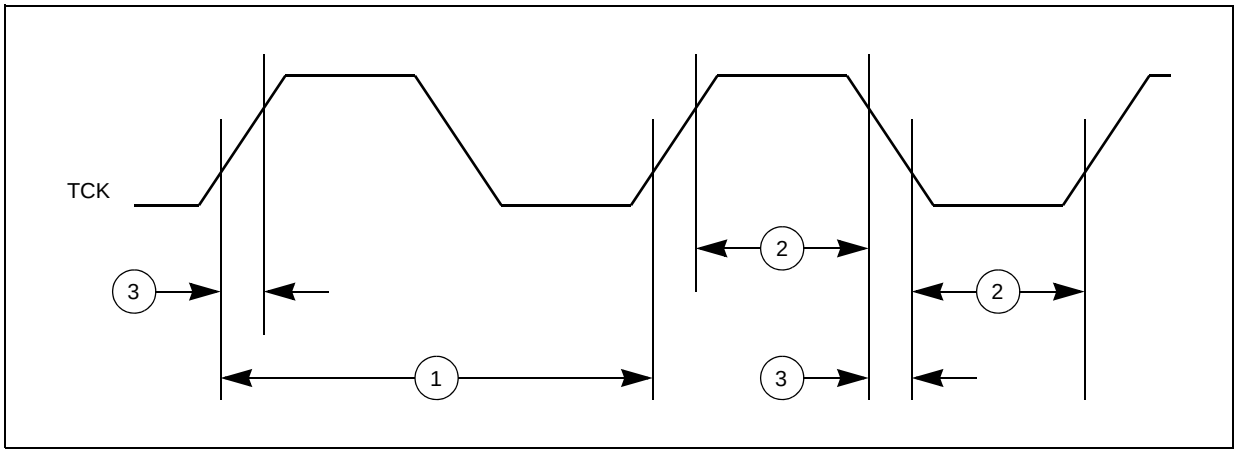


Figure 23. JTAG test clock input timing

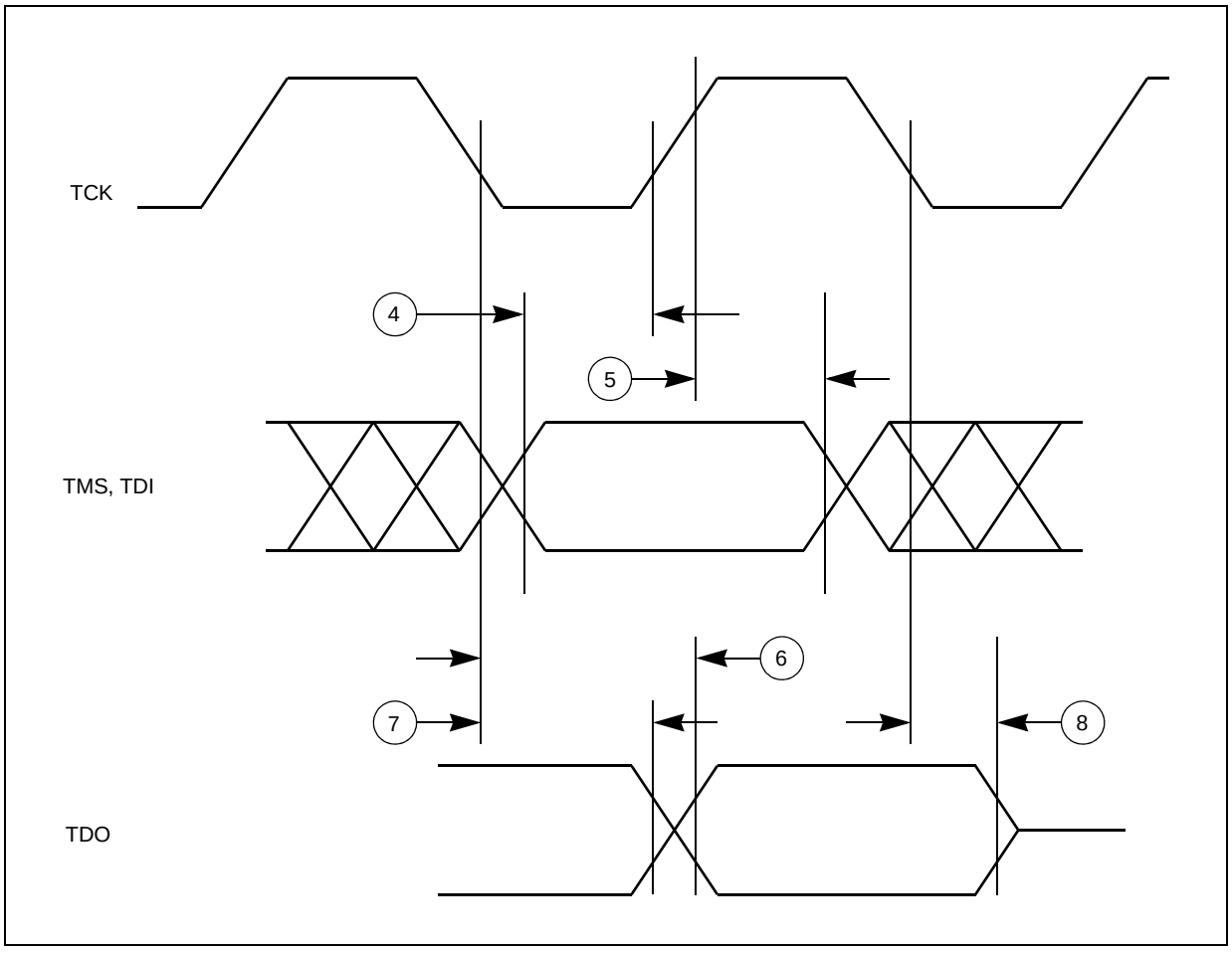


Figure 24. JTAG test access port timing

Table 57. IRQ and NMI timing

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{IPWL}	CC	T	IRQ/NMI Pulse Width Low	200	—	ns
2	t_{IPWH}	CC	T	IRQ/NMI Pulse Width High	200	—	ns
3	t_{ICYC}	CC	T	IRQ/NMI Edge to Edge Time[1]	400	—	ns

NOTES:
1 Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

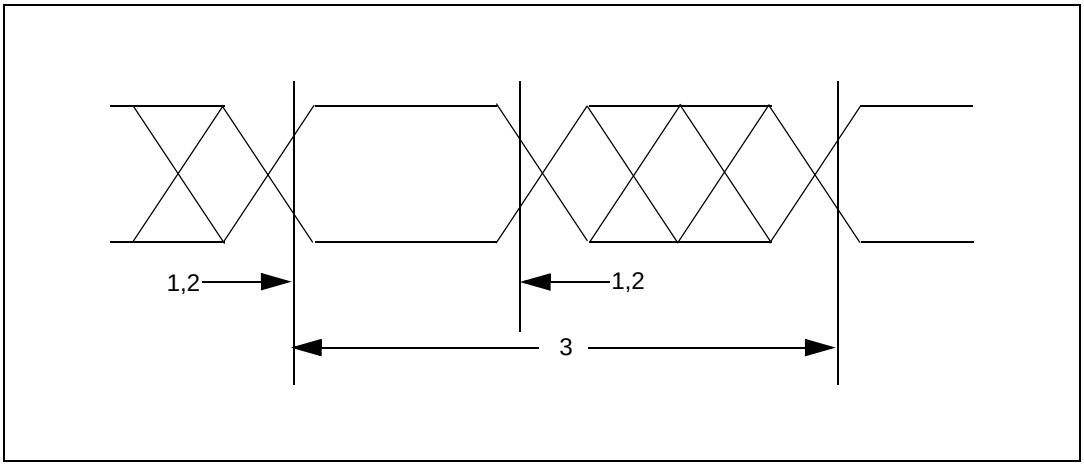


Figure 33. IRQ and NMI timing

3.20.5 eMIOS timing

Table 58. eMIOS timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min[2]	Max	
1	t_{MIPW}	CC	D	eMIOS input pulse width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS output pulse width	1	—	t_{CYC}

NOTES:
1 eMIOS timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00

2 There is no limitation on the peripheral for setting the minimum pulse width, the actual width is restricted by the pad delays. Refer to the pad specification section for the details.

3.20.6 FlexCAN timing

The CAN functions are available as TX pins at normal IO pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 59. FlexCAN timing[1]

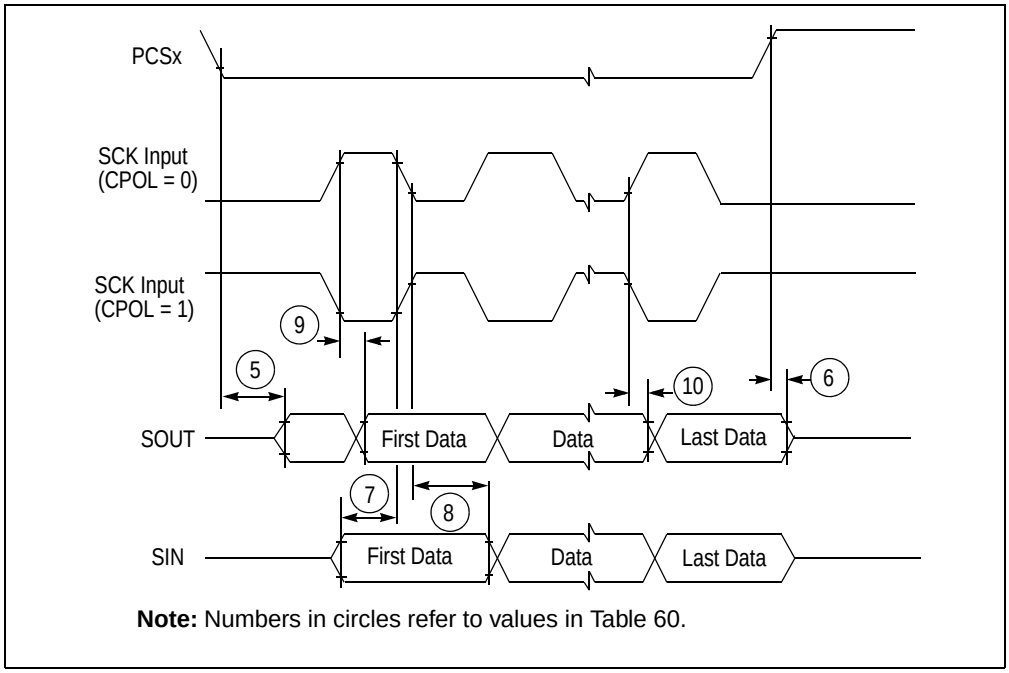
No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{CANOV}	CC	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns
2	t_{CANSU}	CC	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns

NOTES:
1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

3.20.7 Deserial Serial Peripheral Interface (DSPI)

Table 60. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI Cycle TIme[2,3]	Master (MTFE = 0) Slave (MTFE = 0) Slave Receive Only Mode	62 62 62	— — —	ns ns ns
2	t_{CSC}	CC	D	PCS to SCK Delay[4]	—	20	—	ns
3	t_{ASC}	CC	D	After SCK Delay[5]	—	20	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	—	0.4 x t_{SCK}	0.6 x t_{SCK}	ns
5	t_A	CC	D	Slave Access Time (PCSx active to SOUT driven)	SS active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	SS inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}			PCSx to PCSS time	—	20	—	ns
8	t_{PASC}			PCSS to PCSx time	—	20	—	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	35 2 20 35	— — — —	ns ns ns ns
10	t_{HI}	CC	D	Data Hold Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	–5 5 10 –5	— — — —	ns ns ns ns



Note: Numbers in circles refer to values in Table 60.

Figure 41. DSPI modified transfer format timing — slave, CPHA = 1

3.20.8 I^2C timing

Table 61. I^2C Input Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	IP-Bus Cycle[1]
2	—	CC	D	Clock low time	8	—	IP-Bus Cycle[1]
4	—	CC	D	Data hold time	0.0	—	ns
6	—	CC	D	Clock high time	4	—	IP-Bus Cycle[1]
7	—	CC	D	Data setup time	0.0	—	ns
8	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]
9	—	CC	D	Stop condition setup time	2	—	IP-Bus Cycle[1]

NOTES:
1 Inter Peripheral Clock is the clock at which the I^2C peripheral is working in the device

NOTES:

1 DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2 DIMENSIONS IN MILLIMETERS.

3 DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4 DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5 THIS DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.

6 THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. THIS DIMENSIONS INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7 THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 51. LQFP176 mechanical drawing (Part 3 of 3)