Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpxd1010vlu64

1 Overview

1.1 Document overview

This document describes the device features and highlights important electrical and physical characteristics. For functional characteristics, see the *PXD10 Microcontroller Reference Manual*.

1.2 Description

The PXD10 family of chips is designed to enable the development of industrial HMI applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

PXD10 chips incorporate a cost-efficient host processor core compliant with the Power Architecture® embedded category. The processor is 100% user-mode compatible with the Power Architecture and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the PXD10 family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memory sizes. The version with 1 MB of flash memory (PXD1010) features 160 KB of on-chip graphics SRAM.

See Table 1 for specific memory and feature sets of the product family members.

1.3 Device comparison

Table 1. PXD10 family feature set

Feature	PXD1005	PXD1010
CPU	e200z0h	
Execution speed	Static – 64 MHz	
Flash (ECC)	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB	
RAM (ECC)	48 KB	
Graphics RAM	No	160 KB
MPU	12 entry	
eDMA	16 channels	
Display Control Unit (DCU)	No	Yes
Parallel Data Interface	No	Yes
Stepper Motor Controller (SMC)	6 motors	
Stepper Stall Detect (SSD)	Yes	
Sound Generation Logic (SGL)	Yes	

1.6.3 Display Control Unit (DCU)

The DCU is a display controller designed to drive TFT LCD displays capable of driving up to WQVGA resolution screens with 16 layers and 4 planes with real time alpha-blending.

The DCU generates all the necessary signals required to drive the display: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync and Vertical-Sync.

Internal memory resource of the PXD10 allows to easily handle complex graphics contents (pictures, icons, languages, fonts) on a color TFT panel in up to Wide Quarter Video Graphics Array (WQVGA) sizes. All the data fetches from internal and/or external memory are performed by the internal four-channel DMA of the DCU providing a high speed/low latency access to the system backbone.

Control Descriptors (CDs) associated with each layer enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, 24bpp and 24bpp+alpha. The ability of the DCU to handle input data in resolutions as low as 1bpp, 2bpp and 4bpp enables a highly efficient use of internal memory resources of the PXD10. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending
- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic look-up table (color and gamma look-up)
- α–blending range: as many as 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware cursor
- Critical display content integrity monitoring for functional safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and/or external memory.

1.6.8 Flash memory

The PXD10 microcontroller has the following flash memory features:

- As much as 1 MB of burst flash memory
  - — Typical flash memory access time: 0 wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
  - — Two 4 × 128-bit page buffers with programmable prefetch control
    - – One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - – One set of page buffers allocated to Display Controller Unit and the eDMA
  - — 64-bit ECC with single-bit correction, double-bit detection for data integrity
  - — 64 KB data flash memory — separate 4 × 16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- Small block flash memory arrangement to support features such as boot block, operating system block
- Hardware managed flash memory writes, erase and verify sequence
- Censorship protection scheme to prevent flash memory content visibility
- Separate dedicated 64 KB data flash memory for EEPROM emulation
  - — Four erase sectors each containing 16 KB of memory
  - — Offers Read-While-Write functionality from main program space
  - — Same data retention and program erase specification as main program flash memory array

1.6.9 Static random-access memory (SRAM)

The PXD10 microcontrollers have as much as 48 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during STANDBY modes to retain contents during low power mode.

1.6.10 On-chip graphics SRAM

The PXD10 microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.6.16 Controller Area Network (CAN) module

The PXD10 contains two CAN modules that offer the following features:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler
  - Can catch the first message sent on the CAN network while the PXD10 is stopped. This guarantees a clean startup of the system without missing messages on the CAN network.
  - The CAN sampler is connected to one of the CAN RX pins.

1.6.17 Inter-IC Communications (I^2C) module

The I^2C module features the following:

- As many as four I^2C modules supported
- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

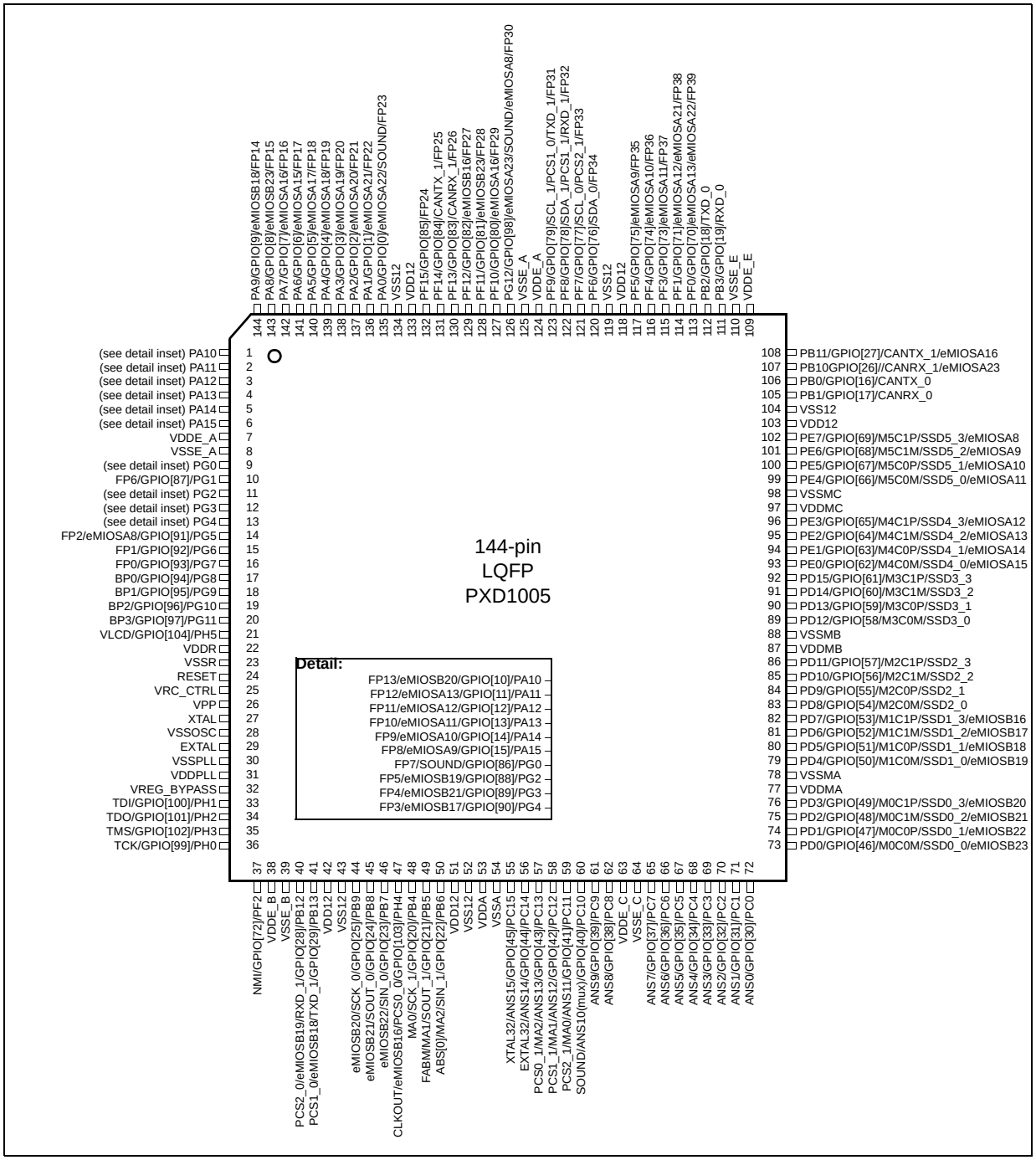

Figure 3. 144-pin LQFP pinout for PXD1005

2.3 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are floating with the following exceptions:

- PB[5] (FAB) is pull-down. Without external strong pullup the device starts fetching from flash.
- RESET pad is driven low. This is released only after PHASE2 reset completion.
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.
- The following pads are pullup:
  - PB[6]
  - PH[0]
  - PH[1]
  - PH[3]
  - EVTI

2.4 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

There is a preferred power-up sequence for devices in the PXD10 family. That sequence is described in the following paragraphs.

Broadly, the supply voltages can be grouped as follows:

- VREG HV supply (V_{DDR})
- Generic I/O supply
  - V_{DDA}
  - V_{DDE_A}
  - V_{DDE_B}
  - V_{DDE_C}
  - V_{DDE_E}
  - V_{DDMA}
  - V_{DDMB}
  - V_{DDMC}
  - V_{DDPLL}
- LV supply (V_{DD12})

The preferred order of ramp up is as follows:

1. Generic I/O supply

Table 4. Debug pin descriptions (continued)

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP [1]	208 MAPBGA
MDO1	Nexus message clock output	M	I/O	None	—	40	C11
MDO2	Nexus message clock output	M	I/O	None	—	42	D11
MDO3	Nexus message clock output	M	I/O	None	—	44	A10
MSEO	Nexus message clock output	M	I/O	None	—	34	C12

NOTES:
1 On the 176 LQFP package options the Nexus pins are multiplexed with other GPIO. On the 208 TEPBGA package, there are additional dedicated Nexus pins.

Table 5. Debug pin descriptions

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP	TEPBGA208 [1]
EVTI	Nexus event input	M	I/O	Input, Pull Up	—	—	T3
EVTO	Nexus event output	M	I/O	Input, Pull Up	—	—	R3
MCKO	Nexus message clock output	F	I/O	Input, Pull Up	—	—	T1
MDO0	Nexus message clock output	M	I/O	Input, Pull Up	—	—	T5
MDO1	Nexus message clock output	M	I/O	Input, Pull Up	—	—	P5
MDO2	Nexus message clock output	M	I/O	Input, Pull Up	—	—	P4
MDO3	Nexus message clock output	M	I/O	Input, Pull Up	—	—	L4
MSEO	Nexus message clock output	M	I/O	Input, Pull Up	—	—	T2

NOTES:
1 The dedicated (208 pin package only) Nexus output pins (Message Data outputs 0:3 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before-the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance-driver (when used as a general purpose input [GPI] in the application).

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PE[2]	PCR[64]	Option 0 Option 1 Option 2 Option 3	GPIO[64] M4C1M SSD4_2 eMIOSA[13]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	95	111
PE[3]	PCR[65]	Option 0 Option 1 Option 2 Option 3	GPIO[65] M4C1P SSD4_3 eMIOSA[12]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	96	112
PE[4]	PCR[66]	Option 0 Option 1 Option 2 Option 3	GPIO[66] M5C0M SSD5_0 eMIOSA[11]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	99	115
PE[5]	PCR[67]	Option 0 Option 1 Option 2 Option 3	GPIO[67] M5C0P SSD5_1 eMIOSA[10]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	100	116
PE[6]	PCR[68]	Option 0 Option 1 Option 2 Option 3	GPIO[68] M5C1M SSD5_2 eMIOSA[9]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	101	117
PE[7]	PCR[69]	Option 0 Option 1 Option 2 Option 3	GPIO[69] M5C1P SSD5_3 eMIOSA[8]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	102	118
PE[8]	—	—	Reserved	—	—	—	—	—	—	—
PE[9]	—	—	Reserved	—	—	—	—	—	—	—
PE[10]	—	—	Reserved	—	—	—	—	—	—	—
PE[11]	—	—	Reserved	—	—	—	—	—	—	—
PE[12]	—	—	Reserved	—	—	—	—	—	—	—
PE[13]	—	—	Reserved	—	—	—	—	—	—	—
PE[14]	—	—	Reserved	—	—	—	—	—	—	—
PE[15]	—	—	Reserved	—	—	—	—	—	—	—

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PG[8]	PCR[94]	Option 0 Option 1 Option 2 Option 3	GPIO[94] DCU_VSYNC — —	BP0	SIUL DCU — —	I/O	M2	Input, None	17	17
PG[9]	PCR[95]	Option 0 Option 1 Option 2 Option 3	GPIO[95] DCU_HSYNC — —	BP1	SIUL DCU — —	I/O	M1	Input, None	18	18
PG[10]	PCR[96]	Option 0 Option 1 Option 2 Option 3	GPIO[96] DCU_DE — —	BP2	SIUL DCU — —	I/O	M2	None, None	19	19
PG[11]	PCR[97]	Option 0 Option 1 Option 2 Option 3	GPIO[97] DCU_PCLK — —	BP3	SIUL DCU — —	I/O	M1	None, None	20	20
PG[12]	PCR[98]	Option 0 Option 1 Option 2 Option 3	GPIO[98] eMIOSA[23] SOUND eMIOSA[8]	FP30	SIUL PWM/Timer SGL PWM/Timer	I/O	S	None, None	126	156
PG[13]	—	—	Reserved	—	—	—	—	—	—	—
PG[14]	—	—	Reserved	—	—	—	—	—	—	—
PG[15]	—	—	Reserved	—	—	—	—	—	—	—
PH[0][7]	PCR[99]	Option 0 Option 1 Option 2 Option 3	GPIO[99] TCK — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	36	43
PH[1][7]	PCR[100]	Option 0 Option 1 Option 2 Option 3	GPIO[100] TDI — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	33	36

3.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Nonvolatile User Options (NVUSRO) register. For a detailed description of the NVUSRO register, please see the chip reference manual.

3.3.1 NVUSRO[PAD3V5V] field description

Table 10 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 10. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’ (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 11. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’

The 4–16 MHz fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

Table 13. Recommended operating conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up	—	5×10^{-6}	0.25	V/µs
T_A	SR	C	Ambient temperature under bias	—	−40	105	°C
T_J	SR	C	Junction temperature under bias		−40	150	

NOTES:
1. 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.
2. At least 10 µF capacitance must be connected between V_{DDR} and V_{SS}. This is required because of sharp surge due to external ballast.
3. V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.
4. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
   When voltage drops below V_{LVDHVL} device is reset.
6. V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

Table 14. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DDE_C}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[3]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD}[4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	4.5	5.5	V

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043 USA
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.6 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.6.1 EMC requirements on board

The following practices help minimize noise in applications.

- Place a 100 nF capacitor between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. The voltage regulator also requires stability capacitors for these supply pairs.
- Place a 10 μF capacitor on VDDR.
- Isolate VDDR with ballast emitter to avoid voltage droop during STANDBY mode exit.
- Enable pad slew rate only as necessary to eliminate I/O noise:
  - — Enabling slew rate for SMD pads will reduce noise on motors.
  - — Disabling slew rate for non-SMD pads will reduce noise on non-SMD IOs.
- Enable PLL modulation (± 2%) for system clock.
- Place decoupling capacitors for all HV supplies close to the pins.

3.6.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:

Table 31. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level MEDIUM configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level MEDIUM configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF MEDIUM configuration	recommended configuration at V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	7	mA/ns
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1	—	—	16	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.
3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 33. SMD pad electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL}	CC	P	Low level input voltage	—	–0.4	—	$0.35 \times V_{DDM}$	V
V_{IH}	CC	P	High level input voltage	—	$0.65 \times V_{DDM}$	—	$V_{DDM}+0.4$	
V_{HYST}	CC	C	Schmitt trigger hysteresis	—	$0.1 \times V_{DDM}$	—	—	
V_{OL}	CC	P	Low level output voltage	I_{OL} = 20 mA[1]	—	—	0.32	
				I_{OL} = 30 mA[2]	—	—	0.48	
V_{OH}	CC	P	High level output voltage	I_{OH} = –20 mA[1]	V_{DDM}–0.32	—	—	
				I_{OH} = –30 mA[2]	V_{DDM}–0.48	—	—	
I_{PU}	CC	P	Internal pull-up device current	$V_{in}=V_{IL}$	–130	—	—	µA
				$V_{in}=V_{IH}$	—	—	–10	
I_{PD}	CC	P	Internal pull-down device current	$V_{in}=V_{IL}$	10	—	—	
				$V_{in}=V_{IH}$	—	—	130	
I_{IN}	CC	P	Input leakage current	—	-1	—	1	
R_{DSONH}	CC	C	SMD pad driver active high impedance	IOH ≤ –30 mA[2]	—	—	16	Ω
R_{DSONL}	CC	C	SMD pad driver active low impedance	IOL ≤ 30 mA[2]	—	—	16	Ω
V_{OMATCH}	CC	P	Output driver matching V_{OH} / V_{OL}	I_{OH} / I_{OL} ≤ 30 mA[2]	—	—	90	mV

NOTES:
1 VDD = 5.0 V ±10%, Tj = -40 to 150 °C.
2 VDD = 5.0 V ±10%, Tj = -40 to 130 °C.

3.8.4 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 34.

Table 35 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 34. I/O supply segment

Package	Supply segment				
	A[1]	B[2]	C[3,4]	D[5]	E[6]
144 LQFP	pins 1–21 pins 113–144	pins 22– 52	pins 53–72	pins 73–102	pins 103–112
176 LQFP	pins 1–21 pins 143–176	pins 22–68	pins 69–88	pins 89–118	pins 119–142

NOTES:
1 LCD pad segment containing pad supplies V_{DDE_A}
2 Miscellaneous pad segment containing pad supplies V_{DDE_B}
3 ADC pad segment containing pad supplies V_{DDE_C}
4 V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE\_C} = V_{DDA} \pm 100$ mV.
5 Stepper Motor pad segment containing I/O supplies V_{DDMA}, V_{DDMB}, V_{DDMC}
6 Miscellaneous pad segment containing pad supplies V_{DDE_E}

Table 35. I/O consumption

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{SWTSLW}	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	3.2	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	2.3	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.7	

Table 35. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	13.4	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	18.3	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	8.5	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	11.0	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22.0	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	33.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	56.0	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	20.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25.0	
I_{DYNSEG}	SR	D	Sum of all the dynamic and static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65	
$I_{DDMxAVG}$	SR	D	Sum of currents of two motors assigned to segment V_{DDMx}, V_{SSMx} pair	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 T_J = 130 °C	—	—	90	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 T_J = –40 °C	—	—	120	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

Table 37. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt Trigger	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS Schmitt Trigger	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	D	Input hysteresis CMOS Schmitt Trigger	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
I_{WPU}	CC	P	Weak pull-up current absolute value	—	10	—	150	µA
		D	RUN Current during RESET	Before Flash is ready	—	10	—	mA
				After Flash is ready	—	20	—	mA

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to reset generation module (RGM) section of the device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).

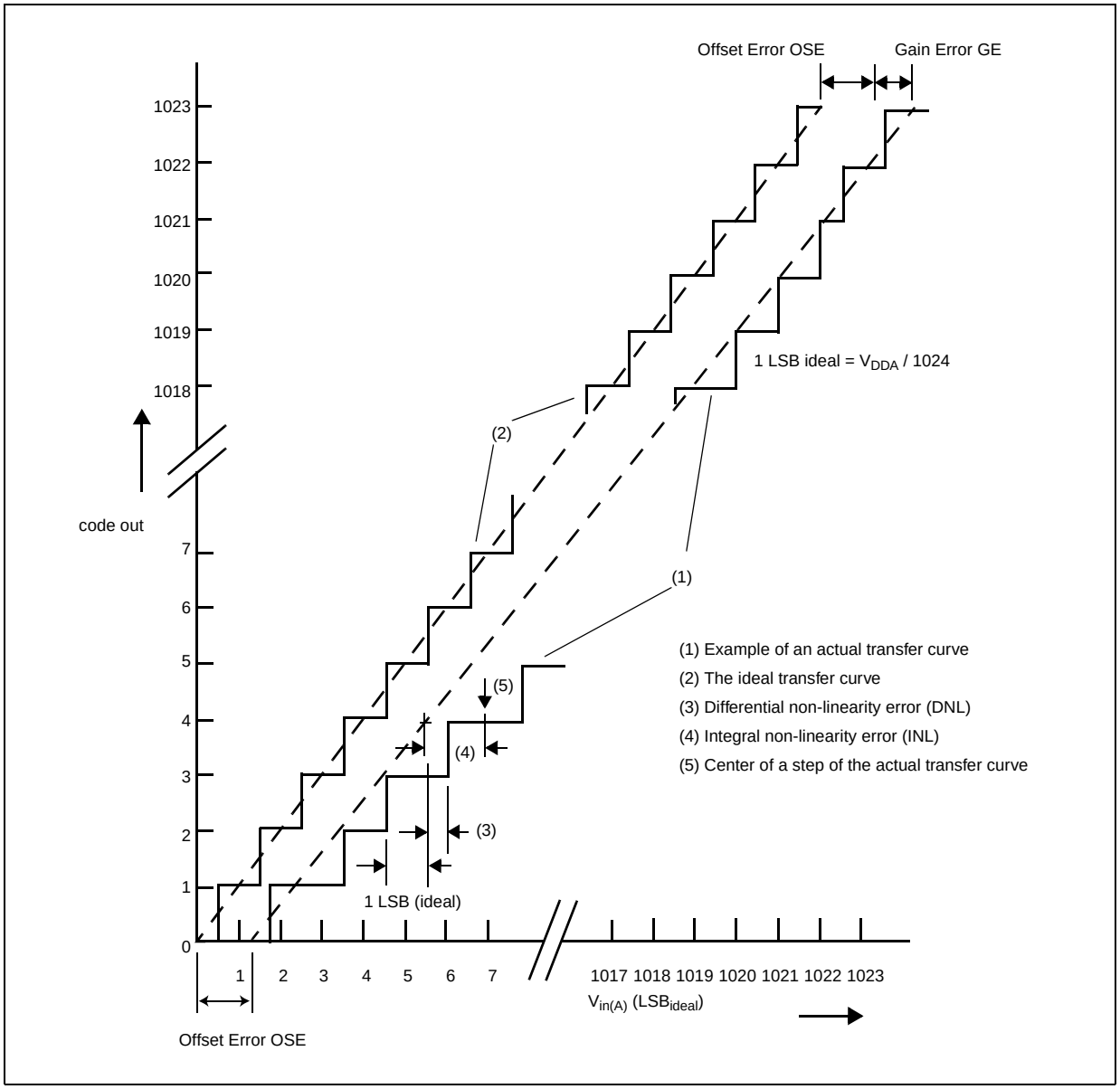

Figure 17. ADC Characteristics and Error Definitions

3.17.1 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer

source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

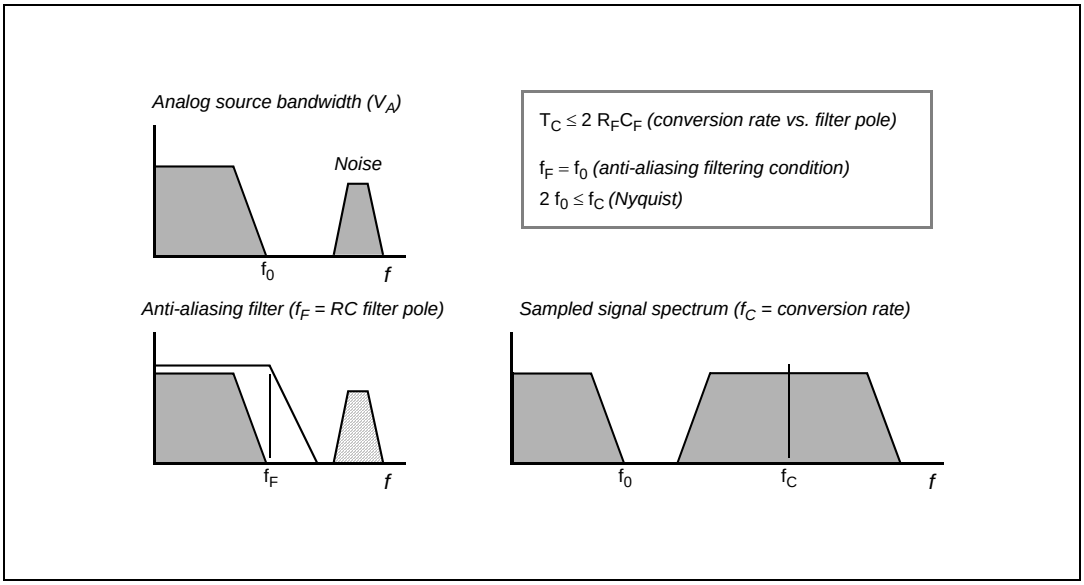

Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 14 between the ideal and real sampled voltage on C_S:

Eqn. 14

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 15

$$C_F > 2048 \bullet C_S$$

6 Revision history

Table 65. Document revision history

Revision	Date	Substantive changes
1	30 Sep 2011	Initial release.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: PXD10
Rev. 1
09/2011

freescale™
semiconductor