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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2921fbd100-551

- Other peripherals:
  - Two 10-bit ADCs, 8-channels each, with 3.3 V measurement range provide 8 analog inputs each with conversion times as low as 2.44 μs per channel. Each channel provides a compare function to minimize interrupts.
  - Multiple trigger-start option for all ADCs: timer, PWM, other ADC and external signal input.
  - Four 32-bit timers each containing four capture-and-compare registers linked to I/Os.
  - Four six-channel PWMs (Pulse Width Modulators) with capture and trap functionality.
  - Two dedicated 32-bit timers to schedule and synchronize PWM and ADC.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - 32-bit watchdog with timer change protection, running on safe clock.
- Up to 60 general-purpose I/O pins with programmable pull-up, pull-down, or bus keeper.
- Vectored Interrupt Controller (VIC) with 16 priority levels.
- Up to 16 level-sensitive external interrupt pins, including USB, CAN and LIN wake-up features.
- Configurable clock out pin for driving external system clocks.
- Processor wake-up from power-down via external interrupt pins and CAN or LIN activity.
- Flexible Reset Generator Unit (RGU) able to control resets of individual modules.
- Flexible Clock-Generation Unit (CGU) able to control clock frequency of individual modules:
  - On-chip very low-power ring oscillator; fixed frequency of 0.4 MHz; always on to provide a Safe_Clock source for system monitoring.
  - On-chip crystal oscillator with a recommended operating range from 10 MHz to 25 MHz. PLL input range 10 MHz to 25 MHz.
  - On-chip PLL allows CPU operation up to a maximum CPU rate of 125 MHz.
  - Generation of up to 11 base clocks.
  - Seven fractional dividers.
- Second, dedicated CGU with its own PLL generates the USB clock and a configurable clock output.
- Highly configurable system Power Management Unit (PMU):
  - clock control of individual modules.
  - allows minimization of system operating power consumption in any configuration.
- Standard ARM test and debug interface with real-time in-circuit emulator.
- Boundary-scan test supported.
- ETM/ETB debug functions with 8 kB of dedicated SRAM also accessible for application code and data storage.
- Dual power supply:
  - CPU operating voltage: 1.8 V ± 5 %.
  - I/O operating voltage: 2.7 V to 3.6 V; inputs tolerant up to 5.5 V.
- 100-pin LQFP package.
- −40 °C to +85 °C ambient operating temperature range.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2921FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2923FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2925FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

3.1 Ordering options

Table 2. Part options

Type number	Flash memory	SRAM (incl. ETB SRAM)	USB device	UART RS-485	LIN 2.0/ UART	CAN	Package
LPC2921FBD100	128 kB	24 kB	yes	2	2	2	LQFP100
LPC2923FBD100	256 kB	24 kB	yes	2	2	2	LQFP100
LPC2925FBD100	512 kB	40 kB	yes	2	2	2	LQFP100

Table 3. LQFP100 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P5[19]/USB_D+	12[2]	GPIO5, pin 19	USB_D+	-	-
P5[18]/USB_D−	13[2]	GPIO5, pin 18	USB_D−	-	-
$V_{DD(IO)}$	14	3.3 V power supply for I/O			
$V_{DD(CORE)}$	15	1.8 V power supply for digital core			
$V_{SS(CORE)}$	16	ground for core			
$V_{SS(IO)}$	17	ground for I/O			
P1[27]/CAP1[2]/ TRAP2/PMAT3[3]	18[1]	GPIO1, pin 27	TIMER1 CAP2, ADC2 EXT START	PWM TRAP2	PWM3 MAT3
P1[26]/PMAT2[0]/ TRAP3/PMAT3[2]	19[1]	GPIO1, pin 26	PWM2 MAT0	PWM TRAP3	PWM3 MAT2
$V_{DD(IO)}$	20	3.3 V power supply for I/O			
P1[25]/PMAT1[0]/ USB_VBUS/ PMAT3[1]	21[1]	GPIO1, pin 25	PWM1 MAT0	USB_VBUS	PWM3 MAT1
P1[24]/PMAT0[0]/ USB_CONNECT/ PMAT3[0]	22[1]	GPIO1, pin 24	PWM0 MAT0	USB_CONNECT	PWM3 MAT0
P1[23]/RXD0	23[1]	GPIO1, pin 23	UART0 RXD	-	-
P1[22]/TXD0/ USB_UP_LED	24[1]	GPIO1, pin 22	UART0 TXD	USB_UP_LED	-
TMS	25[1]	IEEE 1149.1 test mode select, pulled up internally			
TCK	26[1]	IEEE 1149.1 test clock			
P1[21]/CAP3[3]/ CAP1[3]	27[1]	GPIO1, pin 21	TIMER3 CAP3	TIMER1 CAP3, MSCSS PAUSE	-
P1[20]/CAP3[2]/ SCS0[1]	28[1]	GPIO1, pin 20	TIMER3 CAP2	SPI0 SCS1	-
P1[19]/CAP3[1]/ SCS0[2]	29[1]	GPIO1, pin 19	TIMER3 CAP1	SPI0 SCS2	-
P1[18]/CAP3[0]/ SDO0	30[1]	GPIO1, pin 18	TIMER3 CAP0	SPI0 SDO	-
P1[17]/CAP2[3]/ SDI0	31[1]	GPIO1, pin 17	TIMER2 CAP3	SPI0 SDI	-
$V_{SS(IO)}$	32	ground for I/O			
P1[16]/CAP2[2]/ SCK0	33[1]	GPIO1, pin 16	TIMER2 CAP2	SPI0 SCK	-
P1[15]/CAP2[1]/ SCS0[0]	34[1]	GPIO1, pin 15	TIMER2 CAP1	SPI0 SCS0	-
P1[14]/CAP2[0]/ SCS0[3]	35[1]	GPIO1, pin 14	TIMER2 CAP0	SPI0 SCS3	-
P1[13]/EI3/SCL1	36[1]	GPIO1, pin 13	EXTINT3	I^2C1 SCL	-
P1[12]/EI2/SDA1	37[1]	GPIO1, pin 12	EXTINT2	I^2C1 SDA	-
$V_{DD(IO)}$	38	3.3 V power supply for I/O			
P1[11]/SCK1/SCL0	39[1]	GPIO1, pin 11	SPI1 SCK	I^2C0 SCL	-

Table 3. LQFP100 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
$V_{DDA(ADC3V3)}$	74	3.3 V power supply for ADC			
JTAGSEL	75[1]	TAP controller select input; LOW-level selects the ARM debug mode; HIGH-level selects boundary scan; pulled up internally.			
n.c.	76	not connected to a function; must be tied to 3.3 V power supply for ADC $V_{DDA(ADC3V3)}$.			
VREFP	77[3]	HIGH reference for ADC			
VREFN	78[3]	LOW reference for ADC			
P0[8]/IN1[0]	79[4]	GPIO0, pin 8	ADC1 IN0	-	-
P0[9]/IN1[1]	80[4]	GPIO0, pin 9	ADC1 IN1	-	-
P0[10]/IN1[2]/ PMAT1[0]	81[4]	GPIO0, pin 10	ADC1 IN2	PWM1 MAT0	-
P0[11]/IN1[3]/ PMAT1[1]	82[4]	GPIO0, pin 11	ADC1 IN3	PWM1 MAT1	-
$V_{SS(IO)}$	83	ground for I/O			
P0[12]/IN1[4]/ PMAT1[2]	84[4]	GPIO0, pin 12	ADC1 IN4	PWM1 MAT2	-
P0[13]/IN1[5]/ PMAT1[3]	85[4]	GPIO0, pin 13	ADC1 IN5	PWM1 MAT3	-
P0[14]/IN1[6]/ PMAT1[4]	86[4]	GPIO0, pin 14	ADC1 IN6	PWM1 MAT4	-
P0[15]/IN1[7]/ PMAT1[5]	87[4]	GPIO0, pin 15	ADC1 IN7	PWM1 MAT5	-
P0[16]IN2[0]/TXD0	88[4]	GPIO0, pin 16	ADC2 IN0	UART0 TXD	-
P0[17]/IN2[1]/ RXD0/A23	89[4]	GPIO0, pin 17	ADC2 IN1	UART0 RXD	-
$V_{DD(CORE)}$	90	1.8 V power supply for digital core			
$V_{SS(CORE)}$	91	ground for digital core			
$V_{DD(IO)}$	92	3.3 V power supply for I/O			
P0[18]/IN2[2]/ PMAT2[0]	93[4]	GPIO0, pin 18	ADC2 IN2	PWM2 MAT0	-
P0[19]/IN2[3]/ PMAT2[1]	94[4]	GPIO0, pin 19	ADC2 IN3	PWM2 MAT1	-
P0[20]/IN2[4]/ PMAT2[2]	95[4]	GPIO0, pin 20	ADC2 IN4	PWM2 MAT2	-
P0[21]/IN2[5]/ PMAT2[3]	96[4]	GPIO0, pin 21	ADC2 IN5	PWM2 MAT3	-
P0[22]/IN2[6]/ PMAT2[4]/A18	97[4]	GPIO0, pin 22	ADC2 IN6	PWM2 MAT4	-
$V_{SS(IO)}$	98	ground for I/O			

6.8.6 EEPROM

EEPROM is a non-volatile memory mostly used for storing relatively small amounts of data, for example for storing settings. It contains one 16 kB memory block and is byte-programmable and byte-erasable.

The EEPROM can be accessed only through the flash controller.

6.9 General Purpose DMA (GPDMA) controller

The GPDMA controller allows peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master or one area by each master.

The GPDMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

6.9.1 DMA support for peripherals

The GPDMA supports the following peripherals: SPI0/1/2 and UART0/1. The GPDMA can access both embedded SRAM blocks, both TCMs, external static memory, and flash memory.

6.9.2 Clock description

The DMA controller is clocked by CLK_SYS_DMA derived from BASE_SYS_CLK, see Section 6.7.2.

6.10 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the Host controller.

The LPC2921/2923/2925 USB interface includes a device controller with on-chip PHY for device. Details on typical USB interfacing solutions can be found in Section 10.2.

6.10.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

- Set HIGH on match.
- Toggle on match.
- Do nothing on match.

- Pause input pin (MSCSS timers only).

The timers are designed to count cycles of the clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. They also include capture inputs to trap the timer value when an input signal changes state, optionally generating an interrupt. The core function of the timers consists of a 32 bit prescale counter triggering the 32 bit timer counter. Both counters run on clock CLK_TMRx (x runs from 0 to 3) and all time references are related to the period of this clock. Note that each timer has its individual clock source within the Peripheral SubSystem. In the Modulation and Sampling SubSystem each timer also has its own individual clock source. See Section 6.15.5 for information on generation of these clocks.

6.12.3.1 Pin description

The four timers in the peripheral subsystem of the LPC2921/2923/2925 have the pins described below. The two timers in the modulation and sampling subsystem have no external pins except for the pause pin on MSCSS timer 1. See Section 6.14.6 for a description of these timers and their associated pins. The timer pins are combined with other functions on the port pins of the LPC2921/2923/2925, see Section 6.11.3. Table Table 13 shows the timer pins (x runs from 0 to 3).

Table 13. Timer pins

Symbol	Pin name	Direction	Description
TIMERx CAP[0]	CAPx[0]	IN	TIMERx capture input 0[1]
TIMERx CAP[1]	CAPx[1]	IN	TIMERx capture input 1[1]
TIMERx CAP[2]	CAPx[2]	IN	TIMERx capture input 2
TIMERx CAP[3]	CAPx[3]	IN	TIMERx capture input 3
TIMERx MAT[0]	MATx[0]	OUT	TIMERx match output 0
TIMERx MAT[1]	MATx[1]	OUT	TIMERx match output 1
TIMERx MAT[2]	MATx[2]	OUT	TIMERx match output 2
TIMERx MAT[3]	MATx[3]	OUT	TIMERx match output 3

[1] Note that CAP1[0] and CAP1[1] are not pinned out on Timer1.

6.12.3.2 Clock description

The timer modules are clocked by two different clocks; CLK_SYS_PESS and CLK_TMRx (x = 0 to 3), see Section 6.7.2. Note that each timer has its own CLK_TMRx branch clock for power management. The frequency of all these clocks is identical as they are derived from the same base clock BASE_CLK_TMR. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_TMRx.

6.12.4 UARTs

The LPC2921/2923/2925 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs.

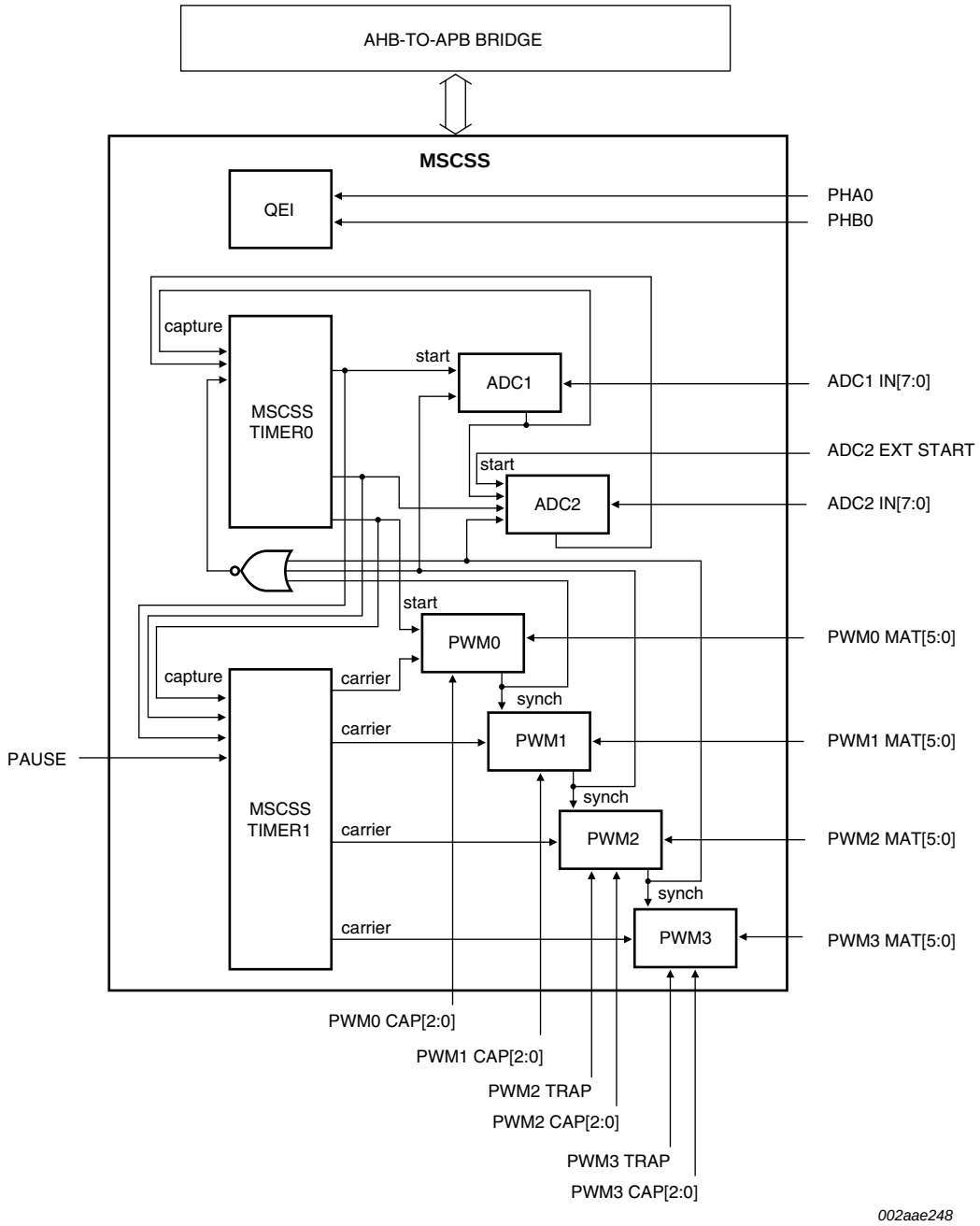


Fig 5. Modulation and Sampling Control SubSystem (MSCSS) block diagram

6.14.2 Pin description

The pins of the LPC2921/2923/2925 MSCSS associated with the two ADC modules are described in Section 6.14.4.2. Pins connected to the four PWM modules are described in Section 6.14.5.4, pins directly connected to the MSCSS timer 1 module are described in Section 6.14.6.1, and pins connected to the quadrature encoder interface are described in Section 6.14.7.1.

A mechanism is provided to modify configuration of the ADC and control the moment at which the updated configuration is transferred to the ADC domain.

The ADC clock is limited to 4.5 MHz maximum frequency and should always be lower than or equal to the system clock frequency. To meet this constraint or to select the desired lower sampling frequency, the clock generation unit provides a programmable fractional system-clock divider dedicated to the ADC clock. Conversion rate is determined by the ADC clock frequency divided by the number of resolution bits plus one. Accessing ADC registers requires an enabled ADC clock, which is controllable via the clock generation unit, see Section 6.15.2.

Each ADC has four start inputs. Note that start 0 and start 2 are captured in the system clock domain while start 1 and start 3 are captured in the ADC domain. The start inputs are connected at MSCSS level, see Section 6.14 for details.

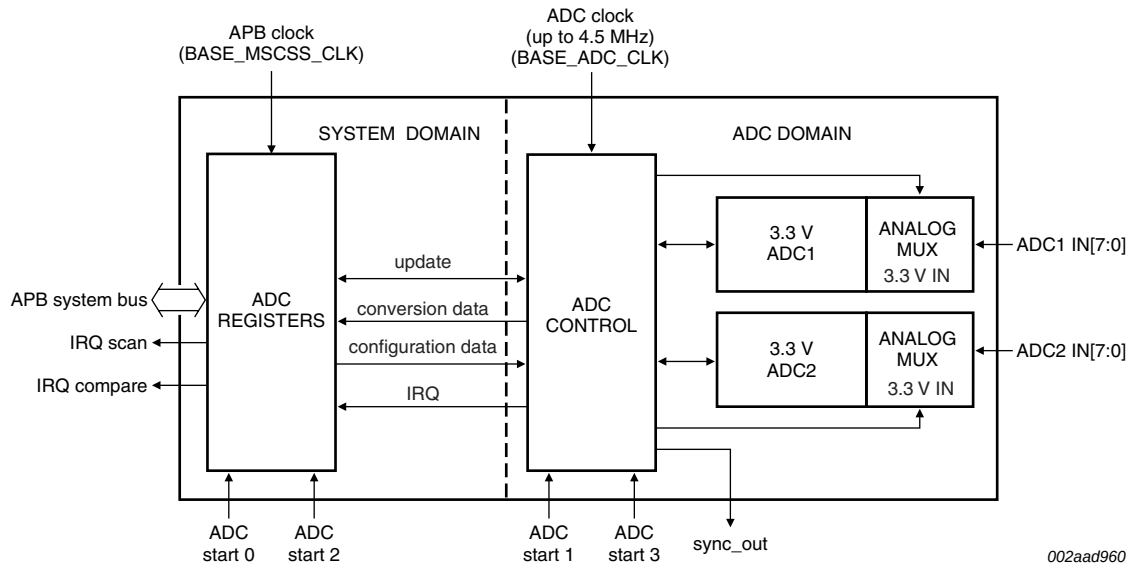


Fig 6. ADC block diagram

6.14.4.2 Pin description

The two ADC modules in the MSCSS have the pins described below. The ADCx input pins are combined with other functions on the port pins of the LPC2921/2923/2925. The VREFN and VREFP pins are common for both ADCs. Table 20 shows the ADC pins.

Table 20. Analog to digital converter pins

Symbol	Pin name	Direction	Description
ADC1/2 IN[7:0]	IN1/2[7:0]	IN	analog input for 3.3 V ADC1/2, channel 7 to channel 0
ADC2_EXT_START	CAP1[2]	IN	ADC external start-trigger input
VREFN	VREFN	IN	ADC LOW reference level
VREFP	VREFP	IN	ADC HIGH reference level
$V_{DDA(ADC3V3)}$	$V_{DDA(ADC3V3)}$	IN	ADC1 and ADC2 3.3 V supply

Remark: Note that the ADC1 and ADC2 accept an input voltage up to of 3.6 V (see Table 31) on the ADC1/2 IN pins. If the ADC is not used, the pins are 5 V tolerant.

6.14.7.1 Pin description

The QEI module in the MSCSS has the following pins. These are combined with other functions on the port pins of the LPC2921/2923/2925. Table 23 shows the QEI pins.

Table 23. QEI pins

Symbol	Pin name	Direction	Description
QEI0 PHA	PHA0	IN	Sensor signal. Corresponds to PHA in quadrature mode and to direction in clock/direction mode.
QEI0 PHB	PHB0	IN	Sensor signal. Corresponds to PHB in quadrature mode and to clock signal in clock/direction mode.

Remark: The index function for the QEI is not pinned out on the LPC2921/2923/2925.

6.14.7.2 Clock description

The QEI module is clocked by CLK_MSCSS_QEI, see Section 6.7.2. The frequency of this clock is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

If the QEI is not used its CLK_MSCSS_QEI branch clock can be switched off.

6.15 Power, Clock, and Reset control SubSystem (PCRSS)

The Power, Clock, and Reset control SubSystem (PCRSS) in the LPC2921/2923/2925 includes a Clock Generator Unit (CGU), a Reset Generator Unit (RGU) and a Power Management Unit (PMU).

Figure 8 provides an overview of the PCRSS. An AHB-to-DTL bridge controls the communication with the AHB system bus.

6.15.2 Clock Generation Unit (CGU0)

The key features are:

- Generation of 11 base clocks selectable from several embedded clock sources.
- Crystal oscillator with power-down.
- Control PLL with power-down.
- Very low-power ring oscillator, always on to provide a safe clock.
- Seven fractional clock dividers with L/D division.
- Individual source selector for each base clock, with glitch-free switching.
- Autonomous clock-activity detection on every clock source.
- Protection against switching to invalid or inactive clock sources.
- Embedded frequency counter.
- Register write-protection mechanism to prevent unintentional alteration of clocks.

Remark: Any clock-frequency adjustment has a direct impact on the timing of all on-board peripherals.

6.15.2.1 Functional description

The clock generation unit provides 11 internal clock sources as described in Table 24.

Table 24. CGU0 base clocks

Number	Name	Frequency (MHz) [1]	Description
0	BASE_SAFE_CLK	0.4	base safe clock (always on)
1	BASE_SYS_CLK	125	base system clock
2	BASE_PCR_CLK	0.4 [2]	base PCR subsystem clock
3	BASE_IVNSS_CLK	125	base IVNSS subsystem clock
4	BASE_MSCSS_CLK	125	base MSCSS subsystem clock
5	BASE_ICLK0_CLK	125	base internal clock 0, for CGU1
6	BASE_UART_CLK	125	base UART clock
7	BASE_SPI_CLK	50	base SPI clock
8	BASE_TMR_CLK	125	base timers clock
9	BASE_ADC_CLK	4.5	base ADCs clock
10	reserved	-	-
11	BASE_ICLK1_CLK	125	base internal clock 1, for CGU1

[1] Maximum frequency that guarantees stable operation of the LPC2921/2923/2925.

[2] Fixed to low-power oscillator.

For generation of these base clocks, the CGU consists of primary and secondary clock generators and one output generator for each base clock.

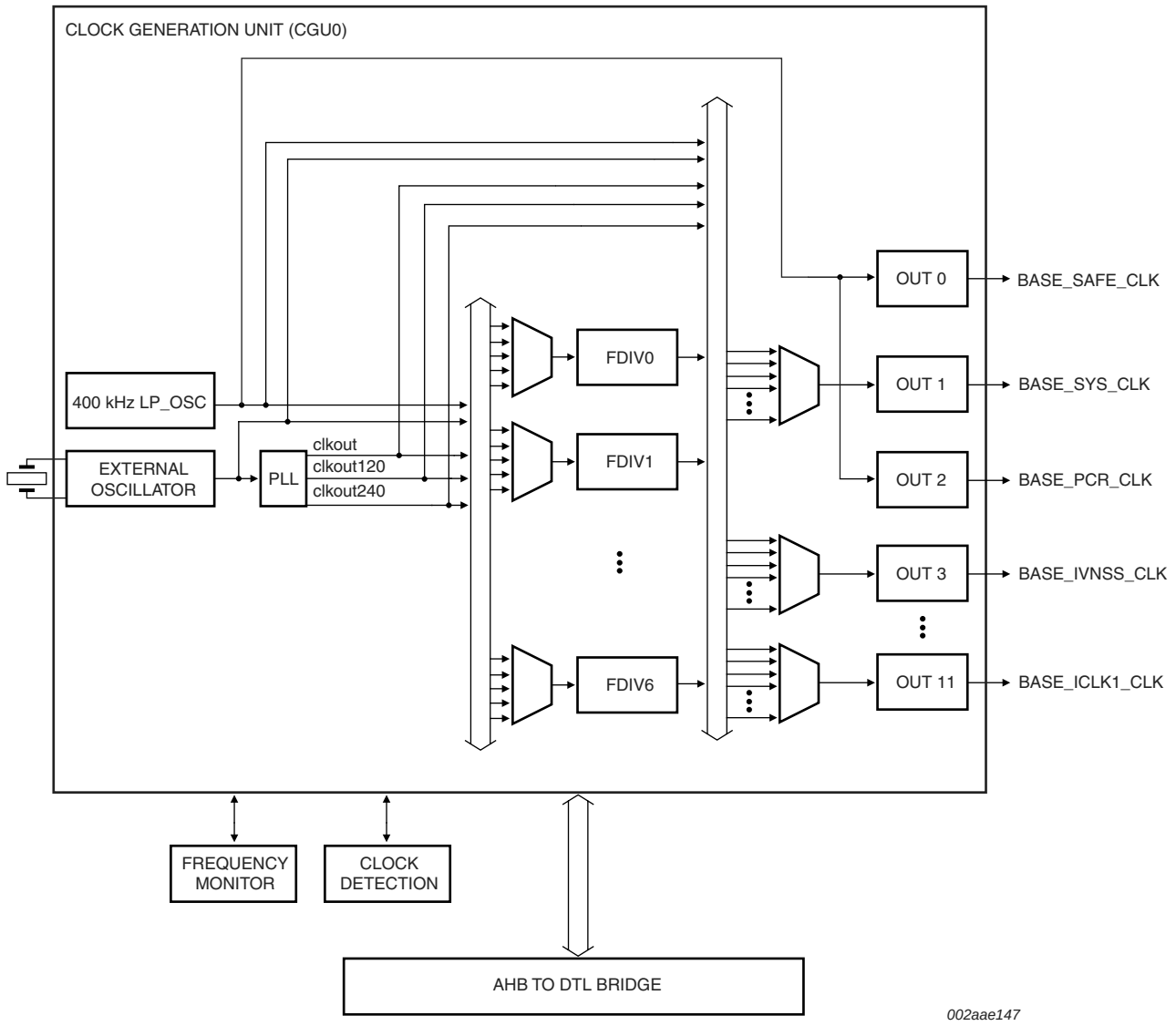


Fig 9. Block diagram of the CGU0 (see Table 24 for all base clocks)

There are two primary clock generators: a low-power ring oscillator (LP_OSC) and a crystal oscillator. See Figure 9.

LP_OSC is the source for the BASE_PCR_CLK that clocks the CGU itself and for BASE_SAFE_CLK that clocks a minimum of other logic in the device (like the watchdog timer). To prevent the device from losing its clock source LP_OSC cannot be put into power-down. The crystal oscillator can be used as source for high-frequency clocks or as an external clock input if a crystal is not connected.

Secondary clock generators are a PLL and seven fractional dividers (FDIV[0:6]). The PLL has three clock outputs: normal, 120° phase-shifted and 240° phase-shifted.

7. Limiting values

Table 30. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Supply pins						
P_{tot}	total power dissipation		[1]	-	1.5	W
$V_{DD(CORE)}$	core supply voltage			−0.5	+2.0	V
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			−0.5	+2.0	V
$V_{DDA(ADC3V3)}$	3.3 V ADC analog supply voltage			−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage			−0.5	+4.6	V
I_{DD}	supply current	average value per supply pin	[2]	-	98	mA
I_{SS}	ground current	average value per ground pin	[2]	-	98	mA
Input pins and I/O pins						
V_{XIN_OSC}	voltage on pin XIN_OSC			−0.5	+2.0	V
$V_{I(IO)}$	I/O input voltage		[3][4][5]	−0.5	$V_{DD(IO)}$ + 3.0	V
$V_{I(ADC)}$	ADC input voltage	for ADC1/2: I/O port 0 pin 8 to pin 23.	[4][5]	−0.5	$V_{DDA(ADC3V3)}$ + 0.5	V
V_{VREFP}	voltage on pin VREFP			−0.5	+3.6	V
V_{VREFN}	voltage on pin VREFN			−0.5	+3.6	V
$I_{I(ADC)}$	ADC input current	average value per input pin	[2]	-	35	mA
Output pins and I/O pins configured as output						
I_{OHS}	HIGH-level short-circuit output current	drive HIGH, output shorted to $V_{SS(IO)}$	[6]	-	−33	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW, output shorted to $V_{DD(IO)}$	[6]	-	+38	mA
General						
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

Table 31. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LIH}	HIGH-level input leakage current		-	-	1	μA
I_{LIL}	LOW-level input leakage current		-	-	1	μA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V; see Figure 20	25	50	100	μA
$I_{I(pu)}$	pull-up input current	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed; Figure 21	−25	−50	−115	μA
C_i	input capacitance	[5]	-	3	8	pF
Output pins and I/O pins configured as output						
V_O	output voltage		0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; see Figure 19	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; Figure 18	-	-	0.4	V
C_L	load capacitance		-	-	25	pF
USB pins USB_D+ and USB_D−						
Input characteristics						
V_{IH}	HIGH-level input voltage		1.5	-	-	V
V_{IL}	LOW-level input voltage		-	-	1.3	V
V_{hys}	hysteresis voltage		0.4	-	-	V
Output characteristics						
Z_o	output impedance	with 33 Ω series resistor	36.0	-	44.1	Ω
V_{OH}	HIGH-level output voltage	(driven) for low-/full-speed; R_L of 15 kΩ to GND	2.9	-	3.5	V
V_{OL}	LOW-level output voltage	(driven) for low-/full-speed; with 1.5 kΩ resistor to 3.6 V external pull-up	-	-	0.18	V
I_{OH}	HIGH-level output current	at V_{OH} = $V_{DD(IO)}$ − 0.3 V; without 33 Ω external series resistor	20.8	-	41.7	mA
		at V_{OH} = $V_{DD(IO)}$ − 0.3 V; with 33 Ω external series resistor	4.8	-	5.3	mA
I_{OL}	LOW-level output current	at V_{OL} = 0.3 V; without 33 Ω external series resistor	26.7	-	57.2	mA
		at V_{OL} = 0.3 V; with 33 Ω external series resistor	5.0	-	5.5	mA
I_{OHS}	HIGH-level short-circuit output current	drive high; pad connected to ground	-	-	90.0	mA

Table 31. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OLS}	LOW-level short-circuit output current	drive high; pad connected to $V_{DD(IO)}$		-	-	95.1	mA
Oscillator							
V_{XIN_OSC}	voltage on pin XIN_OSC			0	-	1.8	V
$R_{s(xtal)}$	crystal series resistance	f_{osc} = 10 MHz to 15 MHz	[6]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	160	Ω
		C_{xtal} = 20 pF; C_{ext} = 39 pF		-	-	60	Ω
		f_{osc} = 15 MHz to 20 MHz	[6]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	80	Ω
C_i	input capacitance	of XIN_OSC	[7]	-	-	2	pF
Power-up reset							
$V_{trip(high)}$	high trip level voltage		[8]	1.1	1.4	1.6	V
$V_{trip(low)}$	low trip level voltage		[8]	1.0	1.3	1.5	V
$V_{trip(dif)}$	difference between high and low trip level voltage		[8]	50	120	180	mV

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power-supply voltage range.

[2] Leakage current is exponential to temperature; worst-case value is at 85 °C T_{vj}. All clocks off. Analog modules and flash powered down.

[3] Not 5 V-tolerant when pull-up is on.

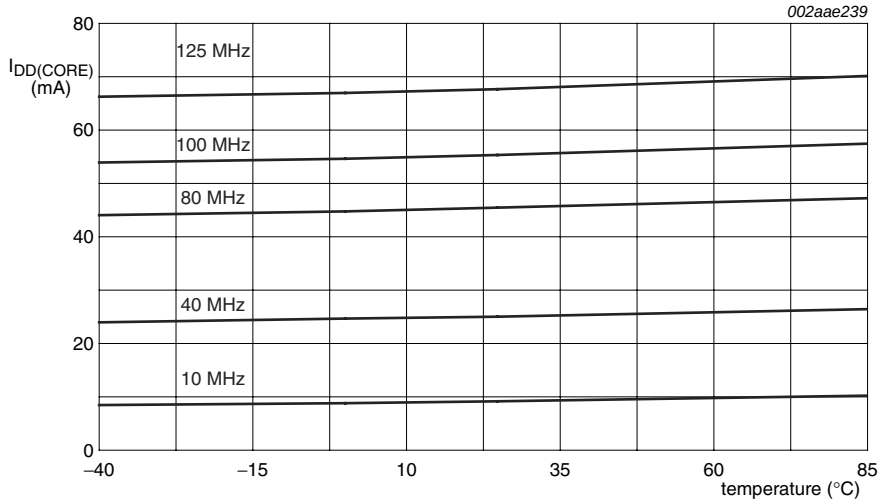
[4] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[5] For Port 0, pin 0 to pin 15 add maximum 1.5 pF for input capacitance to ADC. For Port 0, pin 16 to pin 31 add maximum 1.0 pF for input capacitance to ADC.

[6] C_{xtal} is crystal load capacitance and C_{ext} are the two external load capacitors.

[7] This parameter is not part of production testing or final testing, hence only a typical value is stated. Maximum and minimum values are based on simulation results.

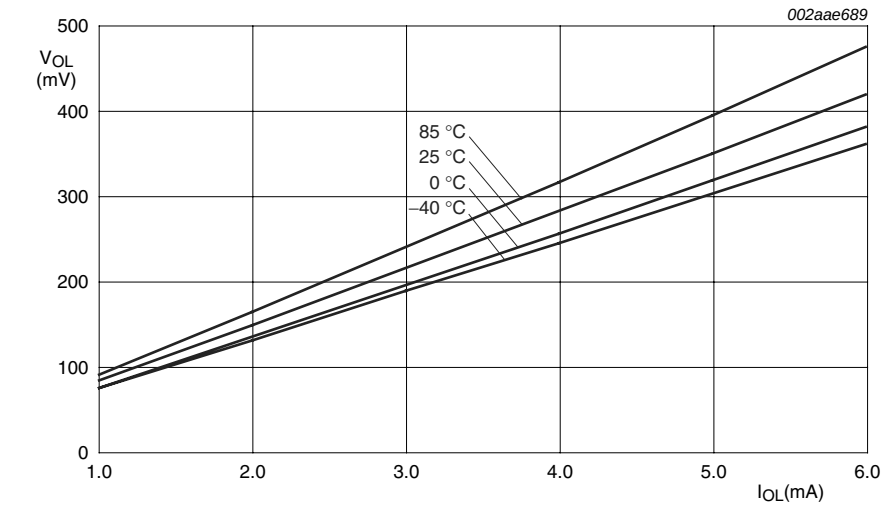
[8] The power-up reset has a time filter: $V_{DD(CORE)}$ must be above $V_{trip(high)}$ for 2 μs before reset is de-asserted; $V_{DD(CORE)}$ must be below $V_{trip(low)}$ for 11 μs before internal reset is asserted.



Conditions: active mode entered executing code from flash; core voltage 1.8 V; all peripherals enabled but not configured to run.

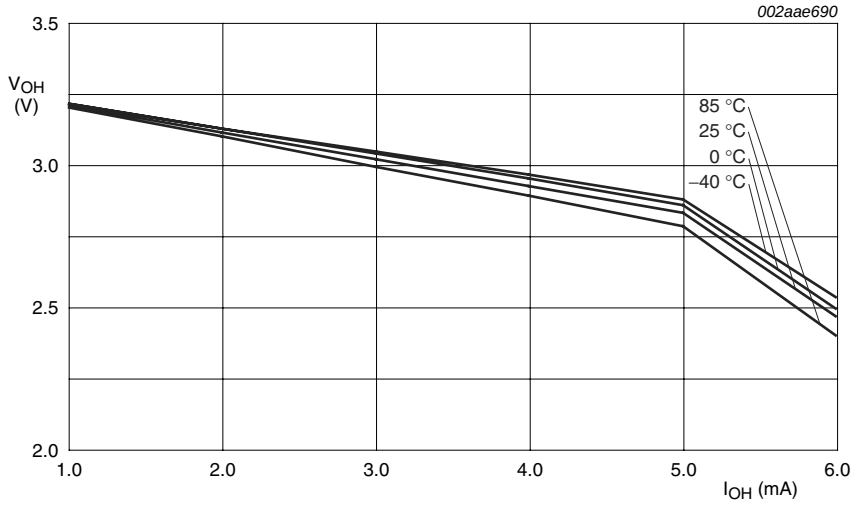
Fig 17. $I_{DD(CORE)}$ at different temperatures (active mode)

8.2 Electrical pin characteristics



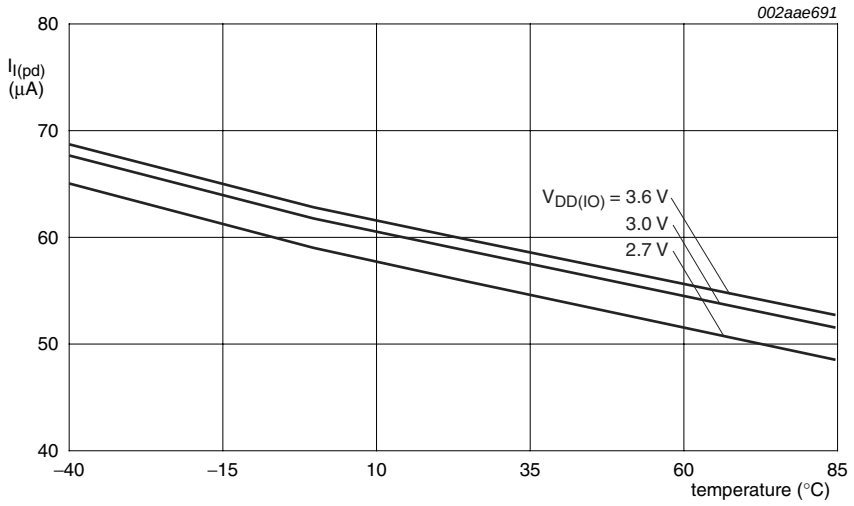
$V_{DD(IO)}$ = 3.3 V.

Fig 18. Typical LOW-level output voltage versus LOW-level output current



$V_{DD(IO)}$ = 3.3 V.

Fig 19. Typical HIGH-level output voltage versus HIGH-level output current



V_I = 3.3 V.

Fig 20. Typical pull-down current versus temperature

9.3 Dynamic characteristics: I²C-bus interface

Table 35. Dynamic characteristic: I²C-bus pins

$V_{DD(CORE)} = V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 33) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 40 and 41

Table 40. SnPb eutectic process (from J-STD-020C)

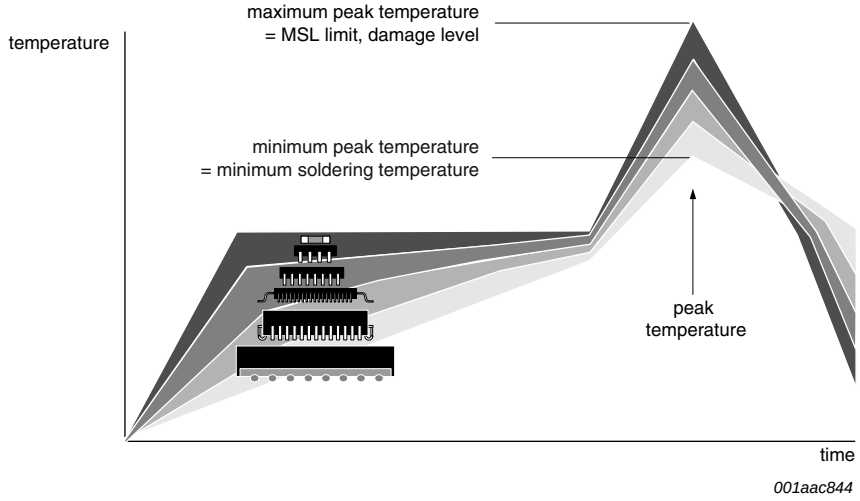
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 41. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 33.



MSL: Moisture Sensitivity Level

Fig 33. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2921_23_25_3	20100414	Product data sheet		LPC2921_23_25_2
Modifications:	• Section 1: Target market “medical” removed. • Document template updated. • USB logo added.			
LPC2921_23_25_2	20091208	Product data sheet	-	LPC2921_23_25_1
LPC2921_23_25_1	20090615	Preliminary data sheet	-	-