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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM968E-S
Core Size	32-Bit
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 1.89V
Data Converters	A/D 16x10b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2925fbd100-551

- Other peripherals:
  - Two 10-bit ADCs, 8-channels each, with 3.3 V measurement range provide 8 analog inputs each with conversion times as low as 2.44 μs per channel. Each channel provides a compare function to minimize interrupts.
  - Multiple trigger-start option for all ADCs: timer, PWM, other ADC and external signal input.
  - Four 32-bit timers each containing four capture-and-compare registers linked to I/Os.
  - Four six-channel PWMs (Pulse Width Modulators) with capture and trap functionality.
  - Two dedicated 32-bit timers to schedule and synchronize PWM and ADC.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - 32-bit watchdog with timer change protection, running on safe clock.
- Up to 60 general-purpose I/O pins with programmable pull-up, pull-down, or bus keeper.
- Vectored Interrupt Controller (VIC) with 16 priority levels.
- Up to 16 level-sensitive external interrupt pins, including USB, CAN and LIN wake-up features.
- Configurable clock out pin for driving external system clocks.
- Processor wake-up from power-down via external interrupt pins and CAN or LIN activity.
- Flexible Reset Generator Unit (RGU) able to control resets of individual modules.
- Flexible Clock-Generation Unit (CGU) able to control clock frequency of individual modules:
  - On-chip very low-power ring oscillator; fixed frequency of 0.4 MHz; always on to provide a Safe_Clock source for system monitoring.
  - On-chip crystal oscillator with a recommended operating range from 10 MHz to 25 MHz. PLL input range 10 MHz to 25 MHz.
  - On-chip PLL allows CPU operation up to a maximum CPU rate of 125 MHz.
  - Generation of up to 11 base clocks.
  - Seven fractional dividers.
- Second, dedicated CGU with its own PLL generates the USB clock and a configurable clock output.
- Highly configurable system Power Management Unit (PMU):
  - clock control of individual modules.
  - allows minimization of system operating power consumption in any configuration.
- Standard ARM test and debug interface with real-time in-circuit emulator.
- Boundary-scan test supported.
- ETM/ETB debug functions with 8 kB of dedicated SRAM also accessible for application code and data storage.
- Dual power supply:
  - CPU operating voltage: 1.8 V ± 5 %.
  - I/O operating voltage: 2.7 V to 3.6 V; inputs tolerant up to 5.5 V.
- 100-pin LQFP package.
- −40 °C to +85 °C ambient operating temperature range.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2921FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2923FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2925FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

3.1 Ordering options

Table 2. Part options

Type number	Flash memory	SRAM (incl. ETB SRAM)	USB device	UART RS-485	LIN 2.0/ UART	CAN	Package
LPC2921FBD100	128 kB	24 kB	yes	2	2	2	LQFP100
LPC2923FBD100	256 kB	24 kB	yes	2	2	2	LQFP100
LPC2925FBD100	512 kB	40 kB	yes	2	2	2	LQFP100

Table 3. LQFP100 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
$V_{DDA(ADC3V3)}$	74	3.3 V power supply for ADC			
JTAGSEL	75[1]	TAP controller select input; LOW-level selects the ARM debug mode; HIGH-level selects boundary scan; pulled up internally.			
n.c.	76	not connected to a function; must be tied to 3.3 V power supply for ADC $V_{DDA(ADC3V3)}$.			
VREFP	77[3]	HIGH reference for ADC			
VREFN	78[3]	LOW reference for ADC			
P0[8]/IN1[0]	79[4]	GPIO0, pin 8	ADC1 IN0	-	-
P0[9]/IN1[1]	80[4]	GPIO0, pin 9	ADC1 IN1	-	-
P0[10]/IN1[2]/ PMAT1[0]	81[4]	GPIO0, pin 10	ADC1 IN2	PWM1 MAT0	-
P0[11]/IN1[3]/ PMAT1[1]	82[4]	GPIO0, pin 11	ADC1 IN3	PWM1 MAT1	-
$V_{SS(IO)}$	83	ground for I/O			
P0[12]/IN1[4]/ PMAT1[2]	84[4]	GPIO0, pin 12	ADC1 IN4	PWM1 MAT2	-
P0[13]/IN1[5]/ PMAT1[3]	85[4]	GPIO0, pin 13	ADC1 IN5	PWM1 MAT3	-
P0[14]/IN1[6]/ PMAT1[4]	86[4]	GPIO0, pin 14	ADC1 IN6	PWM1 MAT4	-
P0[15]/IN1[7]/ PMAT1[5]	87[4]	GPIO0, pin 15	ADC1 IN7	PWM1 MAT5	-
P0[16]IN2[0]/TXD0	88[4]	GPIO0, pin 16	ADC2 IN0	UART0 TXD	-
P0[17]/IN2[1]/ RXD0/A23	89[4]	GPIO0, pin 17	ADC2 IN1	UART0 RXD	-
$V_{DD(CORE)}$	90	1.8 V power supply for digital core			
$V_{SS(CORE)}$	91	ground for digital core			
$V_{DD(IO)}$	92	3.3 V power supply for I/O			
P0[18]/IN2[2]/ PMAT2[0]	93[4]	GPIO0, pin 18	ADC2 IN2	PWM2 MAT0	-
P0[19]/IN2[3]/ PMAT2[1]	94[4]	GPIO0, pin 19	ADC2 IN3	PWM2 MAT1	-
P0[20]/IN2[4]/ PMAT2[2]	95[4]	GPIO0, pin 20	ADC2 IN4	PWM2 MAT2	-
P0[21]/IN2[5]/ PMAT2[3]	96[4]	GPIO0, pin 21	ADC2 IN5	PWM2 MAT3	-
P0[22]/IN2[6]/ PMAT2[4]/A18	97[4]	GPIO0, pin 22	ADC2 IN6	PWM2 MAT4	-
$V_{SS(IO)}$	98	ground for I/O			

Table 3. LQFP100 pin assignment *...continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P0[23]/IN2[7]/ PMAT2[5]/A19	99[4]	GPIO0, pin 23	ADC2 IN7	PWM2 MAT5	-
TDI	100[1]	IEEE 1149.1 data in, pulled up internally			

[1] Bidirectional pad; analog port; plain input; 3-state output; slew rate control; 5 V tolerant; TTL with hysteresis; programmable pull-up/pull-down/repeater.

[2] USB pad.

[3] Analog pad; analog I/O.

[4] Analog I/O pad.

6. Functional description

6.1 Architectural overview

The LPC2921/2923/2925 consists of:

- An ARM968E-S processor with real-time emulation support
- An AMBA multilayer Advanced High-performance Bus (AHB) for interfacing to the on-chip memory controllers
- Two DTL buses (an universal NXP interface) for interfacing to the interrupt controller and the Power, Clock and Reset control SubSystem (PCRSS).
- Three ARM Peripheral Buses (APB - a compatible super set of ARM's AMBA advanced peripheral bus) for connection to on-chip peripherals clustered in subsystems.
- One ARM Peripheral Bus for event router and system control.

The LPC2921/2923/2925 configures the ARM968E-S processor in little-endian byte order. All peripherals run at their own clock frequency to optimize the total system power consumption. The AHB-to-APB bridge used in the subsystems contains a write-ahead buffer one transaction deep. This implies that when the ARM968E-S issues a buffered write action to a register located on the APB side of the bridge, it continues even though the actual write may not yet have taken place. Completion of a second write to the same subsystem will not be executed until the first write is finished.

6.2 ARM968E-S processor

The ARM968E-S is a general purpose 32-bit RISC processor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective controller core.

Amongst the most compelling features of the ARM968E-S are:

- Separate directly connected instruction and data Tightly Coupled Memory (TCM) interfaces.

- Write buffers for the AHB and TCM buses.
- Enhanced 16 × 32 multiplier capable of single-cycle MAC operations and 16-bit fixed-point DSP instructions to accelerate signal-processing algorithms and applications.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. The ARM968E-S is based on the ARMv5TE five-stage pipeline architecture. Typically, in a three-stage pipeline architecture, while one instruction is being executed its successor is being decoded and a third instruction is being fetched from memory. In the five-stage pipeline additional stages are added for memory access and write-back cycles.

The ARM968E-S processor also employs a unique architectural strategy known as THUMB, which makes it ideally suited to high-volume applications with memory restrictions or to applications where code density is an issue.

The key idea behind THUMB is that of a super-reduced instruction set. Essentially, the ARM968E-S processor has two instruction sets:

- Standard 32-bit ARMv5TE set
- 16-bit THUMB set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit controller using 16-bit registers. This is possible because THUMB code operates on the same 32-bit register set as ARM code.

THUMB code can provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM controller connected to a 16-bit memory system.

The ARM968E-S processor is described in detail in the ARM968E-S data sheet Ref. 2.

6.3 On-chip flash memory system

The LPC2921/2923/2925 includes a 128 kB, 256 kB, or 512 kB flash memory system. This memory can be used for both code and data storage. Programming of the flash memory can be accomplished via the flash memory controller or the JTAG.

The flash controller also supports a 16 kB, byte-accessible on-chip EEPROM integrated on the LPC2921/2923/2925.

6.4 On-chip static RAM

In addition to the two 16 kB TCMs, the LPC2921/2923/2925 includes two static RAM memories of 16 kB each for a total of 32 kB (LPC2925 only) or one block of 16 kB (LPC2921/2923). They may be used for code and/or data storage.

The 8 kB SRAM block for the ETB can be used as static memory for code and data storage as well. However, DMA access to this memory region is not supported.

6.5 Memory map

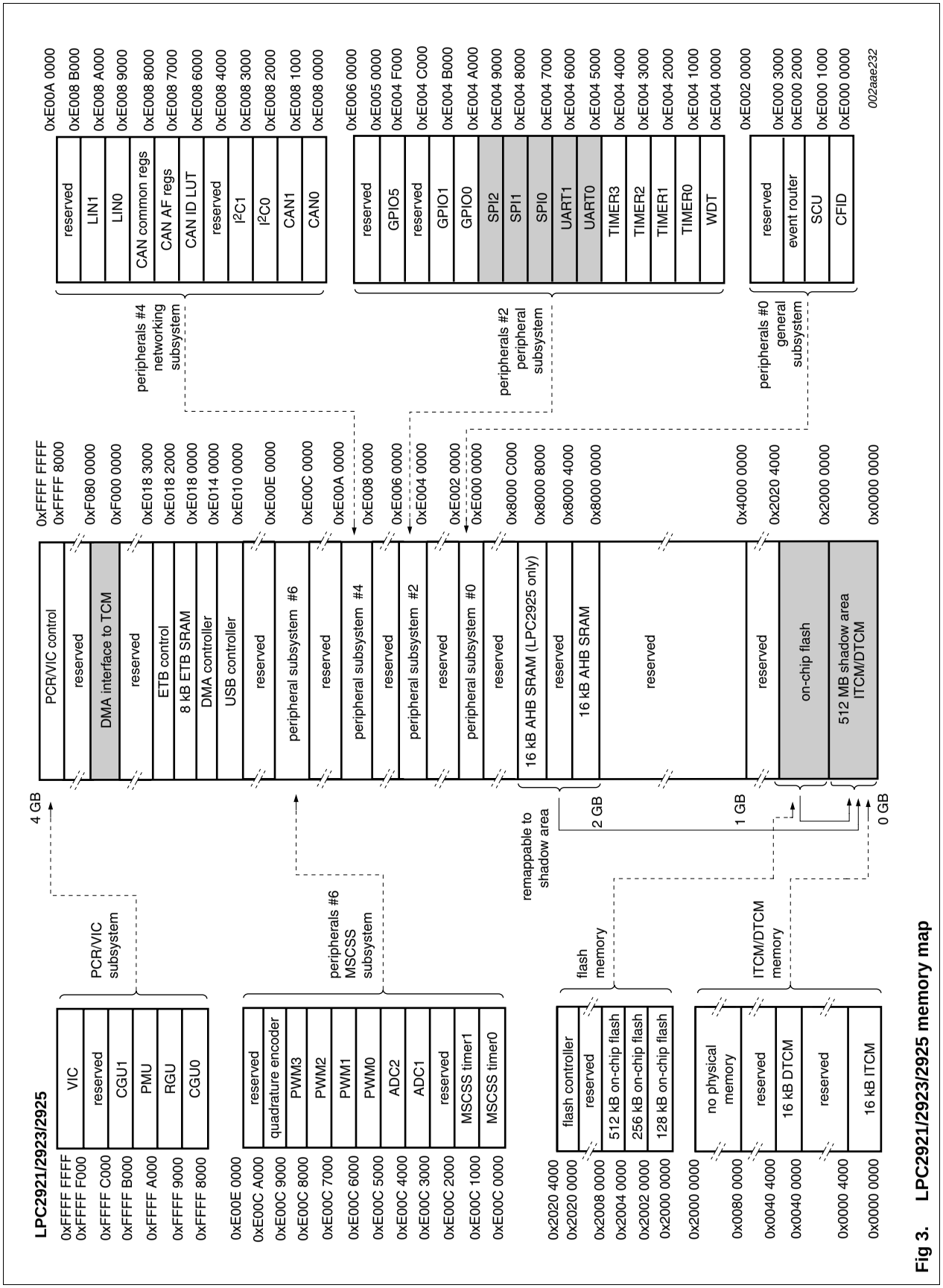


Fig 3. LPC2921/2923/2925 memory map

- Watchdog control register change-protected with key
- Programmable 32-bit watchdog timer period with programmable 32-bit prescaler.

6.12.2.1 Functional description

The watchdog timer consists of a 32-bit counter with a 32-bit prescaler.

The watchdog should be programmed with a time-out value and then periodically restarted. When the watchdog times out, it generates a reset through the RGU.

To generate watchdog interrupts in watchdog debug mode the interrupt has to be enabled via the interrupt enable register. A watchdog-overflow interrupt can be cleared by writing to the clear-interrupt register.

Another way to prevent resets during debug mode is via the Pause feature of the watchdog timer. The watchdog is stalled when the ARM9 is in debug mode and the PAUSE_ENABLE bit in the watchdog timer control register is set.

The Watchdog Reset output is fed to the Reset Generator Unit (RGU). The RGU contains a reset source register to identify the reset source when the device has gone through a reset. See Section 6.15.4.

6.12.2.2 Clock description

The watchdog timer is clocked by two different clocks; CLK_SYS_PESS and CLK_SAFE, see Section 6.7.2. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_SAFE which is always on.

6.12.3 Timer

The LPC2921/2923/2925 contains six identical timers: four in the peripheral subsystem and two in the Modulation and Sampling Control SubSystem (MSCSS) located at different peripheral base addresses. This section describes the four timers in the peripheral subsystem. Each timer has four capture inputs and/or match outputs. Connection to device pins depends on the configuration programmed into the port function-select registers. The two timers located in the MSCSS have no external capture or match pins, but the memory map is identical, see Section 6.14.6. One of these timers has an external input for a pause function.

The key features are:

- 32-bit timer/counter with programmable 32-bit prescaler.
- Up to four 32-bit capture channels per timer. These take a snapshot of the timer value when an external signal connected to the TIMERx CAPn input changes state. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.

6.12.5.3 Clock description

The SPI modules are clocked by two different clocks; CLK_SYS_PESS and CLK_SPIx (x = 0, 1, 2), see Section 6.7.2. Note that each SPI has its own CLK_SPIx branch clock for power management. The frequency of all clocks CLK_SPIx is identical as they are derived from the same base clock BASE_CLK_SPI. The register interface towards the system bus is clocked by CLK_SYS_PESS. The serial-clock rate divisor is clocked by CLK_SPIx.

The SPI clock frequency can be controlled by the CGU. In master mode the SPI clock frequency (CLK_SPIx) must be set to at least twice the SPI serial clock rate on the interface. In slave mode CLK_SPIx must be set to four times the SPI serial clock rate on the interface.

6.12.6 General-purpose I/O

The LPC2921/2923/2925 contains two general-purpose I/O ports located at different peripheral base addresses. All I/O pins are bidirectional, and the direction can be programmed individually. The I/O pad behavior depends on the configuration programmed in the port function-select registers.

The key features are:

- General-purpose parallel inputs and outputs.
- Direction control of individual bits.
- Synchronized input sampling for stable input-data values.
- All I/O pins default to input at reset to avoid any possible bus conflicts.

6.12.6.1 Functional description

The general-purpose I/O provides individual control over each bidirectional port pin. There are two registers to control I/O direction and output level. The inputs are synchronized to achieve stable read-levels.

To generate an open-drain output, set the bit in the output register to the desired value. Use the direction register to control the signal. When set to output, the output driver actively drives the value on the output. When set to input, the signal floats and can be pulled up internally or externally.

6.12.6.2 Pin description

The five GPIO ports in the LPC2921/2923/2925 have the pins listed below. The GPIO pins are combined with other functions on the port pins of the LPC2921/2923/2925. Table 16 shows the GPIO pins.

Table 16. GPIO pins

Symbol	Pin name	Direction	Description
GPIO0 pin[31:0]	P0[31:0]	IN/OUT	GPIO port x pins 31 to 0
GPIO1 pin[27:0]	P1[27:0]	IN/OUT	GPIO port x pins 27 to 0
GPIO5 pin[19:18]	P5[19:18]	IN/OUT	GPIO port x pins 19 and 18

6.13.2 LIN

The LPC2921/2923/2925 contain two LIN 2.0 master controllers. These can be used as dedicated LIN 2.0 master controllers with additional support for sync break generation and with hardware implementation of the LIN protocol according to spec 2.0.

The key features are:

- Complete LIN 2.0 message handling and transfer
- One interrupt per LIN message
- Slave response time-out detection
- Programmable sync-break length
- Automatic sync-field and sync-break generation
- Programmable inter-byte space
- Hardware or software parity generation
- Automatic checksum generation
- Fault confinement
- Fractional baud rate generator

6.13.2.1 Pin description

The two LIN 2.0 master controllers in the LPC2921/2923/2925 have the pins listed below. The LIN pins are combined with other functions on the port pins of the LPC2921/2923/2925. Table 18 shows the LIN pins. For more information see Ref. 1 *subsection 3.43, LIN master controller*.

Table 18. LIN controller pins

Symbol	Pin name	Direction	Description
LIN0/1 TXD	TXDL0/1	OUT	LIN channel 0/1 transmit data output
LIN0/1 RXD	RXDL0/1	IN	LIN channel 0/1 receive data input

Remark: Both LIN channels can be also configured as UART channels.

6.13.3 I^2C-bus serial I/O controllers

The LPC2921/2923/2925 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or as a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus, and it can be controlled by more than one bus master connected to it.

The main features if the I^2C-bus interfaces are:

- I^2C0 and I^2C1 use standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus) and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.

- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- All I^2C-bus controllers support multiple address recognition and a bus monitor mode.

6.13.3.1 Pin description

Table 19. I^2C-bus pins[1]

Symbol	Pin name	Direction	Description
I2C SCL0/1	SCL0/1	I/O	I^2C clock input/output
I2C SDA0/1	SDA0/1	I/O	I^2C data input/output

[1] Note that the pins are not I^2C-bus compliant open-drain pins.

6.14 Modulation and Sampling Control SubSystem (MSCSS)

The Modulation and Sampling Control Subsystem (MSCSS) in the LPC2921/2923/2925 includes four Pulse Width Modulators (PWMs), two 10-bit successive approximation Analog-to-Digital Converters (ADCs) and two timers.

The key features of the MSCSS are:

- Two 10-bit, 400 ksample/s, 8-channel ADCs with 3.3 V inputs and various trigger-start options.
- Four 6-channel PWMs (Pulse Width Modulators) with capture and trap functionality.
- Two dedicated timers to schedule and synchronize the PWMs and ADCs.
- Quadrature encoder interface.

6.14.1 Functional description

The MSCSS contains Pulse Width Modulators (PWMs), Analog-to-Digital Converters (ADCs) and timers.

Figure 5 provides an overview of the MSCSS. An AHB-to-APB bus bridge takes care of communication with the AHB system bus. Two internal timers are dedicated to this subsystem. MSCSS timer 0 can be used to generate start pulses for the ADCs and the first PWM. The second timer (MSCSS timer 1) is used to generate ‘carrier’ signals for the PWMs. These carrier patterns can be used, for example, in applications requiring current control. Several other trigger possibilities are provided for the ADCs (external, cascaded or following a PWM). The capture inputs of both timers can also be used to capture the start pulse of the ADCs.

Remark: The IDX0 function for the QEI, the external start function for ADC1, and the TRAP0/1 functions for the PWM0/1 are not pinned out on the LPC2921/2923/2925.

6.14.3 Clock description

The MSCSS is clocked from a number of different sources:

- CLK_SYS_MSCSS_A clocks the AHB side of the AHB-to-APB bus bridge
- CLK_MSCSS_APB clocks the subsystem APB bus
- CLK_MSCSS_MTMR0/1 clocks the timers
- CLK_MSCSS_PWM[0:3] clocks the PWMs.

Each ADC has two clock areas; an APB part clocked by CLK_MSCSS_ADCx_APB (x = 1 or 2) and a control part for the analog section clocked by CLK_ADCx = 1 or 2), see Section 6.7.2.

All clocks are derived from the BASE_MSCSS_CLK, except for CLK_SYS_MSCSS_A which is derived form BASE_SYS_CLK, and the CLK_ADCx clocks which are derived from BASE_CLK_ADC. If specific PWM or ADC modules are not used their corresponding clocks can be switched off.

6.14.4 Analog-to-digital converter

The MSCSS in the LPC2921/2923/2925 includes two 10-bit successive-approximation analog-to-digital converters.

The key features of the ADC interface module are:

- ADC1 and ADC2: Eight analog inputs; time-multiplexed; measurement range up to 3.3 V.
- External reference-level inputs.
- 400 ksamples per second at 10-bit resolution up to 1500 ksamples per second at 2-bit resolution.
- Programmable resolution from 2-bit to 10-bit.
- Single analog-to-digital conversion scan mode and continuous analog-to-digital conversion scan mode.
- Optional conversion on transition on external start input, timer capture/match signal, PWM_sync or ‘previous’ ADC.
- Converted digital values are stored in a register for each channel.
- Optional compare condition to generate a ‘less than’ or an ‘equal to or greater than’ compare-value indication for each channel.
- Power-down mode.

6.14.4.1 Functional description

The ADC block diagram, Figure 6, shows the basic architecture of each ADC. The ADC functionality is divided into two major parts; one part running on the MSCSS Subsystem clock, the other on the ADC clock. This split into two clock domains affects the behavior from a system-level perspective. The actual analog-to-digital conversions take place in the ADC clock domain, but system control takes place in the system clock domain.

- Motor controller: The PWM provides multi-phase outputs, and these outputs can be controlled to have a certain pattern sequence. In this way the force/torque of the motor can be adjusted as desired. This makes the PWM function as a motor drive.

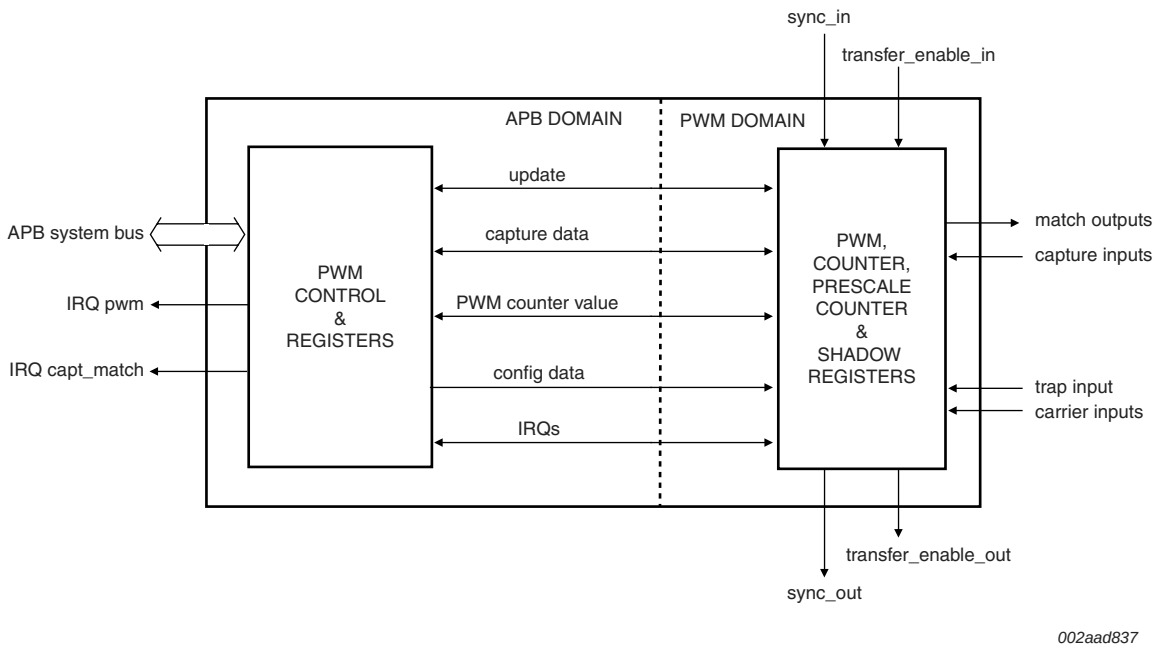


Fig 7. PWM block diagram

The PWM block diagram in Figure 7 shows the basic architecture of each PWM. PWM functionality is split into two major parts, a APB domain and a PWM domain, both of which run on clocks derived from the BASE_MSCSS_CLK. This split into two domains affects behavior from a system-level perspective. The actual PWM and prescale counters are located in the PWM domain but system control takes place in the APB domain.

The actual PWM consists of two counters; a 16-bit prescale counter and a 16-bit PWM counter. The position of the rising and falling edges of the PWM outputs can be programmed individually. The prescale counter allows high system bus frequencies to be scaled down to lower PWM periods. Registers are available to capture the PWM counter values on external events.

Note that in the Modulation and Sampling Control SubSystem (MSCSS), each PWM has its individual clock source CLK_MSCSS_PWMx (x runs from 0 to 3). Both the prescale and the timer counters within each PWM run on this clock CLK_MSCSS_PWMx, and all time references are related to the period of this clock. See Section 6.15 for information on generation of these clocks.

6.14.5.2 Synchronizing the PWM counters

A mechanism is included to synchronize the PWM period to other PWMs by providing a sync input and a sync output with programmable delay. Several PWMs can be synchronized using the trans_enable_in/trans_enable_out and sync_in/sync_out ports. See Figure 5 for details of the connections of the PWM modules within the MSCSS in the LPC2921/2923/2925. PWM0 can be master over PWM1; PWM1 can be master over PWM2, etc.

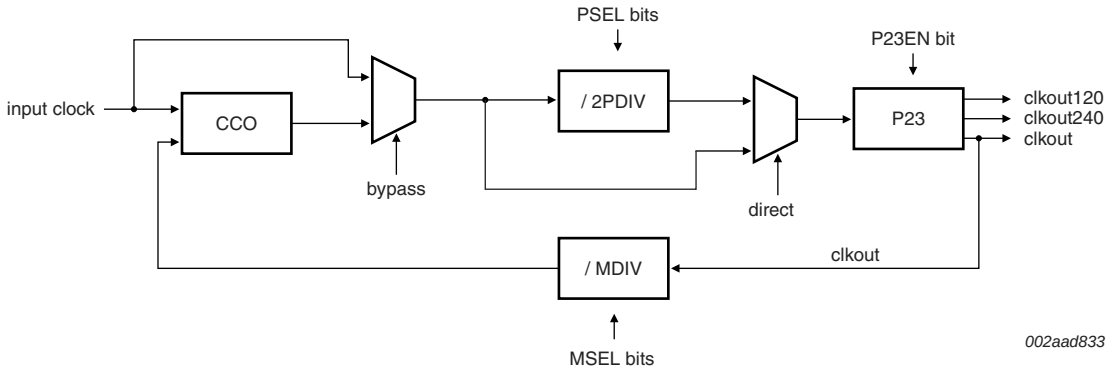


Fig 11. PLL block diagram

Triple output phases: For applications that require multiple clock phases two additional clock outputs can be enabled by setting register P23EN to logic 1, thus giving three clocks with a 120° phase difference. In this mode all three clocks generated by the analog section are sent to the output dividers. When the PLL has not yet achieved lock the second and third phase output dividers run unsynchronized, which means that the phase relation of the output clocks is unknown. When the PLL LOCK register is set the second and third phase of the output dividers are synchronized to the main output clock CLKOUT PLL, thus giving three clocks with a 120° phase difference.

Direct output mode: In normal operating mode (with DIRECT set to logic 0) the CCO clock is divided by 2, 4, 8 or 16 depending on the value on the PSEL[1:0] input, giving an output clock with a 50 % duty cycle. If a higher output frequency is needed the CCO clock can be sent directly to the output by setting DIRECT to logic 1. Since the CCO does not directly generate a 50 % duty cycle clock, the output clock duty cycle in this mode can deviate from 50 %.

Power-down control: A Power-down mode has been incorporated to reduce power consumption when the PLL clock is not needed. This is enabled by setting the PD control register bit. In this mode the analog section of the PLL is turned off, the oscillator and the phase-frequency detector are stopped and the dividers enter a reset state. While in Power-down mode the LOCK output is low, indicating that the PLL is not in lock. When Power-down mode is terminated by clearing the PD control-register bit the PLL resumes normal operation, and makes the LOCK signal high once it has regained lock on the input clock.

6.15.2.3 Pin description

The CGU0 module in the LPC2921/2923/2925 has the pins listed in Table 25 below.

Table 25. CGU0 pins

Symbol	Direction	Description
XOUT_OSC	OUT	Oscillator crystal output
XIN_OSC	IN	Oscillator crystal input or external clock input

Table 29. Branch clock overview *…continued*

Legend:
'1' Indicates that the related register bit is tied off to logic HIGH, all writes are ignored
'0' Indicates that the related register bit is tied off to logic LOW, all writes are ignored
'+' Indicates that the related register bit is readable and writable

Branch clock name	Base clock	Implemented switch on/off mechanism		
		WAKE-UP	AUTO	RUN
CLK_UART0	BASE_UART_CLK	+	+	+
CLK_UART1	BASE_UART_CLK	+	+	+
CLK_SPI0	BASE_SPI_CLK	+	+	+
CLK_SPI1	BASE_SPI_CLK	+	+	+
CLK_SPI2	BASE_SPI_CLK	+	+	+
CLK_TMR0	BASE_TMR_CLK	+	+	+
CLK_TMR1	BASE_TMR_CLK	+	+	+
CLK_TMR2	BASE_TMR_CLK	+	+	+
CLK_TMR3	BASE_TMR_CLK	+	+	+
CLK_ADC1	BASE_ADC_CLK	+	+	+
CLK_ADC2	BASE_ADC_CLK	+	+	+
CLK_USB	BASE_USB_CLK	+	+	+

6.16 Vectored interrupt controller

The LPC2921/2923/2925 contains a very flexible and powerful Vectored Interrupt Controller (VIC) to interrupt the ARM processor on request.

The key features are:

- Level-active interrupt request with programmable polarity.
- 56 interrupt-request inputs.
- Software-interrupt request capability associated with each request input.
- Interrupt request state can be observed before masking.
- Software-programmable priority assignments to interrupt requests up to 15 levels.
- Software-programmable routing of interrupt requests towards the ARM-processor inputs IRQ and FIQ.
- Fast identification of interrupt requests through vector.
- Support for nesting of interrupt service routines.

6.16.1 Functional description

The Vectored Interrupt Controller routes incoming interrupt requests to the ARM processor. The interrupt target is configured for each interrupt request input of the VIC. The targets are defined as follows:

- Target 0 is ARM processor FIQ (fast interrupt service).
- Target 1 is ARM processor IRQ (standard interrupt service).

Interrupt-request masking is performed individually per interrupt target by comparing the priority level assigned to a specific interrupt request with a target-specific priority threshold. The priority levels are defined as follows:

- Priority level 0 corresponds to ‘masked’ (i.e. interrupt requests with priority 0 never lead to an interrupt).
- Priority 1 corresponds to the lowest priority.
- Priority 15 corresponds to the highest priority.

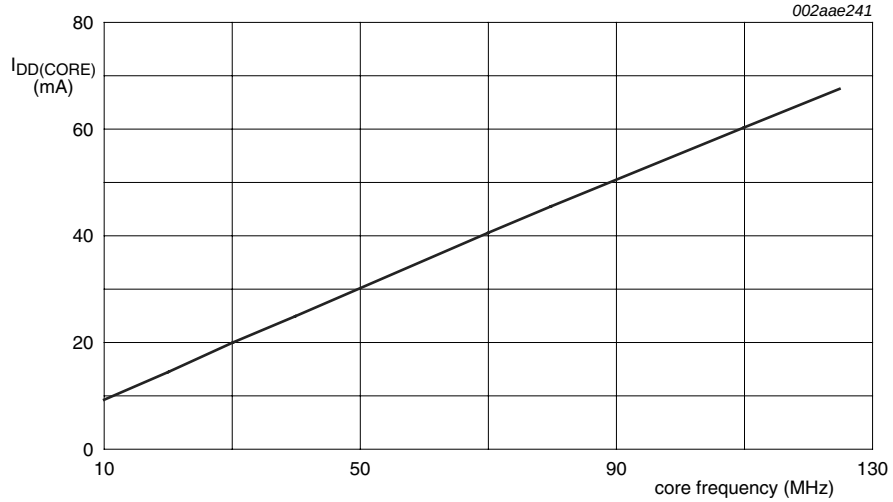
Software interrupt support is provided and can be supplied for:

- Testing RTOS (Real-Time Operating System) interrupt handling without using device-specific interrupt service routines.
- Software emulation of an interrupt-requesting device, including interrupts.

6.16.2 Clock description

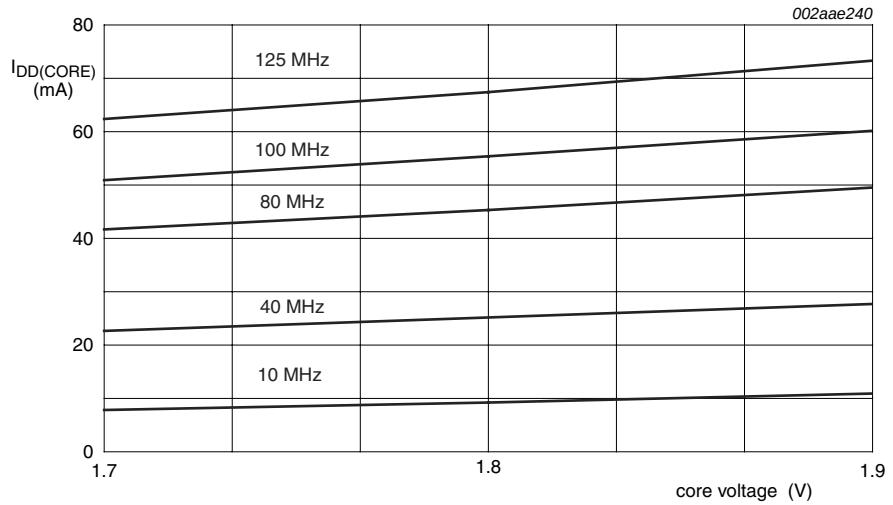
The VIC is clocked by CLK_SYS_VIC, see Section 6.7.2.

8.1 Power consumption



Conditions: T_{amb} = 25 °C; active mode entered executing code from flash; core voltage 1.8 V; all peripherals enabled but not configured to run.

Fig 15. $I_{DD(CORE)}$ at different core frequencies (active mode)



Conditions: T_{amb} = 25 °C; active mode entered executing code from flash; all peripherals enabled but not configured to run.

Fig 16. $I_{DD(CORE)}$ at different core voltages $V_{DD(CORE)}$ (active mode)

9.5 Dynamic characteristics: flash memory and EEPROM

Table 37. Flash characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{prog}	programming time	word		0.95	1	1.05	ms
t_{er}	erase time	global		95	100	105	ms
		sector		95	100	105	ms
t_{init}	initialization time			-	-	150	µs
$t_{wr(pg)}$	page write time			0.95	1	1.05	ms
$t_{fl(BIST)}$	flash word BIST time			-	38	70	ns
$t_{a(clk)}$	clock access time			-	-	63.4	ns
$t_{a(A)}$	address access time			-	-	60.3	ns

[1] Number of program/erase cycles.

Table 38. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency		200	375	400	kHz
N_{endu}	endurance		100000	500000	-	cycles
t_{ret}	retention time	powered	10	-	-	years

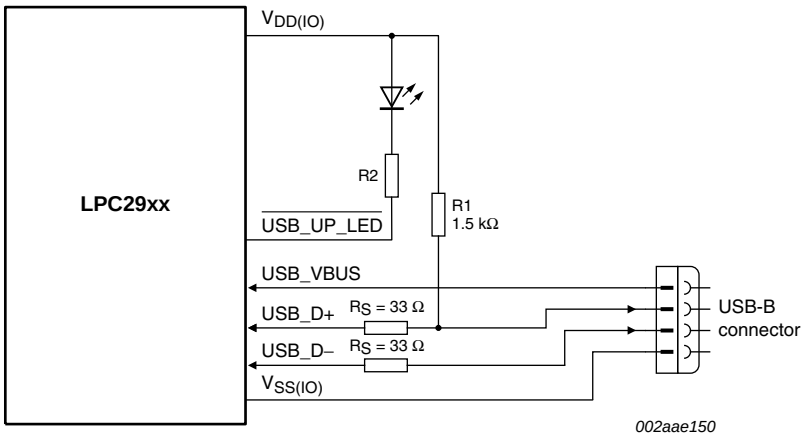


Fig 28. LPC2921/2923/2925 USB interface on a bus-powered device

10.3 SPI signal forms

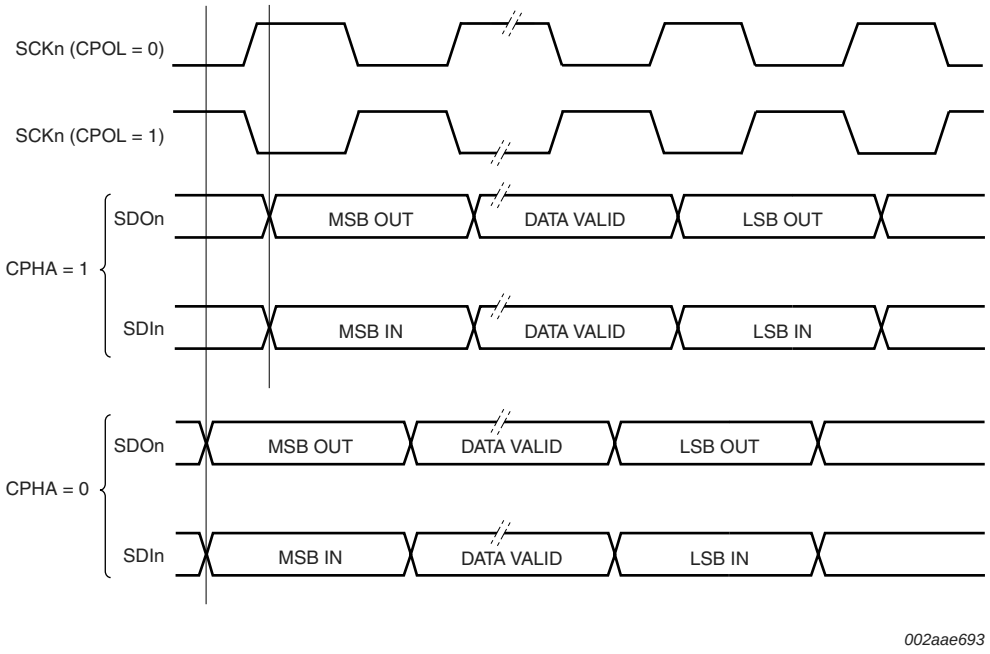


Fig 29. SPI timing in master mode

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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