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Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12xs128j1caer

Table 2-24. PTIS Register Field Descriptions

Field	Description
7-0 PTIS	**Port S input data**— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.28 Port S Data Direction Register (DDRS)

Address 0x0249 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset	0	0	0	0	0	0	0	0

Figure 2-26. Port S Data Direction Register (DDRS)

[1] Read: Anytime
Write: Anytime

Table 2-25. DDRS Register Field Descriptions

Field	Description
7-4 DDRS	**Port S data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI0 the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input
3-2 DDRS	**Port S data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI1 the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input
1-0 DDRS	**Port S data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI0 the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input

2.3.29 Port S Reduced Drive Register (RDRS)

Address 0x024A Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset	0	0	0	0	0	0	0	0

Figure 2-27. Port S Reduced Drive Register (RDRS)

1 Read: Anytime
Write: Anytime

Table 2-26. RDRS Register Field Descriptions

Field	Description
7-0 RDRS	**Port S reduced drive**—Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.30 Port S Pull Device Enable Register (PERS)

Address 0x024B Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset	1	1	1	1	1	1	1	1

Figure 2-28. Port S Pull Device Enable Register (PERS)

1 Read: Anytime
Write: Anytime

Table 2-27. PERS Register Field Descriptions

Field	Description
7-0 PERS	**Port S pull device enable**—Enable pull device on input pin or wired-or output pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has only effect if used in wired-or mode. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.3.63 Port J Polarity Select Register (PPSJ)

Address 0x026D Access: User read/write[1]

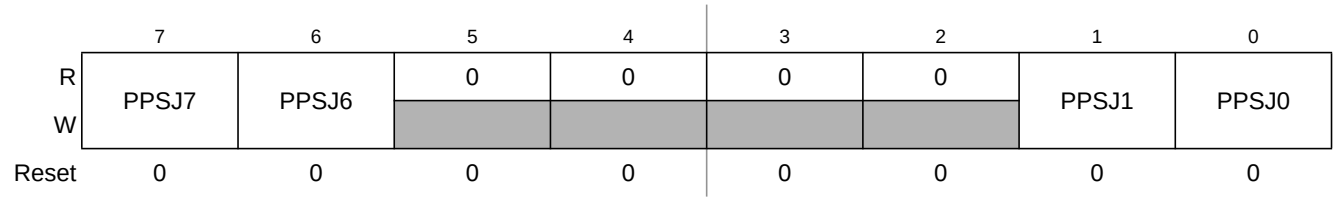

Figure 2-61. Port J Polarity Select Register (PPSJ)

[1] Read: Anytime
Write: Anytime

Table 2-60. PPSJ Register Field Descriptions

Field	Description
7-6, 1-0 PPSJ	**Port J pull device select**—Configure pull device and pin interrupt edge polarity on input pin This bit selects a pull-up or a pull-down device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge. 1 A pull-down device selected; rising edge selected 0 A pull-up device selected; falling edge selected

2.3.64 Port J Interrupt Enable Register (PIEJ)

Address 0x026E Access: User read/write[1]

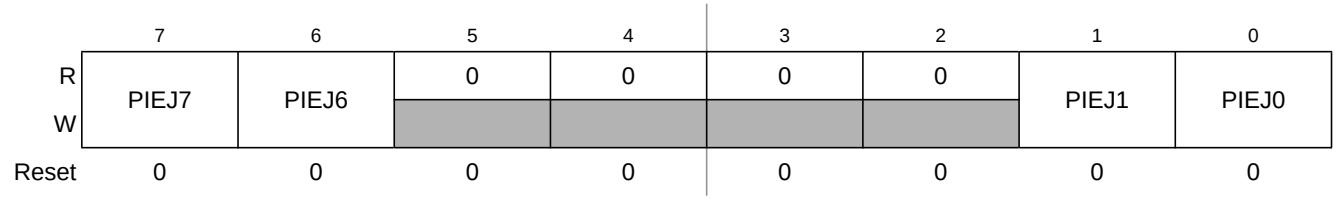

Figure 2-62. Port J Interrupt Enable Register (PIEJ)

[1] Read: Anytime
Write: Anytime

Table 2-61. PIEJ Register Field Descriptions

Field	Description
7-6, 1-0 PIEJ	**Port J interrupt enable**— This bit enables or disables on the edge sensitive pin interrupt on the associated pin. 1 Interrupt enabled 0 Interrupt disabled (interrupt flag masked)

2.3.65 Port J Interrupt Flag Register (PIFJ)

Address 0x026F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-63. Port J Interrupt Flag Register (PIFJ)

1 Read: Anytime
Write: Anytime

Table 2-62. PIFJ Register Field Descriptions

Field	Description
7-6, 1-0 PIFJ	**Port J interrupt flag**— The flag bit is set after an active edge was applied to the associated input pin. This can be a rising or a falling edge based on the state of the polarity select register. Writing a logic “1” to the corresponding bit field clears the flag. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set) 0 No active edge occurred

2.3.66 Port AD0 Data Register 0 (PT0AD0)

Address 0x0270 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PT0AD07	PT0AD06	PT0AD05	PT0AD04	PT0AD03	PT0AD02	PT0AD01	PT0AD00
W								
Altern. Function	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
Reset	0	0	0	0	0	0	0	0

Figure 2-64. Port AD0 Data Register 0 (PT0AD0)

1 Read: Anytime, the data source depends on the data direction value
Write: Anytime

Table 2-63. PT0AD0 Register Field Descriptions

Field	Description
7-0 PT0AD0	**Port AD0 general purpose input/output data**—Data Register, ATD AN analog input When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read.

Chapter 3
Memory Mapping Control (S12XMMCV4)

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
v04.09	01-Feb-08		- Minor changes
v04.10	17-Feb-09		- Minor changes
v04.11	30-Jun-10	3.3.2.7/3-139	- Removed confusing statements in EPAGE description

3.1 Introduction

This section describes the functionality of the module mapping control (MMC) sub-block of the S12X platform. The block diagram of the MMC is shown in Figure 3-1.

The MMC module controls the multi-master priority accesses, the selection of internal resources . Internal buses, including internal memories and peripherals, are controlled in this module. The local address space for each master is translated to a global memory space.

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the XINT module.

4.3.1 Module Memory Map

Table 4-3 gives an overview over all XINT module registers.

Table 4-3. XINT Memory Map

Address	Use	Access
0x0120	RESERVED	—
0x0121	Interrupt Vector Base Register (IVBR)	R/W
0x0122–0x0125	RESERVED	—
0x0126	XGATE Interrupt Priority Configuration Register (INT_XGPRIO)	R/W
0x0127	Interrupt Request Configuration Address Register (INT_CFADDR)	R/W
0x0128	Interrupt Request Configuration Data Register 0 (INT_CFDATA0)	R/W
0x0129	Interrupt Request Configuration Data Register 1 (INT_CFDATA1)	R/W
0x012A	Interrupt Request Configuration Data Register 2 (INT_CFDATA2	R/W
0x012B	Interrupt Request Configuration Data Register 3 (INT_CFDATA3)	R/W
0x012C	Interrupt Request Configuration Data Register 4 (INT_CFDATA4)	R/W
0x012D	Interrupt Request Configuration Data Register 5 (INT_CFDATA5)	R/W
0x012E	Interrupt Request Configuration Data Register 6 (INT_CFDATA6)	R/W
0x012F	Interrupt Request Configuration Data Register 7 (INT_CFDATA7)	R/W

compared to the serial communication rate. This protocol allows a great flexibility for the POD designers, since it does not rely on any accurate time measurement or short response time to any event in the serial communication.

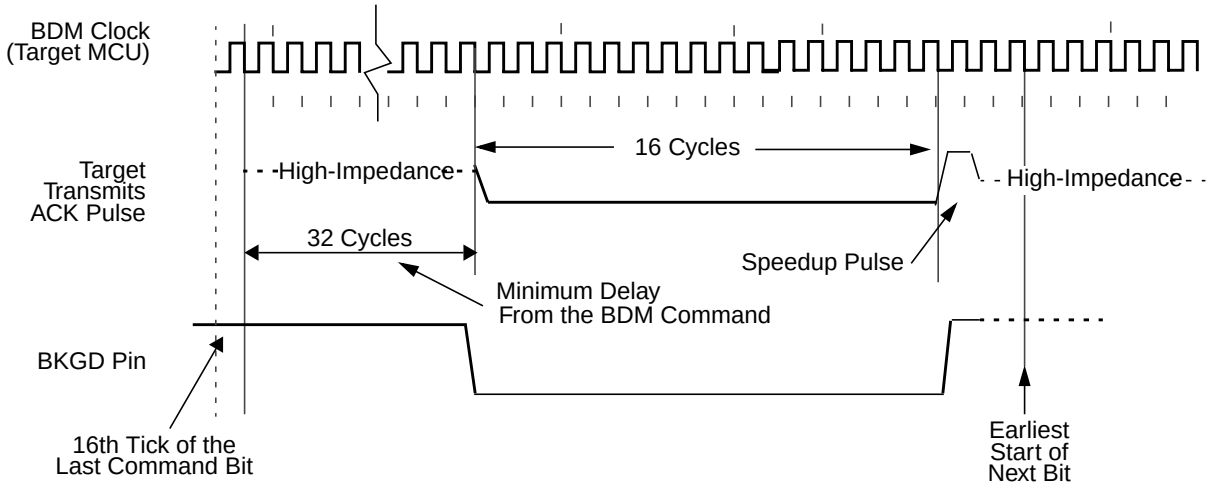

Figure 5-11. Target Acknowledge Pulse (ACK)

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters wait or stop prior to executing a hardware command, the ACK pulse will not be issued meaning that the BDM command was not executed. After entering wait or stop mode, the BDM command is no longer pending.

Figure 5-12 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating that the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

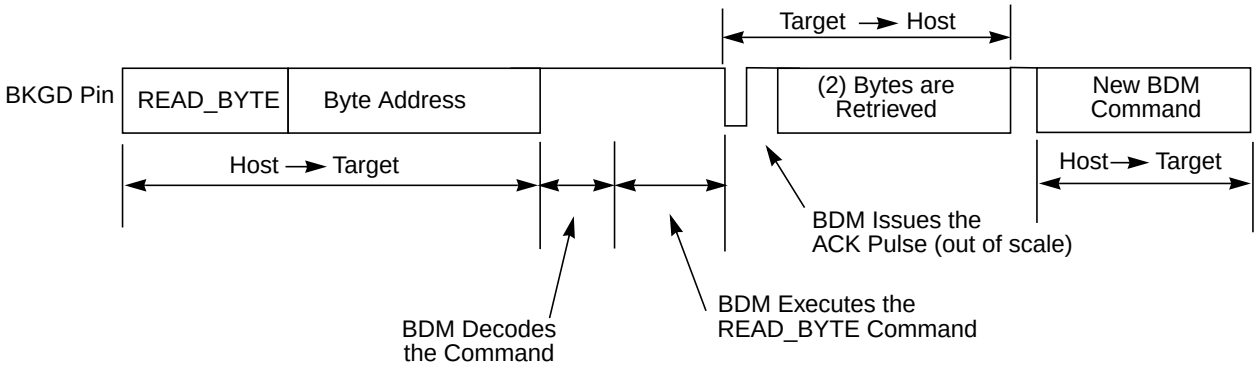

Figure 5-12. Handshake Protocol at Command Level

6.3.2.8.5 Debug Comparator Data High Register (DBGXDH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 6-18. Debug Comparator Data High Register (DBGXDH)

Read: Anytime. See Table 6-26 for visible register encoding.

Write: If DBG not armed. See Table 6-26 for visible register encoding.

Table 6-32. DBGXAH Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Compare Bits** — The Comparator data high compare bits control whether the selected comparator compares the data bus bits [15:8] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparators A and C. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

6.3.2.8.6 Debug Comparator Data Low Register (DBGXDL)

Address: 0x002D

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 6-19. Debug Comparator Data Low Register (DBGXDL)

Read: Anytime. See Table 6-26 for visible register encoding.

Write: If DBG not armed. See Table 6-26 for visible register encoding.

Table 6-33. DBGXDL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Compare Bits** — The Comparator data low compare bits control whether the selected comparator compares the data bus bits [7:0] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparators A and C. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

Table 6-38. NDB and MASK bit dependency

NDB	DBGxDHM[n] / DBGxDLM[n]	Comment
0	0	Do not compare data bus bit.
0	1	Compare data bus bit. Match on equivalence.
1	0	Do not compare data bus bit.
1	1	Compare data bus bit. Match on difference.

6.4.2.4 Range Comparisons

When using the AB comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator A data and data mask registers. Furthermore the DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. Similarly when using the CD comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator C data and data mask registers. Furthermore the DBGCCTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access if tagging is not selected. The corresponding DBGDCTL bits are ignored. The SZE and SZ control bits are ignored in range mode. The comparator A and C TAG bits are used to tag range comparisons for the AB and CD ranges respectively. The comparator B and D TAG bits are ignored in range modes. In order for a range comparison using comparators A and B, both COMPEA and COMPEB must be set; to disable range comparisons both must be cleared. Similarly for a range CD comparison, both COMPEC and COMPED must be set. The comparator A and C BRK bits are used for the AB and CD ranges respectively, the comparator B and D BRK bits are ignored in range mode. When configured for range comparisons and tagging, the ranges are accurate only to word boundaries.

6.4.2.4.1 Inside Range (CompAC_Addr ≤ address ≤ CompBD_Addr)

In the Inside Range comparator mode, either comparator pair A and B or comparator pair C and D can be configured for range comparisons by the control register (DBGC2). The match condition requires that a valid match for both comparators happens on the same bus cycle. A match condition on only one comparator is not valid. An aligned word access which straddles the range boundary will cause a trigger only if the aligned address is inside the range.

6.4.2.4.2 Outside Range (address < CompAC_Addr or address > CompBD_Addr)

In the Outside Range comparator mode, either comparator pair A and B or comparator pair C and D can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. An aligned word access which straddles the range boundary will cause a trigger only if the aligned address is outside the range.

Outside range mode in combination with tagged triggers can be used to detect if the opcode fetches are from an unexpected range. In forced trigger modes the outside range trigger would typically be activated at any interrupt vector fetch or register access. This can be avoided by setting the upper or lower range limit to $7FFFFF or $000000 respectively. Interrupt vector fetches do not cause taghits

```
SUB_1    BRN     *                       ; JMP Destination address TRACE BUFFER ENTRY 1
                                         ; RTI Destination address TRACE BUFFER ENTRY 3
         NOP                             ;
ADDR1    DBNE    A,PART5                 ; Source address TRACE BUFFER ENTRY 4

IRQ_ISR  LDAB    #$F0                    ; IRQ Vector $FFF2 = TRACE BUFFER ENTRY 2
         STAB    VAR_C1
         RTI                             ;
```

The execution flow taking into account the IRQ is as follows

```
         LDX     #SUB_1
MARK1    JMP     0,X                     ;
IRQ_ISR  LDAB    #$F0                    ;
         STAB    VAR_C1
         RTI                             ;
SUB_1    BRN     *
         NOP                             ;
ADDR1    DBNE    A,PART5                 ;
```

6.4.5.2.2 Loop1 Mode

Loop1 Mode, similarly to Normal Mode also stores only COF address information to the trace buffer, it however allows the filtering out of redundant information.

The intent of Loop1 Mode is to prevent the Trace Buffer from being filled entirely with duplicate information from a looping construct such as delays using the DBNE instruction or polling loops using BRSET/BRCLR instructions. Immediately after address information is placed in the Trace Buffer, the S12XDBG module writes this value into a background register. This prevents consecutive duplicate address entries in the Trace Buffer resulting from repeated branches.

Loop1 Mode only inhibits consecutive duplicate source address entries that would typically be stored in most tight looping constructs. It does not inhibit repeated entries of destination addresses or vector addresses, since repeated entries of these would most likely indicate a bug in the user's code that the S12XDBG module is designed to help find.

6.4.5.2.3 Detail Mode

In Detail Mode, address and data for all memory and register accesses is stored in the trace buffer. This mode also features information byte entries to the trace buffer, for each address byte entry. The information byte indicates the size of access (word or byte) and the type of access (read or write).

When tracing CPU12X activity in Detail Mode, all cycles are traced except those when the CPU12X is either in a free or opcode fetch cycle, the address range can be limited to a range specified by the TRANGE bits in DBGTCR. This function uses comparators C and D to define an address range inside which CPU12X activity should be traced (see Table 6-40). Thus the traced CPU12X activity can be restricted to particular register range accesses.

6.4.5.2.4 Pure PC Mode

In Pure PC Mode, tracing from the CPU the PC addresses of all executed opcodes, including illegal opcodes, are stored.

NOTE

The CANTBSEL register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK=1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 11-17. CANTBSEL Register Field Descriptions

Field	Description
2-0 TX[2:0]	**Transmit Buffer Select** — The lowest numbered bit places the respective transmit buffer in the CANTXFG register space (e.g., TX1 = 1 and TX0 = 1 selects transmit buffer TX0; TX1 = 1 and TX0 = 0 selects transmit buffer TX1). Read and write accesses to the selected transmit buffer will be blocked, if the corresponding TXEx bit is cleared and the buffer is scheduled for transmission (see Section 11.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)"). 0 The associated message buffer is deselected 1 The associated message buffer is selected, if lowest numbered bit

The following gives a short programming example of the usage of the CANTBSEL register:

To get the next available transmit buffer, application software must read the CANTFLG register and write this value back into the CANTBSEL register. In this example Tx buffers TX1 and TX2 are available. The value read from CANTFLG is therefore 0b0000_0110. When writing this value back to CANTBSEL, the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to 1 is at bit position 1. Reading back this value out of CANTBSEL results in 0b0000_0010, because only the lowest numbered bit position set to 1 is presented. This mechanism eases the application software's selection of the next available Tx buffer.

- LDAA CANTFLG; value read is 0b0000_0110
- STAA CANTBSEL; value written is 0b0000_0110
- LDAA CANTBSEL; value read is 0b0000_0010

If all transmit message buffers are deselected, no accesses are allowed to the CANTXFG registers.

11.3.2.12 MSCAN Identifier Acceptance Control Register (CANIDAC)

The CANIDAC register is used for identifier acceptance control as described below.

Module Base + 0x000B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-15. MSCAN Identifier Acceptance Control Register (CANIDAC)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except bits IDHITx, which are read-only

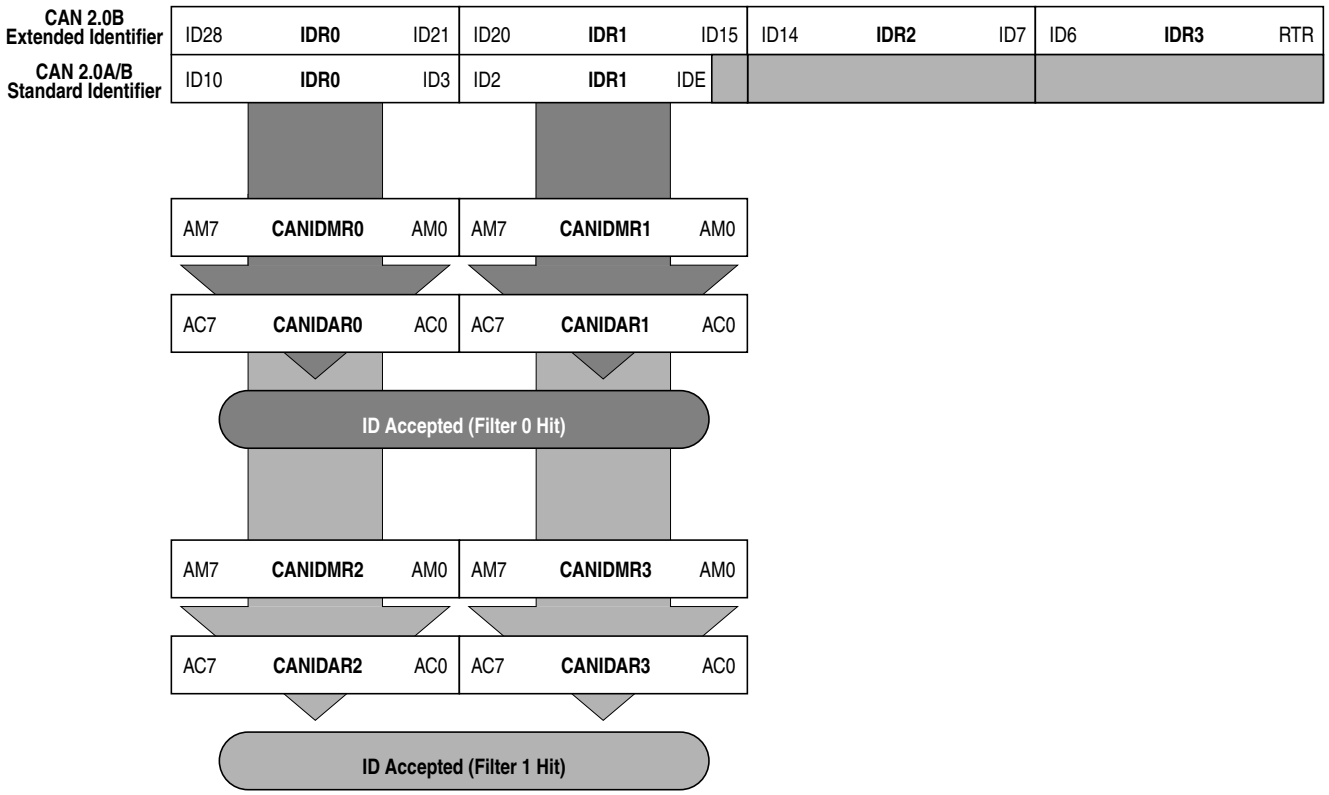

Figure 11-41. 16-bit Maskable Identifier Acceptance Filters

Address & Name		7	6	5	4	3	2	1	0
0x0002 FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
	W								
0x0003 FECCRIX	R	0	0	0	0	0	ECCRIX2	ECCRIX1	ECCRIX0
	W								
0x0004 FCNFG	R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
	W								
0x0005 FERCNFG	R			0				DFDIE	SFDIE
	W								
0x0006 FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
0x0007 FERSTAT	R	0	0	0	0	0	0	DFDIF	SFDIF
	W								
0x0008 FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
0x0009 DFPROT	R	DPOPEN	0	0	DPS4	DPS3	DPS2	DPS1	DPS0
	W								
0x000A FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000B FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000C FRSV0	R	0	0	0	0	0	0	0	0
	W								
0x000D FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000E FECCRHI	R	ECCR15	ECCR14	ECCR13	ECCR12	ECCR11	ECCR10	ECCR9	ECCR8
	W								
0x000F FECCRLO	R	ECCR7	ECCR6	ECCR5	ECCR4	ECCR3	ECCR2	ECCR1	ECCR0
	W								

Figure 19-4. FTMR128K1 Register Summary (continued)

P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.

Table 19-22. DFPROT Field Descriptions

Field	Description
7 DPOPEN	**D-Flash Protection Control** 0 Enables D-Flash memory protection from program and erase with protected address range defined by DPS bits 1 Disables D-Flash memory protection from program and erase
4–0 DPS[4:0]	**D-Flash Protection Size** — The DPS[4:0] bits determine the size of the protected area in the D-Flash memory as shown in Table 19-23.

Table 19-23. D-Flash Protection Address Range

DPS[4:0]	Global Address Range	Protected Size
0_0000	0x10_0000 – 0x10_00FF	256 bytes
0_0001	0x10_0000 – 0x10_01FF	512 bytes
0_0010	0x10_0000 – 0x10_02FF	768 bytes
0_0011	0x10_0000 – 0x10_03FF	1024 bytes
0_0100	0x10_0000 – 0x10_04FF	1280 bytes
0_0101	0x10_0000 – 0x10_05FF	1536 bytes
0_0110	0x10_0000 – 0x10_06FF	1792 bytes
0_0111	0x10_0000 – 0x10_07FF	2048 bytes
0_1000	0x10_0000 – 0x10_08FF	2304 bytes
0_1001	0x10_0000 – 0x10_09FF	2560 bytes
0_1010	0x10_0000 – 0x10_0AFF	2816 bytes
0_1011	0x10_0000 – 0x10_0BFF	3072 bytes
0_1100	0x10_0000 – 0x10_0CFF	3328 bytes
0_1101	0x10_0000 – 0x10_0DFF	3584 bytes
0_1110	0x10_0000 – 0x10_0EFF	3840 bytes
0_1111	0x10_0000 – 0x10_0FFF	4096 bytes
1_0000	0x10_0000 – 0x10_10FF	4352 bytes
1_0001	0x10_0000 – 0x10_11FF	4608 bytes
1_0010	0x10_0000 – 0x10_12FF	4864 bytes
1_0011	0x10_0000 – 0x10_13FF	5120 bytes
1_0100	0x10_0000 – 0x10_14FF	5376 bytes
1_0101	0x10_0000 – 0x10_15FF	5632 bytes

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes, aligned words, or misaligned words. Read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

It is not possible to read from a Flash block while any command is executing on that specific Flash block. It is possible to read from a Flash block while a command is executing on a different Flash block.

Both P-Flash and D-Flash memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by phrase, only one single bit fault in the phrase containing the byte or word accessed will be corrected.

20.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

D-Flash Memory — The D-Flash memory constitutes the nonvolatile memory store for data.

D-Flash Sector — The D-Flash sector is the smallest portion of the D-Flash memory that can be erased. The D-Flash sector consists of four 64 byte rows for a total of 256 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes eight ECC bits for single bit fault correction and double bit fault detection within the phrase.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 1024 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Device ID, Version ID, and the Program Once field. The Program IFR is visible in the global memory map by setting the PGMIFRON bit in the MMCCTL1 register.

20.1.2 Features

20.1.2.1 P-Flash Features

- 64 Kbytes of P-Flash memory composed of one 64 Kbyte Flash block divided into 64 sectors of 1024 bytes
- Single bit fault correction and double bit fault detection within a 64-bit phrase during read operations

Table 20-45. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [22:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 20-46. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-28)
		Set if an invalid global address [22:16] is supplied[1]
		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[2]

1 As defined by the memory map for FTMR128K1.

2 As found in the memory map for FTMR128K1.

20.4.2.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 20-47. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [22:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 20.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 20-63. Erase D-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters
001	Global address [15:0] anywhere within the sector to be erased. See Section 20.1.2.2 for D-Flash sector size.

Upon clearing CCIF to launch the Erase D-Flash Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase D-Flash Sector operation has completed.

Table 20-64. Erase D-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-28)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.3 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 20-65. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

20.4.3.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with

Table A-5. Thermal Package Characteristics (9S12XS256)[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
LQFP 112							
1	D	Thermal resistance LQFP 112, single sided PCB[2]	θ_{JA}	—	—	62	°C/W
2	D	Thermal resistance LQFP 112, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	51	°C/W
3	D	Junction to Board LQFP 112	θ_{JB}	—	—	39	°C/W
4	D	Junction to Case LQFP 112[4]	θ_{JC}	—	—	16	°C/W
5	D	Junction to Package Top LQFP 112[5]	Ψ_{JT}	—	—	3	°C/W
QFP 80							
6	D	Thermal resistance QFP 80, single sided PCB[2]	θ_{JA}	—	—	57	°C/W
7	D	Thermal resistance QFP 80, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	45	°C/W
8	D	Junction to Board QFP 80	θ_{JB}	—	—	29	°C/W
9	D	Junction to Case QFP 80[4]	θ_{JC}	—	—	20	°C/W
10	D	Junction to Package Top QFP 80[5]	Ψ_{JT}	—	—	5	°C/W
LQFP 64							
11	D	Thermal resistance LQFP 64, single sided PCB[2]	θ_{JA}	—	—	68	°C/W
12	D	Thermal resistance LQFP 64, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	50	°C/W
13	D	Junction to Board LQFP 64	θ_{JB}	—	—	32	°C/W
14	D	Junction to Case LQFP 64[4]	θ_{JC}	—	—	15	°C/W
15	D	Junction to Package Top LQFP 64[5]	Ψ_{JT}	—	—	3	°C/W

1 The values for thermal resistance are achieved by package simulations

2 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection.

3 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-7 in a horizontal configuration in natural convection.

4 Junction to case thermal resistance was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. This basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.

5 Thermal characterization parameter Ψ_{JT} is the “resistance” from junction to reference point thermocouple on top center of the case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.