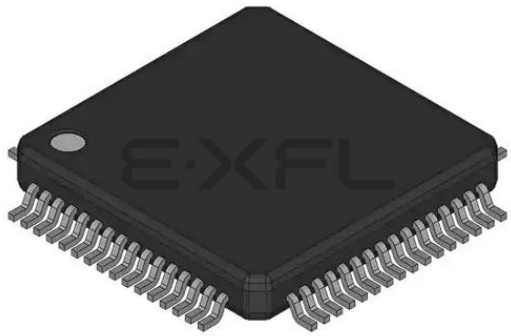

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12xs128j1mae

1.2.3.36 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general-purpose input or output pin. It can be configured as the transmit pin TXD of serial communication interface 0 (SCI0).

1.2.3.37 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general-purpose input or output pin. It can be configured as the receive pin RXD of serial communication interface 0 (SCI0).

1.2.3.38 PT[7:6] / IOC[7:6] / PWM[7:6] — Port T I/O Pins 7-6

PT[7:6] are general-purpose input or output pins. They can be configured as timer (TIM) channel 7-6 or pulse width modulator (PWM) outputs 7-6

1.2.3.39 PT5 / IOC5 / VREG_API — Port T I/O Pin 5

PT[5] is a general-purpose input or output pin. It can be configured as timer (TIM) channel 5, pulse width modulator (PWM) output 5 or as the VREG_API signal output.

1.2.3.40 PT4 / IOC4 / PWM4 — Port T I/O Pin 4

PT4 is a general-purpose input or output pin. It can be configured as timer (TIM) channel 4 or pulse width modulator (PWM) output 4.

1.2.3.41 PT[3:0] / IOC[3:0] — Port T I/O Pin [3:0]

PT[3:0] are a general-purpose input or output pins. They can be configured as timer (TIM) channels 3-0.

1.2.4 Power Supply Pins

S12XS Family power and ground pins are described below.

Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible.

NOTE

All V_{SS} pins must be connected together in the application.

1.2.4.1 VDDX[2:1], VSSX[2:1] — Power and Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All V_{DDX} pins are connected together internally. All V_{SSX} pins are connected together internally.

1.2.4.2 VDDR — Power Pin for Internal Voltage Regulator

Power supply input to the internal voltage regulator.

Table 1-7. Power and Ground Connection Summary

Mnemonic	Nominal Voltage	Description
VDDPLL	1.8 V	Provides operating voltage and ground for the phased-locked loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	0 V	

Read: Anytime

Write: Anytime

These eight index bits are used to page 4KB blocks into the RAM page window located in the local (CPU or BDM) memory map from address 0x1000 to address 0x1FFF (see Figure 3-14). This supports accessing up to 1022KB of RAM (in the Global map) within the 64KB Local map. The RAM page index register is effectively used to construct paged RAM addresses in the Local map format.

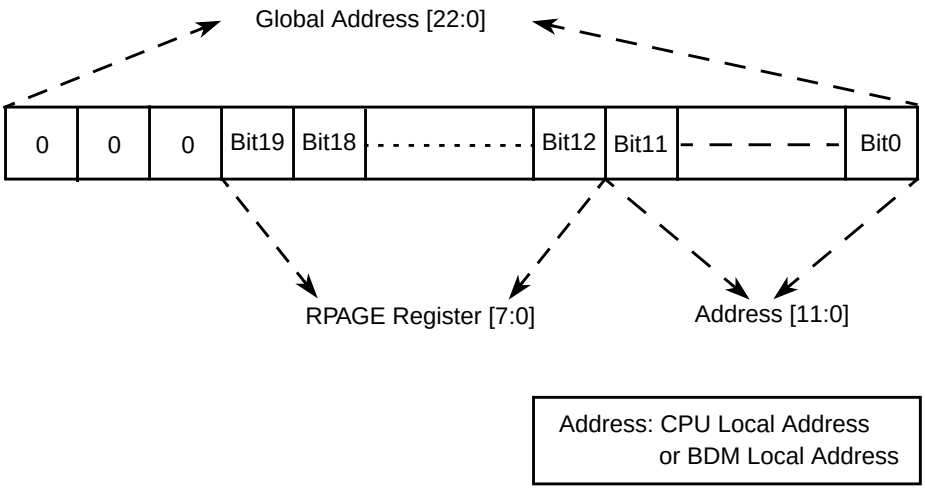

Figure 3-14. RPAGE Address Mapping

NOTE

Because RAM page 0 has the same global address as the register space, it is possible to write to registers through the RAM space when RPAGE = 0x00.

Table 3-8. RPAGE Field Descriptions

Field	Description
7–0 RP[7:0]	**RAM Page Index Bits 7–0** — These page index bits are used to select which of the 256 RAM array pages is to be accessed in the RAM Page Window.

The reset value of 0xFD ensures that there is a linear RAM space available between addresses 0x1000 and 0x3FFF out of reset.

The fixed 4K page from 0x2000–0x2FFF of RAM is equivalent to page 254 (page number 0xFE).

The fixed 4K page from 0x3000–0x3FFF of RAM is equivalent to page 255 (page number 0xFF).

NOTE

The page 0xFD (reset value) contains unimplemented area in the range not occupied by RAM if RAMSIZE is less than 12KB (Refer to Section 3.4.2.3, “Implemented Memory Map).

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the XINT module.

4.3.1 Module Memory Map

Table 4-3 gives an overview over all XINT module registers.

Table 4-3. XINT Memory Map

Address	Use	Access
0x0120	RESERVED	—
0x0121	Interrupt Vector Base Register (IVBR)	R/W
0x0122–0x0125	RESERVED	—
0x0126	XGATE Interrupt Priority Configuration Register (INT_XGPRIO)	R/W
0x0127	Interrupt Request Configuration Address Register (INT_CFADDR)	R/W
0x0128	Interrupt Request Configuration Data Register 0 (INT_CFDATA0)	R/W
0x0129	Interrupt Request Configuration Data Register 1 (INT_CFDATA1)	R/W
0x012A	Interrupt Request Configuration Data Register 2 (INT_CFDATA2	R/W
0x012B	Interrupt Request Configuration Data Register 3 (INT_CFDATA3)	R/W
0x012C	Interrupt Request Configuration Data Register 4 (INT_CFDATA4)	R/W
0x012D	Interrupt Request Configuration Data Register 5 (INT_CFDATA5)	R/W
0x012E	Interrupt Request Configuration Data Register 6 (INT_CFDATA6)	R/W
0x012F	Interrupt Request Configuration Data Register 7 (INT_CFDATA7)	R/W

5.3 Memory Map and Register Definition

5.3.1 Module Memory Map

Table 5-2 shows the BDM memory map when BDM is active.

Table 5-2. BDM Memory Map

Global Address	Module	Size (Bytes)
0x7FFF00–0x7FFF0B	BDM registers	12
0x7FFF0C–0x7FFF0E	BDM firmware ROM	3
0x7FFF0F	Family ID (part of BDM firmware ROM)	1
0x7FFF10–0x7FFFFF	BDM firmware ROM	240

5.3.2 Register Descriptions

A summary of the registers associated with the BDM is shown in Figure 5-2. Registers are accessed by host-driven communications to the BDM hardware using READ_BD and WRITE_BD commands.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x7FFF00	Reserved	R	X	X	X	X	X	X	0	0
		W								
0x7FFF01	BDMSTS	R	ENBDM	BDMACT	0	SDV	TRACE	CLKSW	UNSEC	0
		W								
0x7FFF02	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x7FFF03	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x7FFF04	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x7FFF05	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x7FFF06	BDMCCRL	R	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
		W								

= Unimplemented, Reserved; = Implemented (do not alter)

X = Indeterminate; 0 = Always read zero

Figure 5-2. BDM Register Summary

Chapter 6
S12X Debug (S12XDBGV3) Module

Table 6-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V03.20	14 Sep 2007	6.3.2.7/6-205	- Clarified reserved State Sequencer encodings.
V03.21	23 Oct 2007	6.4.2.2/6-218 6.4.2.4/6-219	- Added single databyte comparison limitation information - Added statement about interrupt vector fetches whilst tagging.
V03.22	12 Nov 2007	6.4.5.2/6-223 6.4.5.5/6-227	- Removed LOOP1 tracing restriction NOTE. - Added pin reset effect NOTE.
V03.23	13 Nov 2007	General	- Text readability improved, typo removed.
V03.24	04 Jan 2008	6.4.5.3/6-225	- Corrected bit name.
V03.25	14 May 2008	General	- Updated Revision History Table format. Corrected other paragraph formats.
V03.26	12 Sep 2012	General	- Added missing full stops. Removed redundant quotation marks.

6.1 Introduction

The S12XDBG module provides an on-chip trace buffer with flexible triggering capability to allow non-intrusive debug of application software. The S12XDBG module is optimized for the S12X 16-bit architecture and allows debugging of CPU12X module operations.

Typically the S12XDBG module is used in conjunction with the S12XBDM module, whereby the user configures the S12XDBG module for a debugging session over the BDM interface. Once configured the S12XDBG module is armed and the device leaves BDM Mode returning control to the user program, which is then monitored by the S12XDBG module. Alternatively the S12XDBG module can be configured over a serial interface using SWI routines.

6.1.1 Glossary

Table 6-2. Glossary Of Terms

Term	Definition
COF	Change Of Flow. Change in the program flow due to a conditional branch, indexed jump or interrupt
BDM	Background Debug Mode
DUG	Device User Guide, describing the features of the device into which the DBG is integrated
WORD	16-bit data entity

Read: Anytime

Write: Anytime

Table 8-5. CRGINT Field Descriptions

Field	Description
7 RTIE	**Real Time Interrupt Enable Bit** 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	**Lock Interrupt Enable Bit** 0 LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 SCMIE	**Self Clock Mode Interrupt Enable Bit** 0 SCM interrupt requests are disabled. 1 Interrupt will be requested whenever SCMIF is set.

8.3.2.6 S12XECRG Clock Select Register (CLKSEL)

This register controls S12XECRG clock selection. Refer toFigure 8-16 for more details on the effect of each bit.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	PLLSEL	PSTP	XCLKS	0	PLLWAI	0	RTIWAI	COPWAI
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-8. S12XECRG Clock Select Register (CLKSEL)

Read: Anytime

Write: Refer to each bit for individual write conditions

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTIER register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 11-14. CANTIER Register Field Descriptions

Field	Description
2-0 TXEIE[2:0]	**Transmitter Empty Interrupt Enable** 0 No interrupt request is generated from this event. 1 A transmitter empty (transmit buffer available for transmission) event causes a transmitter empty interrupt request.

11.3.2.9 MSCAN Transmitter Message Abort Request Register (CANTARQ)

The CANTARQ register allows abort request of queued messages as described below.

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-12. MSCAN Transmitter Message Abort Request Register (CANTARQ)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTARQ register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 11-15. CANTARQ Register Field Descriptions

Field	Description
2-0 ABTRQ[2:0]	**Abort Request** — The CPU sets the ABTRQx bit to request that a scheduled message buffer (TXEx = 0) be aborted. The MSCAN grants the request if the message has not already started transmission, or if the transmission is not successful (lost arbitration or error). When a message is aborted, the associated TXE (see Section 11.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and abort acknowledge flags (ABTAK, see Section 11.3.2.10, "MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)") are set and a transmit interrupt occurs if enabled. The CPU cannot reset ABTRQx. ABTRQx is reset whenever the associated TXE flag is set. 0 No abort request 1 Abort request pending

Module Base + 0x000E — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-18. MSCAN Receive Error Counter (CANRXERR)

1. Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
   Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

11.3.2.16 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-19. MSCAN Transmit Error Counter (CANTXERR)

1. Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
   Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

18.4.1.3 Valid Flash Module Commands

Table 18-28. Flash Commands by Mode

FCMD	Command	Unsecured				Secured			
		NS[1]	NX[2]	SS[3]	ST[4]	NS[5]	NX[6]	SS[7]	ST[8]
0x01	Erase Verify All Blocks	*	*	*	*	*	*	*	*
0x02	Erase Verify Block	*	*	*	*	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	*	*			
0x04	Read Once	*	*	*	*	*			
0x06	Program P-Flash	*	*	*	*	*			
0x07	Program Once	*	*	*	*	*			
0x08	Erase All Blocks			*	*			*	*
0x09	Erase Flash Block	*	*	*	*	*			
0x0A	Erase P-Flash Sector	*	*	*	*	*			
0x0B	Unsecure Flash			*	*			*	*
0x0C	Verify Backdoor Access Key	*				*			
0x0D	Set User Margin Level	*	*	*	*	*			
0x0E	Set Field Margin Level			*	*				
0x10	Erase Verify D-Flash Section	*	*	*	*	*			
0x11	Program D-Flash	*	*	*	*	*			
0x12	Erase D-Flash Sector	*	*	*	*	*			

1 Unsecured Normal Single Chip mode.
2 Unsecured Normal Expanded mode.
3 Unsecured Special Single Chip mode.
4 Unsecured Special Mode.
5 Secured Normal Single Chip mode.
6 Secured Normal Expanded mode.
7 Secured Special Single Chip mode.
8 Secured Special Mode.

18.4.1.4 P-Flash Commands

Table 18-29 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

19.3.2.9.1 P-Flash Protection Restrictions

The general guideline is that P-Flash protection can only be added and not removed. Table 19-21 specifies all valid transitions between P-Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPHS and FPLS bit descriptions for additional restrictions.

Table 19-21. P-Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1 Allowed transitions marked with X, see Figure 19-14 for a definition of the scenarios.

19.3.2.10 D-Flash Protection Register (DFPROT)

The DFPROT register defines which D-Flash sectors are protected against program and erase operations.

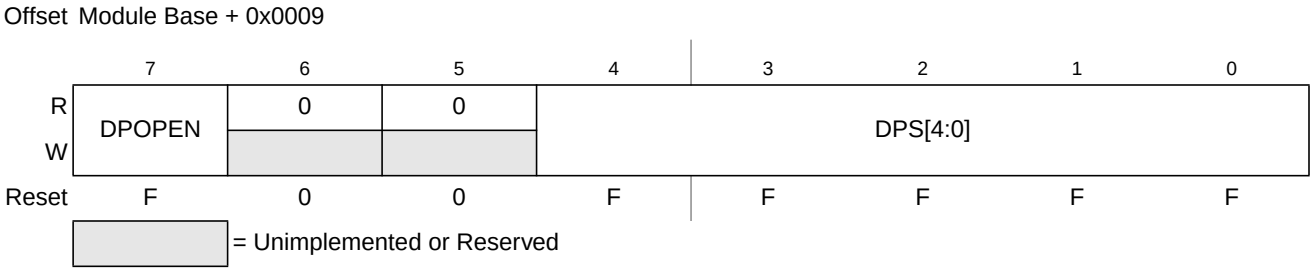

Figure 19-15. D-Flash Protection Register (DFPROT)

The (unreserved) bits of the DFPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOEN bit can only be written from 1 (protection disabled) to 0 (protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, the DFPROT register is loaded with the contents of the D-Flash protection byte in the Flash configuration field at global address 0x7F_FF0D located in P-Flash memory (see Table 19-3) as indicated by reset condition F in Figure 19-15. To change the D-Flash protection that will be loaded during the reset sequence, the P-Flash sector containing the D-Flash protection byte must be unprotected, then the D-Flash protection byte must be programmed. If a double bit fault is detected while reading the

20.4.1.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide OSCCLK down to a target FCLK of 1 MHz. Table 20-7 shows recommended values for the FDIV field based on OSCCLK frequency.

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 1 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

20.4.1.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see Section 20.3.2.7) and the CCIF flag should be tested to determine the status of the current command write sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

CAUTION

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and Memory Controller behavior.

20.4.1.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 20.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 20-26.

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed.

Table 20-32. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[1]

1 As found in the memory map for FTMR128K1.

20.4.2.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or D-Flash block has been erased. The FCCOB upper global address bits determine which block must be verified.

Table 20-33. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Global address [22:16] of the Flash block to be verified.

Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or D-Flash block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.

Table 20-34. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid global address [22:16] is supplied[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2]

1 As defined by the memory map for FTMR128K1.

2 As found in the memory map for FTMR128K1.

20.4.2.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases. The section to be verified cannot cross a 128 Kbyte boundary in the P-Flash memory space.

Table A-8. 5-V I/O Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
16	D	Port H, J, P interrupt input pulse passed ($\overline{STOP}$)	t_{PULSE}	4	—	—	tcyc
17	D	$\overline{IRQ}$ pulse width, edge-sensitive mode ($\overline{STOP}$)	PW_{IRQ}	1	—	—	tcyc
18	D	$\overline{XIRQ}$ pulse width with X-bit set (STOP)	PW_{XIRQ}	4	—	—	tosc

1 Maximum leakage current occurs at maximum operating temperature.
2 Refer to Section A.1.4, “Current Injection” for more details
3 Parameter only applies in stop or pseudo stop mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Typical Run Current Measurement Conditions

Since the current consumption of the output drivers is load dependent, all measurements are without output loads and with minimum I/O activity. The currents are measured in single chip mode, S12XCPU code is executed from Flash. V_{DD35}=5V, internal voltage regulator is enabled and the bus frequency is 40MHz using a 4MHz oscillator in loop controlled Pierce mode.

Since the DBG and BDM modules are typically not used in the end application, the supply current values for these modules is not specified.

An overhead of current consumption exists independent of the listed modules, due to voltage regulation and clock logic that is not dedicated to a specific module. This is listed in the table row named “overhead”.

Table A-9 shows the configuration of the peripherals for typical run current.

Table A-9. Module Configurations for Typical Run Supply (VDDR+VDDA) Current V_{DD35}=5V

Peripheral	Configuration
S12XCPU	420 cycle loop: 384 DBNE cycles plus subroutine entry to stimulate stacking (RAM access)
MSCAN	Configured to loop-back mode using a bit rate of 500kbit/s
SPI	Configured to master mode, continuously transmit data (0x55 or 0xAA) at 2Mbit/s
SCI	Configured into loop mode, continuously transmit data (0x55) at speed of 19200 baud
PWM	Configured to toggle its pins at the rate of 1kHz
TIM	The peripheral shall be configured in output compare mode. Pulse accumulator and modulus counter enabled.
ATD	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
Overhead	VREG supplying 1.8V from a 5V input voltage, PLL on

A.1.10.2 Maximum Run Current Measurement Conditions

Currents are measured in single chip mode, S12XCPU with V_{DD35}=5.5V, internal voltage regulator enabled and a 40MHz bus frequency from a 4MHz input. Characterized parameters are derived using a

A.2 ATD Characteristics

This section describes the characteristics of the analog-to-digital converter.

A.2.1 ATD Operating Characteristics

The Table A-14 and Table A-15 show conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}.$$

This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-14. ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted, supply voltage 3.13 V < V_{DDA} < 5.5 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$	 — —	 $V_{DDA}/2$ V_{DDA}	 V V
2	D	Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	–2.35	0	0.1	V
3	D	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
4	C	Differential reference voltage[1]	V_{RH}-V_{RL}	3.13	5.0	5.5	V
5	C	ATD Clock Frequency (derived from bus clock via the prescaler bus)	f_{ATDCLk}	0.25	—	8.3	MHz
6	P	ATD Clock Frequency in Stop mode (internal generated temperature and voltage dependent clock, ICLK)		0.6	1	1.7	MHz
7	D	ADC conversion in stop, recovery time[2]	$t_{ATDSTPRCV}$	—	—	1.5	µs
8	D	ATD Conversion Period[3] 12 bit resolution: 10 bit resolution: 8 bit resolution:	 N_{CONV12} N_{CONV10} N_{CONV8}	 20 19 17	 — — —	 42 41 39	 ATD clock cycles

1 Full accuracy is not guaranteed when differential voltage is less than 4.50 V
2 When converting in Stop Mode (ICLKSTP=1) an ATD Stop Recovery time tATDSTPRCV is required to switch back to bus clock based ATDCLK when leaving Stop Mode. Do not access ATD registers during this time.
3 The minimum time assumes a sample time of 4 ATD clock cycles. The maximum time assumes a sample time of 24 ATD clock cycles and the discharge feature (SMP_DIS) enabled, which adds 2 ATD clock cycles.

A.2.2 Factors Influencing Accuracy

Source resistance, source capacitance and current injection have an influence on the accuracy of the ATD. A further factor is that PortAD pins that are configured as output drivers switching.

A.2.2.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ATD accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ATD supply pins. Although internal design measures are implemented to minimize the affect of output driver noise, it

A.5 Output Loads

A.5.1 Resistive Loads

The voltage regulator is intended to supply the internal logic and oscillator. It allows no external DC loads.

A.5.2 Capacitive Loads

The capacitive loads are specified in Table A-21. Ceramic capacitors with X7R dielectricum are required.

Table A-21. S12XS family - Capacitive Loads

Num	Characteristic	Symbol	Min	Recommended	Max	Unit
1	VDD/VDDF external capacitive load	C_{DDext}	176	220	264	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	80	220	264	nF

A.5.3 Chip Power-up and Voltage Drops

LVI (low voltage interrupt), POR (power-on reset) and LVRs (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is shown in Figure A-2 .

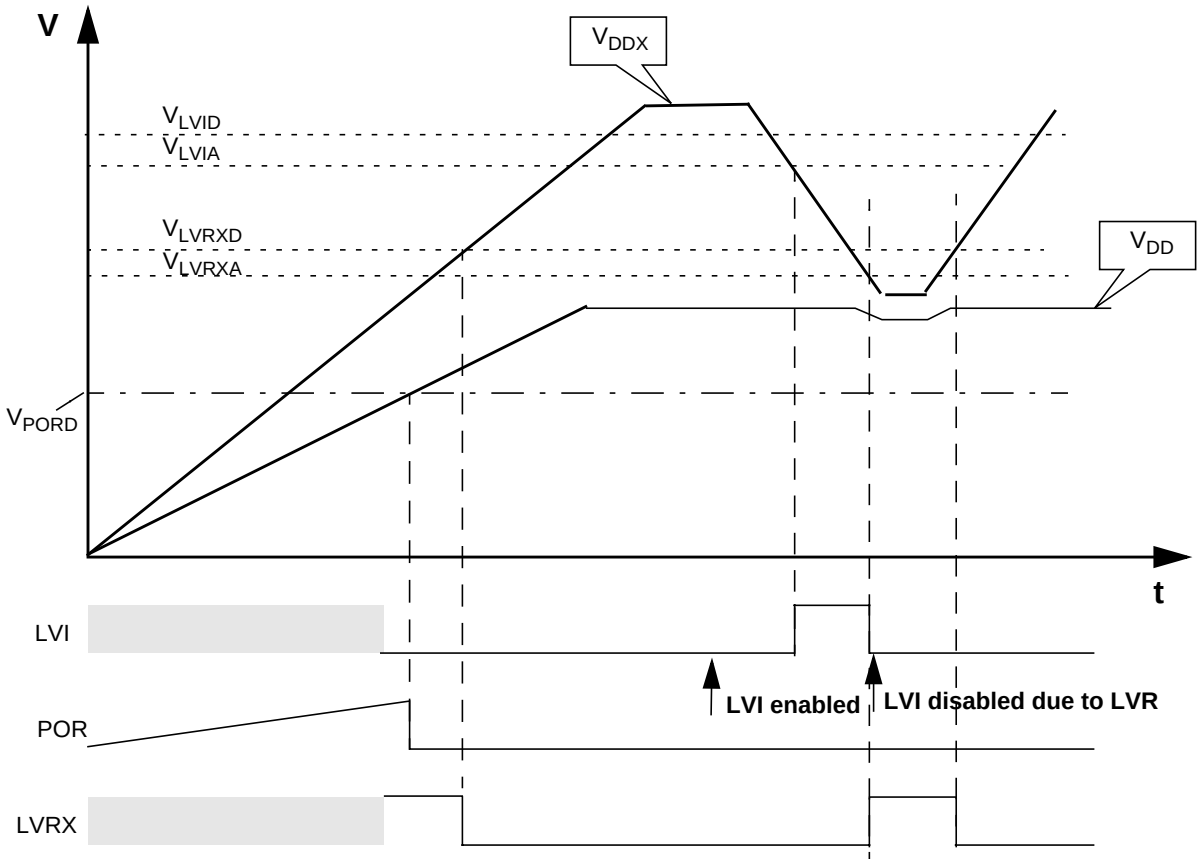

Figure A-2. S12XS family - Chip Power-up and Voltage Drops (not scaled)

A.6.3 Phase Locked Loop

A.6.3.1 Jitter Information

With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure A-4.

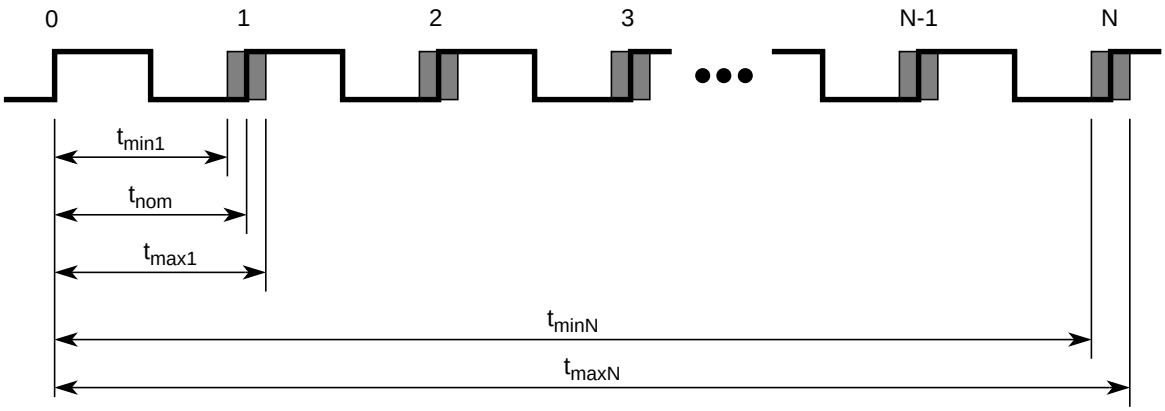

Figure A-4. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

Appendix C
PCB Layout Guidelines

C.1 General

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins .
- Central point of the ground star should be the VSS3 pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSS3.
- VSSPLL must be directly connected to VSS3.
- Keep traces of VSSPLL, EXTAL, and XTAL as short as possible and occupied board area for C7, C8, and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Example layouts are illustrated on the following pages.

Table C-1. Recommended Decoupling Capacitor Choice

Component	Purpose	Type	Value
C1	V_{DDF} filter capacitor	Ceramic X7R	220 nF
C2	N/A	—	—
C3	V_{DDX2} filter capacitor	X7R/tantalum	>=100 nF
C4	V_{DDPLL} filter capacitor	Ceramic X7R	220 nF
C5	OSC load capacitor	From crystal manufacturer	
C6	OSC load capacitor		
C7	V_{DDR} filter capacitor	X7R/tantalum	>=100 nF
C8	N/A	—	—
C9	V_{DD} filter capacitor	Ceramic X7R	220 nF
C10	V_{DDA1} filter capacitor	Ceramic X7R	>=100 nF
C11	V_{DDX1} filter capacitor	X7R/tantalum	>=100 nF
Q1	Quartz	—	—

0x001E–0x001F Port Integration Module (PIM) Map 3 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001E	IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								
0x001F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0020–0x002F Debug Module (S12XDBG) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0020	DBGC1	R	ARM	0	reserved	BDM	DBGBRK	reserved	COMRV	
		W		TRIG						
0x0021	DBGSR	R	TBF	0	0	0	0	SSF2	SSF1	SSF0
		W								
0x0022	DBGTCR	R	reserved	TSOURCE	TRANGE		TRCMOD		TALIGN	
		W								
0x0023	DBGC2	R	0	0	0	0	CDCM		ABCM	
		W								
0x0024	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0025	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0026	DBGCNT	R	0	CNT						
		W								
0x0027	DBGSCRX	R	0	0	0	0	SC3	SC2	SC1	SC0
		W								
0x0027	DBGMFR	R	0	0	0	0	MC3	MC2	MC1	MC0
		W								
0x0028[1]	DBGXCTL (COMPA/C)	R	0	NDB	TAG	BRK	RW	RWE	reserved	COMPE
		W								
0x0028[2]	DBGXCTL (COMPB/D)	R	SZE	SZ	TAG	BRK	RW	RWE	reserved	COMPE
		W								
0x0029	DBGXAH	R	0	Bit 22	21	20	19	18	17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGXDH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGXDL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGXDHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGXDLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

1 This represents the contents if the Comparator A or C control register is blended into this address
2 This represents the contents if the Comparator B or D control register is blended into this address

0x0240–0x027F Port Integration Module (PIM) Map 5 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0260	PTH	R	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		W								
0x0261	PTIH	R	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		W								
0x0262	DDRH	R	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		W								
0x0263	RDRH	R	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		W								
0x0264	PERH	R	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		W								
0x0265	PPSH	R	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		W								
0x0266	PIEH	R	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		W								
0x0267	PIFH	R	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		W								
0x0268	PTJ	R	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
		W								
0x0269	PTIJ	R	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
		W								
0x026A	DDRJ	R	DDRJ7	DDRJ6	0	0	0	0	DDRJ1	DDRJ0
		W								
0x026B	RDRJ	R	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
		W								
0x026C	PERJ	R	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
		W								
0x026D	PPSJ	R	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
		W								
0x026E	PIEJ	R	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
		W								
0x026f	PIFJ	R	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
		W								
0x0270	PT0AD0	R	PT0AD07	PT0AD06	PT0AD05	PT0AD04	PT0AD03	PT0AD02	PT0AD01	PT0AD00
		W								
0x0271	PT1AD0	R	PT1AD07	PT1AD06	PT1AD05	PT1AD04	PT1AD03	PT1AD02	PT1AD01	PT1AD00
		W								
0x0272	DDR0AD0	R	DDR0AD07	DDR0AD06	DDR0AD05	DDR0AD04	DDR0AD03	DDR0AD02	DDR0AD01	DDR0AD00
		W								
0x0273	DDR1AD0	R	DDR1AD07	DDR1AD06	DDR1AD05	DDR1AD04	DDR1AD03	DDR1AD02	DDR1AD01	DDR1AD00
		W								
0x0274	RDR0AD0	R	RDR0AD07	RDR0AD06	RDR0AD05	RDR0AD04	RDR0AD03	RDR0AD02	RDR0AD01	RDR0AD00
		W								
0x0275	RDR1AD0	R	RDR1AD07	RDR1AD06	RDR1AD05	RDR1AD04	RDR1AD03	RDR1AD02	RDR1AD01	RDR1AD00
		W								