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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12xs128j1vaa

Appendix D
Derivative Differences

Appendix E
Detailed Register Address Map

Appendix F
Ordering Information

Chapter 1
Device Overview S12XS Family

1.1 Introduction

The new S12XS family of 16-bit micro controllers is a compatible, reduced version of the S12XE family. These families provide an easy approach to develop common platforms from low-end to high-end applications, minimizing the redesign of software and hardware.

Targeted at generic automotive applications and CAN nodes, some typical examples of these applications are: Body Controllers, Occupant Detection, Door Modules, RKE Receivers, Smart Actuators, Lighting Modules and Smart Junction Boxes amongst many others.

The S12XS family retains many of the features of the S12XE family including Error Correction Code (ECC) on Flash memory, a separate Data-Flash Module for code or data storage, a Frequency Modulated Locked Loop (IPLL) that improves the EMC performance and a fast ATD converter.

S12XS family delivers 32-bit performance with all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Freescale's existing 16-bit S12 and S12X MCU families. Like members of other S12X families, the S12XS family runs 16-bit wide accesses without wait states for all peripherals and memories.

The S12XS family is available in 112-pin LQFP, 80-pin QFP, 64-pin LQFP package options and maintains a high level of pin compatibility with the S12XE family. In addition to the I/O ports available in each module, up to 18 further I/O ports are available with interrupt capability allowing Wake-Up from stop or wait modes.

The peripheral set includes MSCAN, SPI, two SCIs, an 8-channel 24-bit periodic interrupt timer, 8-channel 16-bit Timer, 8-channel PWM and up to 16- channel 12-bit ATD converter.

Software controlled peripheral-to-port routing enables access to a flexible mix of the peripheral modules in the lower pin count package options.

1.1.1 Features

Features of the S12XS Family are listed here. Please see Table D-1 for memory options and Table D-2 for the peripheral features that are available on the different family members.

- 16-bit CPU12X
  - Upward compatible with S12 instruction set with the exception of five Fuzzy instructions (MEM, WAV, WAVR, REV, REVW) which have been removed
  - Enhanced indexed addressing
  - Access to large data segments independent of PPAGE

Table 1-6. Pin-Out Summary[1] (continued)

Package Terminal			Function					Power Supply	Internal Pull Resistor		Description
LQFP 112	QFP 80	LQFP 64	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State	
36	24	20	PE7	$\overline{\text{XCLKS}}$	ECLKX2	—	—	V_{DDX}	PUCR	Up	Port E I/O, system clock output, clock select input
37	25	-	PE6	—	—	—	—	V_{DDX}	While $\overline{\text{RESET}}$ pin is low: down[2]		Port E I/O
38	26	-	PE5	—	—	—	—	V_{DDX}	While $\overline{\text{RESET}}$ pin is low: down[2]		Port E I/O
39	27	21	PE4	ECLK	—	—	—	V_{DDX}	PUCR	Up	Port E I/O, bus clock output
40	28	22	VSSX2	—	—	—	—	—	—	—	—
41	29	23	VDDX2	—	—	—	—	—	—	—	—
42	30	24	$\overline{\text{RESET}}$	—	—	—	—	V_{DDX}	PULLUP		External reset
43	31	25	VDDR	—	—	—	—	—	—	—	—
44	32	26	VSS3	—	—	—	—	—	—	—	—
45	33	27	VSSPLL	—	—	—	—	—	—	—	—
46	34	28	EXTAL	—	—	—	—	V_{DDPLL}	NA	NA	Oscillator pin
47	35	29	XTAL	—	—	—	—	V_{DDPLL}	NA	NA	Oscillator pin
48	36	30	VDDPLL	—	—	—	—	—	—	—	—
49	-	-	PH3	KWH3	—	—	—	V_{DDX}	PERH/PPSH	Disabled	Port H I/O, interrupt
50	-	-	PH2	KWH2	—	—	—	V_{DDX}	PERH/PPSH	Disabled	Port H I/O, interrupt
51	-	-	PH1	KWH1	—	—	—	V_{DDX}	PERH/PPSH	Disabled	Port H I/O, interrupt
52	-	-	PH0	KWH0	—	—	—	V_{DDX}	PERH/PPSH	Disabled	Port H I/O, interrupt
53	37	-	PE3	—	—	—	—	V_{DDX}	PUCR	Up	Port E I/O
54	38	-	PE2	—	—	—	—	V_{DDX}	PUCR	Up	Port E I/O

1.2.3.27 PP2 / KWP2 / PWM2 / TXD1 / IOC2 — Port P I/O Pin 2

PP2 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as pulse width modulator (PWM) channel 2 output, TIM channel 2 or as the transmit pin TXD of serial communication interface 1 (SCI1).

1.2.3.28 PP1 / KWP1 / PWM1 / IOC1 — Port P I/O Pin 1

PP1 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as pulse width modulator (PWM) channel 1 output, TIM channel 1.

1.2.3.29 PP0 / KWP0 / PWM0 / RXD1 / IOC0 — Port P I/O Pin 0

PP0 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as pulse width modulator (PWM) channel 0 output, TIM channel 0 or as the receive pin RXD of serial communication interface 1 (SCI1).

1.2.3.30 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS7 is a general-purpose input or output pin. It can be configured as the slave select pin $\overline{SS}$ of the serial peripheral interface 0 (SPI0).

1.2.3.31 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general-purpose input or output pin. It can be configured as the serial clock pin SCK of the serial peripheral interface 0 (SPI0).

1.2.3.32 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general-purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the serial peripheral interface 0 (SPI0).

1.2.3.33 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general-purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the serial peripheral interface 0 (SPI0).

1.2.3.34 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general-purpose input or output pin. It can be configured as the transmit pin TXD of serial communication interface 1 (SCI1).

1.2.3.35 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general-purpose input or output pin. It can be configured as the receive pin RXD of serial communication interface 1 (SCI1).

Table 2-11. RDRIV Register Field Descriptions (continued)

Field	Description
1 RDPB	**Port B reduced drive**—Select reduced drive for output port This bit configures the drive strength of all associated port output pins as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled
0 RDPA	**Port A reduced drive**—Select reduced drive for output port This bit configures the drive strength of all associated port output pins as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.12 ECLK Control Register (ECLKCTL)

Address 0x001C (PRR) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
Reset:	Mode Depen-dent	1	0	0	0	0	0	0
Special single-chip	0	1	0	0	0	0	0	0
Normal single-chip	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-10. ECLK Control Register (ECLKCTL)

[1] Read: Anytime
Write: Anytime

[1] Read: Anytime
Write: Anytime

Table 2-19. RDRT Register Field Descriptions

Field	Description
7-0 RDRT	**Port T reduced drive**—Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.22 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset	0	0	0	0	0	0	0	0

Figure 2-20. Port T Pull Device Enable Register (PERT)

[1] Read: Anytime
Write: Anytime

Table 2-20. PERT Register Field Descriptions

Field	Description
7-0 PERT	**Port T pull device enable**—Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.3.23 Port T Polarity Select Register (PPST)

Address 0x0245 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset	0	0	0	0	0	0	0	0

Figure 2-21. Port T Polarity Select Register (PPST)

[1] Read: Anytime
Write: Anytime

Table 2-30. PTM Register Field Descriptions (continued)

Field	Description
4 PTM	**Port M general purpose input/output data**—Data Register, routed SPI0 MOSI input/output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The SPI0 function takes precedence over the general purpose I/O function if enabled.
3 PTM	**Port M general purpose input/output data**—Data Register, routed SPI0 $\overline{SS}$ input/output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The SPI0 function takes precedence over the general purpose I/O function if enabled.
2 PTM	**Port M general purpose input/output data**—Data Register, routed SPI0 MISO input/output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The SPI0 function takes precedence over the general purpose I/O function if enabled.
1 PTM	**Port M general purpose input/output data**—Data Register, CAN0 TXCAN output, SCI1 TXD output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The CAN0 function takes precedence over the general purpose I/O function if enabled. • The SCI1 function takes precedence over the general purpose I/O function if enabled.
0 PTM	**Port M general purpose input/output data**—Data Register, CAN0 RXCAN input, SCI1 RXD input When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The CAN0 function takes precedence over the general purpose I/O function if enabled. • The SCI1 function takes precedence over the general purpose I/O function if enabled.

6.3.2.8.5 Debug Comparator Data High Register (DBGXDH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 6-18. Debug Comparator Data High Register (DBGXDH)

Read: Anytime. See Table 6-26 for visible register encoding.

Write: If DBG not armed. See Table 6-26 for visible register encoding.

Table 6-32. DBGXAH Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Compare Bits** — The Comparator data high compare bits control whether the selected comparator compares the data bus bits [15:8] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparators A and C. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

6.3.2.8.6 Debug Comparator Data Low Register (DBGXDL)

Address: 0x002D

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 6-19. Debug Comparator Data Low Register (DBGXDL)

Read: Anytime. See Table 6-26 for visible register encoding.

Write: If DBG not armed. See Table 6-26 for visible register encoding.

Table 6-33. DBGXDL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Compare Bits** — The Comparator data low compare bits control whether the selected comparator compares the data bus bits [7:0] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparators A and C. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

Table 11-11. CANRFLG Register Field Descriptions (continued)

Field	Description
1 OVRIF	**Overrun Interrupt Flag** — This flag is set when a data overrun condition occurs. If not masked, an error interrupt is pending while this flag is set. 0 No data overrun condition 1 A data overrun detected
0 RXF(2)	**Receive Buffer Full Flag** — RXF is set by the MSCAN when a new message is shifted in the receiver FIFO. This flag indicates whether the shifted buffer is loaded with a correctly received message (matching identifier, matching cyclic redundancy code (CRC) and no other errors detected). After the CPU has read that message from the RxFG buffer in the receiver FIFO, the RXF flag must be cleared to release the buffer. A set RXF flag prohibits the shifting of the next FIFO entry into the foreground buffer (RxFG). If not masked, a receive interrupt is pending while this flag is set. 0 No new message available within the RxFG 1 The receiver FIFO is not empty. A new message is available in the RxFG

1. Redundant information for the most critical CAN bus status which is "bus-off". This only occurs if the Tx error counter exceeds a number of 255 errors. Bus-off affects the receiver state. As soon as the transmitter leaves its bus-off state the receiver state skips to RxOK too. Refer also to TSTAT[1:0] coding in this register.
2. To ensure data integrity, do not read the receive buffer registers while the RXF flag is cleared. For MCUs with dual CPUs, reading the receive buffer registers while the RXF flag is cleared may result in a CPU fault condition.

11.3.2.6 MSCAN Receiver Interrupt Enable Register (CANRIER)

This register contains the interrupt enable bits for the interrupt flags described in the CANRFLG register.

Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0

Figure 11-9. MSCAN Receiver Interrupt Enable Register (CANRIER)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANRIER register is held in the reset state when the initialization mode is active (INITRQ=1 and INITAK=1). This register is writable when not in initialization mode (INITRQ=0 and INITAK=0).

The RSTATE[1:0], TSTATE[1:0] bits are not affected by initialization mode.

14.1.4 Block Diagram

Figure 14-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

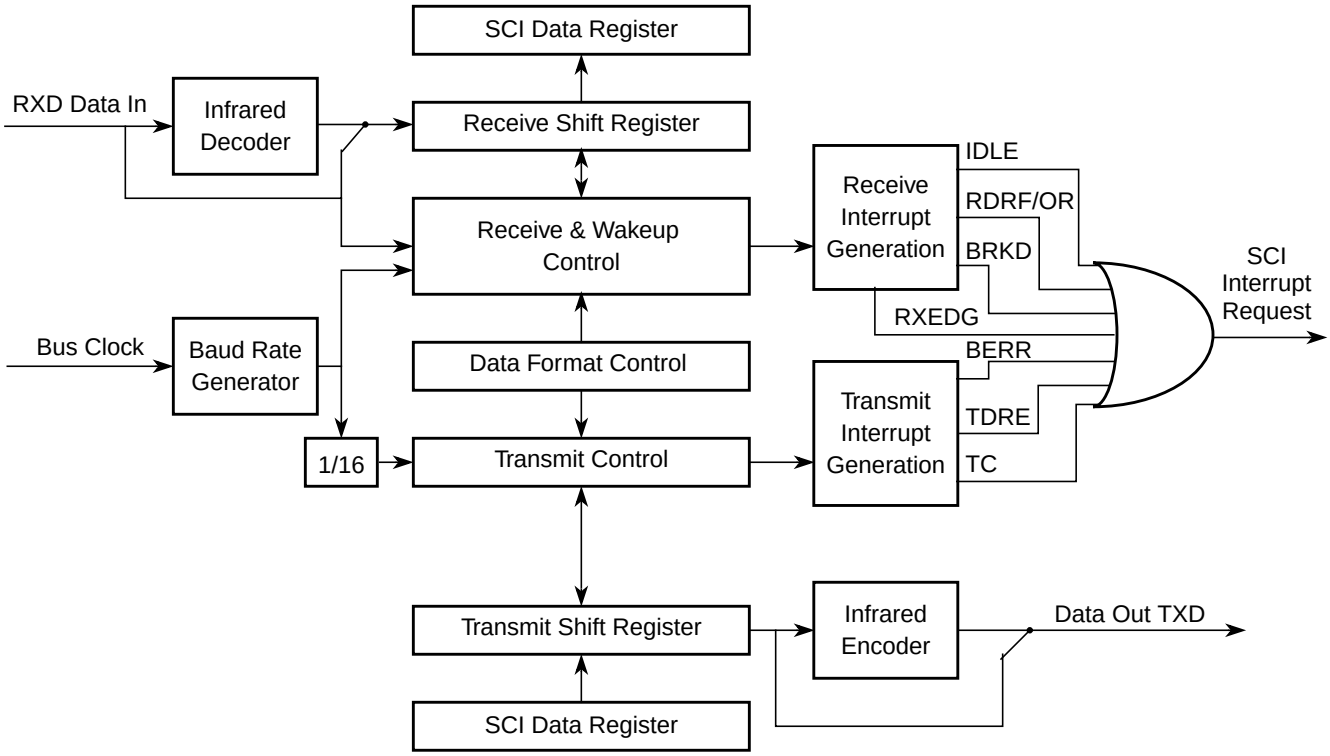

Figure 14-1. SCI Block Diagram

Table 15-7. Example SPI Baud Rate Selection (25 MHz Bus Clock) (Sheet 3 of 3)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
1	1	0	1	1	0	896	27.90 kbit/s
1	1	0	1	1	1	1792	13.95 kbit/s
1	1	1	0	0	0	16	1.5625 Mbit/s
1	1	1	0	0	1	32	781.25 kbit/s
1	1	1	0	1	0	64	390.63 kbit/s
1	1	1	0	1	1	128	195.31 kbit/s
1	1	1	1	0	0	256	97.66 kbit/s
1	1	1	1	0	1	512	48.83 kbit/s
1	1	1	1	1	0	1024	24.41 kbit/s
1	1	1	1	1	1	2048	12.21 kbit/s

15.3.2.4 SPI Status Register (SPISR)

Module Base +0x0003

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-6. SPI Status Register (SPISR)

Read: Anytime

Write: Has no effect

Table 15-8. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after received data has been transferred into the SPI data register. For information about clearing SPIF Flag, please refer to Table 15-9. 0 Transfer not yet complete. 1 New data copied to SPIDR.
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates that the transmit data register is empty. For information about clearing this bit and placing data into the transmit data register, please refer to Table 15-10. 0 SPI data register not empty. 1 SPI data register empty.
4 MODF	**Mode Fault Flag** — This bit is set if the $\overline{SS}$ input becomes low while the SPI is configured as a master and mode fault detection is enabled, MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 15.3.2.2, “SPI Control Register 2 (SPICR2)”. The flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to the SPI control register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

16.2.7 IOC1 — Input Capture and Output Compare Channel 1 Pin

This pin serves as input capture or output compare for channel 1.

16.2.8 IOC0 — Input Capture and Output Compare Channel 0 Pin

This pin serves as input capture or output compare for channel 0.

NOTE

For the description of interrupts see Section 16.6, “Interrupts”.

16.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

16.3.1 Module Memory Map

The memory map for the TIM16B8CV2 module is given below in Figure 16-5. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B8CV2 module and the address offset for each register.

16.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x0002 OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
	W								
0x0003 OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
	W								
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								

= Unimplemented or Reserved

Figure 16-5. TIM16B8CV2 Register Summary (Sheet 1 of 3)

NOTE

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

16.3.2.12 Main Timer Interrupt Flag 1 (TFLG1)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 16-20. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write: Used in the clearing mechanism (set bits cause corresponding bits to be cleared). Writing a zero will not affect current status of the bit.

Table 16-16. TRLG1 Field Descriptions

Field	Description
7:0 C[7:0]F	**Input Capture/Output Compare Channel “x” Flag** — These flags are set when an input capture or output compare event occurs. Clearing requires writing a one to the corresponding flag bit while TEN or PAEN is set to one. When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel (0x0010–0x001F) will cause the corresponding channel flag CxF to be cleared.

16.3.2.13 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 16-21. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 or PAEN bit of PACTL is set to one.

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x7F_FF0E located in P-Flash memory (see Table 18-3) as indicated by reset condition F in Figure 18-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 18-27. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

18.3.2.16 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-23. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

18.3.2.17 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-24. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

18.3.2.18 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Table 19-40. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 19-28)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [22:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

19.4.2.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash block 0. The Program Once reserved field can be read using the Read Once command as described in Section 19.4.2.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash block 0 cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 19-41. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 20-61. Program D-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. The CCIF flag is set when the operation has completed.

Table 20-62. Program D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 20-28)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the D-Flash block
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.2.16 Erase D-Flash Sector Command

The Erase D-Flash Sector operation will erase all addresses in a sector of the D-Flash block.

Table 20-63. Erase D-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x12	Global address [22:16] to identify D-Flash block

Table 20-63. Erase D-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters
001	Global address [15:0] anywhere within the sector to be erased. See Section 20.1.2.2 for D-Flash sector size.

Upon clearing CCIF to launch the Erase D-Flash Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase D-Flash Sector operation has completed.

Table 20-64. Erase D-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-28)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.3 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 20-65. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

20.4.3.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with

Table A-1. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, regulator and analog supply voltage	V_{DD35}	–0.3	6.0	V
2	Digital logic supply voltage[2]	V_{DD}	–0.3	2.16	V
3	PLL supply voltage[2]	V_{DDPLL}	–0.3	2.16	V
4	NVM supply voltage[2]	V_{DDF}	–0.3	3.6	V
5	Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	–6.0	0.3	V
6	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.3	0.3	V
7	Digital I/O input voltage	V_{IN}	–0.3	6.0	V
8	Analog reference	V_{RH}, V_{RL}	–0.3	6.0	V
9	EXTAL, XTAL	V_{ILV}	–0.3	2.16	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins[3]	I_D	–25	+25	mA
12	Instantaneous maximum current Single pin limit for EXTAL, XTAL[4]	I_{DL}	–25	+25	mA
14	Maximum current Single pin limit for power supply pins	I_{DV}	–100	+100	mA
15	Storage temperature range	T_{stg}	–65	155	°C

1 Beyond absolute maximum ratings device might be damaged.
2 The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3 All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, or V_{SSA} and V_{DDA}.
4 Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Detailed MSCAN Foreground Receive and Transmit Buffer Layout (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xXX1F	CANxTTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								

0x0180–0x023F Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180-0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0240–0x027F Port Integration Module (PIM) Map 5 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0241	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0242	DDRT	R	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0243	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0247	PTTRR	R	PTTRR7	PTTRR6	PTTRR5	PTTRR4	0	PTTRR2	PTTRR1	PTTRR0
		W								