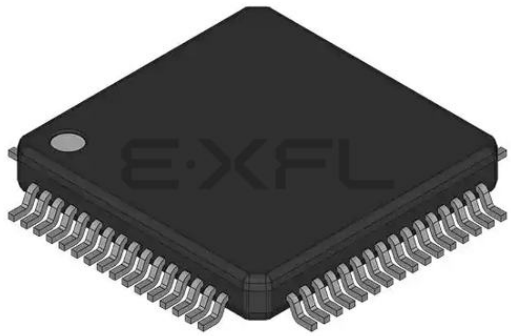

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12xs128j1vae

Table 1-6 provides a pin out summary listing the availability and functionality of individual pins for each package option.

Table 1-6. Pin-Out Summary[1]

Package Terminal			Function					Power Supply	Internal Pull Resistor		Description
LQFP 112	QFP 80	LQFP 64	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State	
1	1	1	PP3	KWP3	PWM3	—	—	V_{DDX}	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
2	2	2	PP2	KWP2	PWM2	IOC2	TXD1	V_{DDX}	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM/TIM channel, TXD of SCI1
3	3	3	PP1	KWP1	PWM1	IOC1	—	V_{DDX}	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM/TIM channel
4	4	4	PP0	KWP0	PWM0	IOC0	RXD1	V_{DDX}	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM/TIM channel, RXD of SCI1
5	-	-	PK3	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
6	-	-	PK2	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
7	-	-	PK1	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
8	-	-	PK0	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
9	5	5	PT0	IOC0	—	—	—	V_{DDX}	PERT/PPST	Disabled	Port T I/O, TIM channel
10	6	6	PT1	IOC1	—	—	—	V_{DDX}	PERT/PPST	Disabled	Port T I/O, TIM channel
11	7	7	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled	Port T I/O, TIM channel
12	8	8	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled	Port T I/O, TIM channel
13	9	9	VDDF	—	—	—	—	—	—	—	—
14	10	10	VSS1	—	—	—	—	—	—	—	—
15	11	11	PT4	IOC4	PWM4	—	—	V_{DDX}	PERT/PPST	Disabled	Port T I/O, PWM/TIM channel

Table 2-16. PTT Register Field Descriptions (continued)

Field	Description
5 PTT	**Port T general purpose input/output data**—Data Register, TIM output, routed PWM output, VREG_API output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The TIM output function takes precedence over the routed PWM, VREG_API function and the general purpose I/O function if the related channel is enabled. • The routed PWM function takes precedence over VREG_API and the general purpose I/O function if the related channel is enabled. • The VREG_API takes precedence over the general purpose I/O function if enabled.
3-0 PTT	**Port T general purpose input/output data**—Data Register, TIM output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The TIM output function takes precedence over the general purpose I/O function if the related channel is enabled.

2.3.19 Port T Input Register (PTIT)

Address 0x0241 Access: User read[1]

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	u	u	u	u	u	u	u	u

= Unimplemented or Reserved u = Unaffected by reset

Figure 2-17. Port T Input Register (PTIT)

[1] Read: Anytime
Write:Never, writes to this register have no effect

Table 2-17. PTIT Register Field Descriptions

Field	Description
7-0 PTIT	**Port T input data**— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.40 Port M Wired-Or Mode Register (WOMM)

Address 0x0256 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Reset	0	0	0	0	0	0	0	0

Figure 2-38. Port M Wired-Or Mode Register (WOMM)

1 Read: Anytime
Write: Anytime

Table 2-36. WOMM Register Field Descriptions

Field	Description
7-0 WOMM	**Port M wired-or mode**—Enable open-drain functionality on output pin This bit configures an output pin as wired-or (open-drain) or push-pull independent of the function used on the pins. In wired-or mode a logic “0” is driven active low while a logic “1” remains undriven. This allows a multipoint connection of several serial modules. The bit has no influence on pins used as input. 1 Output buffer operates as open-drain output. 0 Output buffer operates as push-pull output.

2.3.41 Module Routing Register (MODRR)

Address 0x0257 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	MODRR7	MODRR6	0	MODRR4	0	0	0	0
W								
Routing Option	SCI1	SCI1	—	SPI0	—	—	—	—
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-39. Module Routing Register (MODRR)

1 Read: Anytime
Write: Anytime

This register configures the re-routing of SCI1 and SPI0 on alternative ports.

Table 2-37. SCI1 Routing

MODRRx		Related Pins	
7	6	TXD	RXD

2.3.44 Port P Data Direction Register (DDRP)

Address 0x025A

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset	0	0	0	0	0	0	0	0

Figure 2-42. Port P Data Direction Register (DDRP)

1 Read: Anytime
Write: Anytime

Table 2-41. DDRP Register Field Descriptions

Field	Description
7 DDRP	**Port P data direction**— This bit determines whether the associated pin is an input or output. The PWM forces the I/O state to be an output for an enabled channel. If the PWM shutdown feature is enabled this pin is forced to be an input. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input
6-3 DDRP	**Port P data direction**— This bit determines whether the associated pin is an input or output. The PWM forces the I/O state to be an output for an enabled channel. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input
2,0 DDRP	**Port P data direction**— This bit determines whether the associated pin is an input or output. The PWM forces the I/O state to be an output for an enabled channel. Else the TIM forces the I/O state to be an output for a timer port associated with an enabled output compare. Else depending on the configuration of the enabled SCI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input
1 DDRP	**Port P data direction**— This bit determines whether the associated pin is an input or output. The PWM forces the I/O state to be an output for an enabled channel. Else the TIM forces the I/O state to be an output for a timer port associated with an enabled output compare. In this case the data direction bit will not change. 1 Associated pin configured as output 0 Associated pin configured as input

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x7FFF07	BDMCCRH	R	0	0	0	0	0	CCR10	CCR9	CCR8
		W								
0x7FFF08	BDMGPR	R	BGAE	BGP6	BGP5	BGP4	BGP3	BGP2	BGP1	BGP0
		W								
0x7FFF09	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented, Reserved

= Implemented (do not alter)

X = Indeterminate

0 = Always read zero

Figure 5-2. BDM Register Summary (continued)

5.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x7FFF01

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	CLKSW	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0[1]	1	0	0	0	0	0[3]	0
Emulation Modes (if modes available)	1	0	0	0	0	1[2]	0	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

= Implemented (do not alter)

0 = Always read zero

1 ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (non-volatile memory). This is because the ENBDM bit is set by the standard firmware before a BDM command can be fully transmitted and executed.

2 CLKSW is read as 1 by a debugging environment in emulation modes when the device is not secured and read as 0 when secured if emulation modes available.

3 UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Figure 5-3. BDM Status Register (BDMSTS)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0024	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0025	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0026	DBGCNT	R	0	CNT						
		W								
0x0027	DBGSCRX	R	0	0	0	0	SC3	SC2	SC1	SC0
		W								
0x0027	DBGMFR	R	0	0	0	0	MC3	MC2	MC1	MC0
		W								
0x0028[1]	DBGXCTL (COMPA/C)	R	0	NDB	TAG	BRK	RW	RWE	reserved	COMPE
		W								
0x0028[2]	DBGXCTL (COMPB/D)	R	SZE	SZ	TAG	BRK	RW	RWE	reserved	COMPE
		W								
0x0029	DBGXAH	R	0	Bit 22	21	20	19	18	17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGXDH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGXDL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGXDHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGXDLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

1 This represents the contents if the Comparator A or C control register is blended into this address.

2 This represents the contents if the Comparator B or D control register is blended into this address

Figure 6-2. Quick Reference to S12XDBG Registers

6.3.2 Register Descriptions

This section consists of the S12XDBG control and trace buffer register descriptions in address order. Each comparator has a bank of registers that are visible through an 8-byte window between 0x0028 and 0x002F in the S12XDBG module register address map. When ARM is set in DBGC1, the only bits in the S12XDBG module registers that can be written are ARM, TRIG, and COMRV[1:0].

```
SUB_1    BRN     *                       ; JMP Destination address TRACE BUFFER ENTRY 1
                                         ; RTI Destination address TRACE BUFFER ENTRY 3
         NOP                             ;
ADDR1    DBNE    A,PART5                 ; Source address TRACE BUFFER ENTRY 4

IRQ_ISR  LDAB    #$F0                    ; IRQ Vector $FFF2 = TRACE BUFFER ENTRY 2
         STAB    VAR_C1
         RTI                             ;
```

The execution flow taking into account the IRQ is as follows

```
         LDX     #SUB_1
MARK1    JMP     0,X                     ;
IRQ_ISR  LDAB    #$F0                    ;
         STAB    VAR_C1
         RTI                             ;
SUB_1    BRN     *
         NOP                             ;
ADDR1    DBNE    A,PART5                 ;
```

6.4.5.2.2 Loop1 Mode

Loop1 Mode, similarly to Normal Mode also stores only COF address information to the trace buffer, it however allows the filtering out of redundant information.

The intent of Loop1 Mode is to prevent the Trace Buffer from being filled entirely with duplicate information from a looping construct such as delays using the DBNE instruction or polling loops using BRSET/BRCLR instructions. Immediately after address information is placed in the Trace Buffer, the S12XDBG module writes this value into a background register. This prevents consecutive duplicate address entries in the Trace Buffer resulting from repeated branches.

Loop1 Mode only inhibits consecutive duplicate source address entries that would typically be stored in most tight looping constructs. It does not inhibit repeated entries of destination addresses or vector addresses, since repeated entries of these would most likely indicate a bug in the user's code that the S12XDBG module is designed to help find.

6.4.5.2.3 Detail Mode

In Detail Mode, address and data for all memory and register accesses is stored in the trace buffer. This mode also features information byte entries to the trace buffer, for each address byte entry. The information byte indicates the size of access (word or byte) and the type of access (read or write).

When tracing CPU12X activity in Detail Mode, all cycles are traced except those when the CPU12X is either in a free or opcode fetch cycle, the address range can be limited to a range specified by the TRANGE bits in DBGTCR. This function uses comparators C and D to define an address range inside which CPU12X activity should be traced (see Table 6-40). Thus the traced CPU12X activity can be restricted to particular register range accesses.

6.4.5.2.4 Pure PC Mode

In Pure PC Mode, tracing from the CPU the PC addresses of all executed opcodes, including illegal opcodes, are stored.

SEC[1:0] = ‘10’. All other combinations put the device in a secured mode. The recommended value to put the device in secured state is the inverse of the unsecured state, i.e. SEC[1:0] = ‘01’.

Table 7-4. Security Bits

SEC[1:0]	Security State
00	1 (secured)
01	1 (secured)
10	***0 (unsecured)***
11	1 (secured)

NOTE

Please refer to the Flash block guide for actual security configuration (in section “Flash Module Security”).

7.1.4 Operation of the Secured Microcontroller

By securing the device, unauthorized access to the EEPROM and Flash memory contents can be prevented. However, it must be understood that the security of the EEPROM and Flash memory contents also depends on the design of the application program. For example, if the application has the capability of downloading code through a serial port and then executing that code (e.g. an application containing bootloader code), then this capability could potentially be used to read the EEPROM and Flash memory contents even when the microcontroller is in the secure state. In this example, the security of the application could be enhanced by requiring a challenge/response authentication before any code can be downloaded.

Secured operation has the following effects on the microcontroller:

7.1.4.1 Normal Single Chip Mode (NS)

- Background debug module (BDM) operation is completely disabled.
- Execution of Flash and EEPROM commands is restricted. Please refer to the NVM block guide for details.
- Tracing code execution using the DBG module is disabled.

7.1.4.2 Special Single Chip Mode (SS)

- BDM firmware commands are disabled.
- BDM hardware commands are restricted to the register space.
- Execution of Flash and EEPROM commands is restricted. Please refer to the NVM block guide for details.
- Tracing code execution using the DBG module is disabled.

Special single chip mode means BDM is active after reset. The availability of BDM firmware commands depends on the security state of the device. The BDM secure firmware first performs a blank check of both the Flash memory and the EEPROM. If the blank check succeeds, security will be temporarily turned off and the state of the security bits in the appropriate Flash memory location can be changed If the blank check fails, security will remain active, only the BDM hardware commands will be enabled, and the accessible memory space is restricted to the peripheral register area. This will allow the BDM to be used to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to “unsecured” state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

8.3.2.2 S12XECRG Reference Divider Register (REFDV)

The REFDV register provides a finer granularity for the IPLL multiplier steps.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	REFFRQ[1:0]		REFDIV[5:0]					
Reset	0	0	0	0	0	0	0	0

Figure 8-4. S12XECRG Reference Divider Register (REFDV)

Read: Anytime

Write: Anytime except when PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit.

$$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

The REFFRQ[1:0] bit are used to configure the internal PLL filter for optimal stability and lock time. For correct IPLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Figure 8-3. Setting the REFFRQ[1:0] bits wrong can result in a non functional IPLL (no locking and/or insufficient stability).

Table 8-3. Reference Clock Frequency Selection

REFCLK Frequency Ranges	REFFRQ[1:0]
1MHz <= f_{REF} <= 2MHz	00
2MHz < f_{REF} <= 6MHz	01
6MHz < f_{REF} <= 12MHz	10
f_{REF} >12MHz	11

8.3.2.3 S12XECRG Post Divider Register (POSTDIV)

The POSTDIV register controls the frequency ratio between the VCOCLK and PLLCLK. The count in the final divider divides VCOCLK frequency by 1 or 2*POSTDIV. Note that if POSTDIV = $00 f_{PLL}= f_{VCO} (divide by one).

10.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

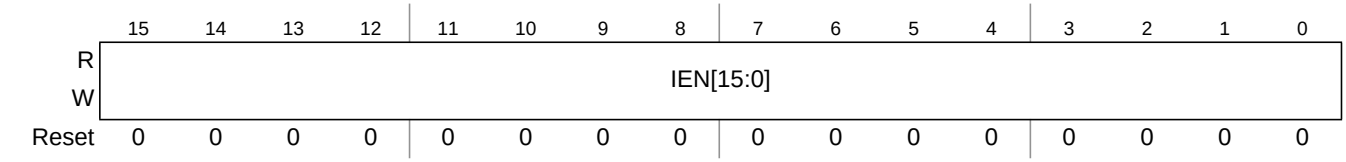

Figure 10-13. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 10-20. ATDDIEN Field Descriptions

Field	Description
15–0 IEN[15:0]	**ATD Digital Input Enable on channel *x* (*x*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register. 0 Disable digital input buffer to AN*x* pin 1 Enable digital input buffer on AN*x* pin. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

10.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

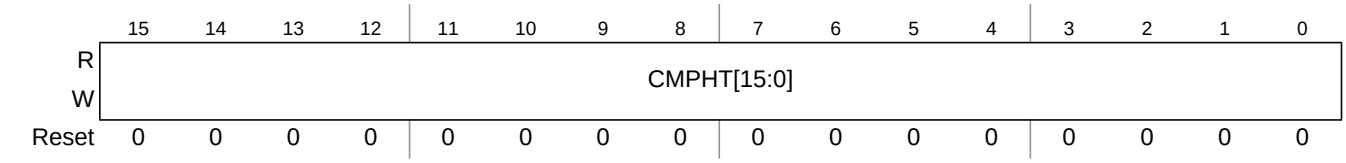

Figure 10-14. ATD Compare Higher Than Register (ATDCMPHT)

Table 10-21. ATDCMPHT Field Descriptions

Field	Description
15–0 CMPHT[15:0]	**Compare Operation Higher Than Enable for conversion number *n* (*n*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence** — This bit selects the operator for comparison of conversion results. 0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2

12.3.0.2 PIT Force Load Timer Register (PITFLT)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W					PFLT3	PFLT2	PFLT1	PFLT0
Reset	0	0	0	0	0	0	0	0

Figure 12-4. PIT Force Load Timer Register (PITFLT)

Read: Anytime

Write: Anytime

Table 12-3. PITFLT Field Descriptions

Field	Description
3:0 PFLT[3:0]	**PIT Force Load Bits for Timer 3-0** — These bits have only an effect if the corresponding timer channel (PCE set) is enabled and if the PIT module is enabled (PITE set). Writing a one into a PFLT bit loads the corresponding 16-bit timer load register into the 16-bit timer down-counter. Writing a zero has no effect. Reading these bits will always return zero.

12.3.0.3 PIT Channel Enable Register (PITCE)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	PCE3	PCE2	PCE1	PCE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-5. PIT Channel Enable Register (PITCE)

Read: Anytime

Write: Anytime

Table 12-4. PITCE Field Descriptions

Field	Description
3:0 PCE[3:0]	**PIT Enable Bits for Timer Channel 3:0** — These bits enable the PIT channels 3-0. If PCE is cleared, the PIT channel is disabled and the corresponding flag bit in the PITTF register is cleared. When PCE is set, and if the PIT module is enabled (PITE = 1) the 16-bit timer counter is loaded with the start count value and starts down-counting. 0 The corresponding PIT channel is disabled. 1 The corresponding PIT channel is enabled.

14.3.2.3 SCI Alternative Status Register 1 (SCIASR1)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-6. SCI Alternative Status Register 1 (SCIASR1)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 14-6. SCIASR1 Field Descriptions

Field	Description
7 RXEDGIF	**Receive Input Active Edge Interrupt Flag** — RXEDGIF is asserted, if an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD input occurs. RXEDGIF bit is cleared by writing a “1” to it. 0 No active receive on the receive input has occurred 1 An active edge on the receive input has occurred
2 BERRV	**Bit Error Value** — BERRV reflects the state of the RXD input when the bit error detect circuitry is enabled and a mismatch to the expected value happened. The value is only meaningful, if BERRIF = 1. 0 A low input was sampled, when a high was expected 1 A high input reassembled, when a low was expected
1 BERRIF	**Bit Error Interrupt Flag** — BERRIF is asserted, when the bit error detect circuitry is enabled and if the value sampled at the RXD input does not match the transmitted value. If the BERRIE interrupt enable bit is set an interrupt will be generated. The BERRIF bit is cleared by writing a “1” to it. 0 No mismatch detected 1 A mismatch has occurred
0 BKDIF	**Break Detect Interrupt Flag** — BKDIF is asserted, if the break detect circuitry is enabled and a break signal is received. If the BKDIE interrupt enable bit is set an interrupt will be generated. The BKDIF bit is cleared by writing a “1” to it. 0 No break signal was received 1 A break signal was received

Table 14-11. SCISR1 Field Descriptions (continued)

Field	Description
3 OR	**Overrun Flag** — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL). 0 No overrun 1 Overrun **Note:** OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs: 1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear); 2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set); 3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register); 4. Read status register SCISR1 (returns RDRF clear and OR set). Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received.
2 NF	**Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL). 0 No noise 1 Noise
1 FE	**Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	**Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

17.4 Functional Description

17.4.1 General

Module VREG_3V3 is a voltage regulator, as depicted in Figure 17-1. The regulator functional elements are the regulator core (REG), a low-voltage detect module (LVD), a control block (CTRL), a power-on reset module (POR), and a low-voltage reset module (LVR)and a high temperature sensor (HTD).

17.4.2 Regulator Core (REG)

Respectively its regulator core has three parallel, independent regulation loops (REG1,REG2 and REG3). REG1 and REG3 differ only in the amount of current that can be delivered.

The regulators are linear regulator with a bandgap reference when operated in Full Performance Mode. They act as a voltage clamp in Reduced Power Mode. All load currents flow from input VDDR to VSS or VSSPLL. The reference circuits are supplied by VDDA and VSSA.

17.4.2.1 Full Performance Mode

In Full Performance Mode, the output voltage is compared with a reference voltage by an operational amplifier. The amplified input voltage difference drives the gate of an output transistor.

17.4.2.2 Reduced Power Mode

In Reduced Power Mode, the gate of the output transistor is connected directly to a reference voltage to reduce power consumption. Mode switching from reduced power to full performance requires a transition time of t_{vup}, if the voltage regulator is enabled.

17.4.3 Low-Voltage Detect (LVD)

Subblock LVD is responsible for generating the low-voltage interrupt (LVI). LVD monitors the input voltage (V_{DDA}–V_{SSA}) and continuously updates the status flag LVDS. Interrupt flag LVIF is set whenever status flag LVDS changes its value. The LVD is available in FPM and is inactive in Reduced Power Mode or Shutdown Mode.

17.4.4 Power-On Reset (POR)

This functional block monitors VDD. If V_{DD} is below V_{PORD}, POR is asserted; if V_{DD} exceeds V_{PORD}, the POR is deasserted. POR asserted forces the MCU into Reset. POR Deasserted will trigger the power-on sequence.

17.4.5 Low-Voltage Reset (LVR)

Block LVR monitors the supplies VDD, VDDX and VDDF. If one (or more) drops below it's corresponding assertion level, signal LVR asserts; if all VDD,VDDX and VDDF supplies are above their

Table 18-4. Program IFR Fields

Global Address (PGMIFRON)	Size (Bytes)	Field Description
0x40_0000 – 0x40_0007	8	Device ID
0x40_0008 – 0x40_00E7	224	Reserved
0x40_00E8 – 0x40_00E9	2	Version ID
0x40_00EA – 0x40_00FF	22	Reserved
0x40_0100 – 0x40_013F	64	Program Once Field Refer to Section 18.4.2.6, “Program Once Command”
0x40_0140 – 0x40_01FF	192	Reserved

Table 18-5. D-Flash and Memory Controller Resource Fields

Global Address	Size (Bytes)	Description
0x10_0000 – 0x10_1FFF	8,192	D-Flash Memory
0x10_2000 – 0x11_FFFF	122,880	Reserved
0x12_0000 – 0x12_007F	128	D-Flash Nonvolatile Information Register (DFIFRON[1] = 1)
0x12_0080 – 0x12_0FFF	3,968	Reserved
0x12_1000 – 0x12_1FFF	4,096	Reserved
0x12_2000 – 0x12_3CFF	7,242	Reserved
0x12_3D00 – 0x12_3FFF	768	Memory Controller Scratch RAM (MGRAMON[1] = 1)
0x12_4000 – 0x12_E7FF	43,008	Reserved
0x12_E800 – 0x12_FFFF	6,144	Reserved
0x13_0000 – 0x13_FFFF	65,536	Reserved

1 MMCCTL1 register bit

19.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

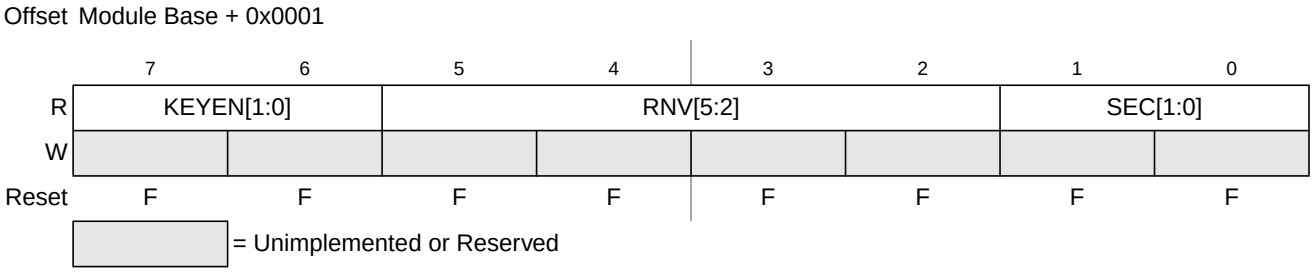

Figure 19-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x7F_FF0F located in P-Flash memory (see Table 19-3) as indicated by reset condition F in Figure 19-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 19-8. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 19-9.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 19-10. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 19-9. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED[1]
10	ENABLED
11	DISABLED

1 Preferred KEYEN state to disable backdoor key access.

Table 19-10. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED[1]
10	UNSECURED
11	SECURED

P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.

Table 19-22. DFPROT Field Descriptions

Field	Description
7 DPOPEN	**D-Flash Protection Control** 0 Enables D-Flash memory protection from program and erase with protected address range defined by DPS bits 1 Disables D-Flash memory protection from program and erase
4–0 DPS[4:0]	**D-Flash Protection Size** — The DPS[4:0] bits determine the size of the protected area in the D-Flash memory as shown in Table 19-23.

Table 19-23. D-Flash Protection Address Range

DPS[4:0]	Global Address Range	Protected Size
0_0000	0x10_0000 – 0x10_00FF	256 bytes
0_0001	0x10_0000 – 0x10_01FF	512 bytes
0_0010	0x10_0000 – 0x10_02FF	768 bytes
0_0011	0x10_0000 – 0x10_03FF	1024 bytes
0_0100	0x10_0000 – 0x10_04FF	1280 bytes
0_0101	0x10_0000 – 0x10_05FF	1536 bytes
0_0110	0x10_0000 – 0x10_06FF	1792 bytes
0_0111	0x10_0000 – 0x10_07FF	2048 bytes
0_1000	0x10_0000 – 0x10_08FF	2304 bytes
0_1001	0x10_0000 – 0x10_09FF	2560 bytes
0_1010	0x10_0000 – 0x10_0AFF	2816 bytes
0_1011	0x10_0000 – 0x10_0BFF	3072 bytes
0_1100	0x10_0000 – 0x10_0CFF	3328 bytes
0_1101	0x10_0000 – 0x10_0DFF	3584 bytes
0_1110	0x10_0000 – 0x10_0EFF	3840 bytes
0_1111	0x10_0000 – 0x10_0FFF	4096 bytes
1_0000	0x10_0000 – 0x10_10FF	4352 bytes
1_0001	0x10_0000 – 0x10_11FF	4608 bytes
1_0010	0x10_0000 – 0x10_12FF	4864 bytes
1_0011	0x10_0000 – 0x10_13FF	5120 bytes
1_0100	0x10_0000 – 0x10_14FF	5376 bytes
1_0101	0x10_0000 – 0x10_15FF	5632 bytes

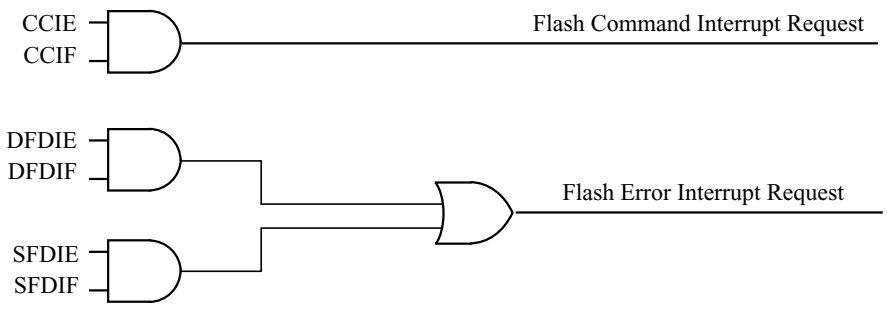

Figure 19-27. Flash Module Interrupts Implementation

19.4.4 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 19.4.3, “Interrupts”).

19.4.5 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the CPU is allowed to enter stop mode.

19.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 19-10). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x7F_FF0F.

The security state out of reset can be permanently changed by programming the security byte of the Flash configuration field. This assumes that you are starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

19.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x7F_FF00–0x7F_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 19.3.2.2), the Verify Backdoor Access Key command (see Section 19.4.2.11) allows the user to present four prospective keys for comparison to the

Appendix E
Detailed Register Address Map

E.1 Detailed Register Map

The following tables show the detailed register map of the S12XS family.

0x0000–0x0009 Port Integration Module (PIM) Map 1 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA 0
		W								
0x0001	PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		W								
0x0002	DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
0x0003	DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		W								
0x0004	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0005	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0006	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0007	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0008	PORTE	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
		W								
0x0009	DDRE	R	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	0	0
		W								

0x000A–0x000B Module Mapping Control (S12XMMC) Map 1 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x000A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x000B	MODE	R	MODC	0	0	0	0	0	0	0
		W								

0x000C–0x000D Port Integration Module (PIM) Map 2 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x000C	PUCR	R	PUPKE	BKPUE	0	PUPEE	0	0	PUPBE	PUPAE
		W								
0x000D	RDRIV	R	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		W								