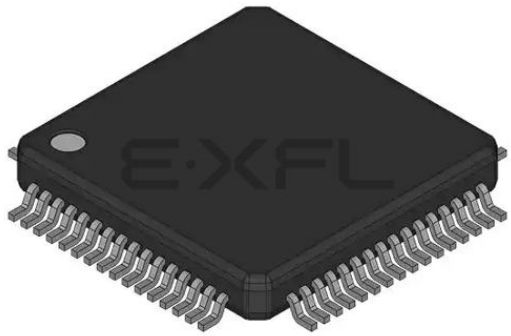

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Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12xs256j0caer

Table 1-6. Pin-Out Summary[1] (continued)

Package Terminal			Function					Power Supply	Internal Pull Resistor		Description
LQFP 112	QFP 80	LQFP 64	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State	
72	-	-	PAD10	AN10	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
73	54	42	PAD03	AN03	—	—	—	V_{DDA}	PER1AD	Disabled	Port AD I/O, analog input of ATD
74	-	-	PAD11	AN11	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
75	55	43	PAD04	AN04	—	—	—	V_{DDA}	PER1AD	Disabled	Port AD I/O, analog input of ATD
76	-	-	PAD12	AN12	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
77	56	44	PAD05	AN05	—	—	—	V_{DDA}	PER1AD	Disabled	Port AD I/O, analog input of ATD
78	-	-	PAD13	AN13	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
79	57	45	PAD06	AN06	—	—	—	V_{DDA}	PER1AD	Disabled	Port AD I/O, analog input of ATD
80	-	-	PAD14	AN14	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
81	58	46	PAD07	AN07	—	—	—	V_{DDA}	PER1AD	Disabled	Port AD I/O, analog input of ATD
82	-	-	PAD15	AN15	—	—	—	V_{DDA}	PER0AD	Disabled	Port AD I/O, analog input of ATD
83	59	47	VDDA	—	—	—	—	—	—	—	—
84	60	48	VRH	—	—	—	—	—	—	—	—
85	61	49	VRL[3]	—	—	—	—	—	—	—	—
86	62	49	VSSA	—	—	—	—	—	—	—	—

Table 2-11. RDRIV Register Field Descriptions (continued)

Field	Description
1 RDPB	**Port B reduced drive**—Select reduced drive for output port This bit configures the drive strength of all associated port output pins as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled
0 RDPA	**Port A reduced drive**—Select reduced drive for output port This bit configures the drive strength of all associated port output pins as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.12 ECLK Control Register (ECLKCTL)

Address 0x001C (PRR) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
Reset:	Mode Depen-dent	1	0	0	0	0	0	0
Special single-chip	0	1	0	0	0	0	0	0
Normal single-chip	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-10. ECLK Control Register (ECLKCTL)

[1] Read: Anytime
Write: Anytime

3.4.2.1.1 Expansion of the Local Address Map

Expansion of the CPU Local Address Map

The program page index register in MMC allows accessing up to 4MB of FLASH or ROM in the global memory map by using the eight page index bits to page 256 16KB blocks into the program page window located from address 0x8000 to address 0xBFFF in the local CPU memory map.

The page value for the program page window is stored in the PPAGE register. The value of the PPAGE register can be read or written by normal memory accesses as well as by the CALL and RTC instructions (see Section 3.5.1, “CALL and RTC Instructions).

Control registers, vector space and parts of the on-chip memories are located in unpaged portions of the 64KB local CPU address space.

The starting address of an interrupt service routine must be located in unpaged memory unless the user is certain that the PPAGE register will be set to the appropriate value when the service routine is called. However an interrupt service routine can call other routines that are in paged memory. The upper 16KB block of the local CPU memory space (0xC000–0xFFFF) is unpaged. It is recommended that all reset and interrupt vectors point to locations in this area or to the other unpaged sections of the local CPU memory map.

The RAM page index register allows accessing up to 1MB minus 2KB of RAM in the global memory map by using the eight RPAGE index bits to page 4KB blocks into the RAM page window located in the local CPU memory space from address 0x1000 to address 0x1FFF. The Data FLASH page index register EPAGE allows accessing up to 256KB of Data Flash in the system by using the eight EPAGE index bits to page 1KB blocks into the Data FLASH page window located in the local CPU memory space from address 0x0800 to address 0x0BFF.

- System Reset generation from the following possible sources:
  - Power on reset
  - Low voltage reset
  - Illegal address reset
  - COP reset
  - Loss of clock reset
  - External pin reset
- Real-Time Interrupt (RTI)

8.1.2 Modes of Operation

This subsection lists and briefly describes all operating modes supported by the S12XECRG.

- Run Mode

  All functional parts of the S12XECRG are running during normal Run Mode. If RTI or COP functionality is required the individual bits of the associated rate select registers (COPCTL, RTICTL) have to be set to a non zero value.
- Wait Mode

  In this mode the IPLL can be disabled automatically depending on the PLLWAI bit.
- Stop Mode

  Depending on the setting of the PSTP bit Stop Mode can be differentiated between Full Stop Mode (PSTP = 0) and Pseudo Stop Mode (PSTP = 1).
  - Full Stop Mode

    The oscillator is disabled and thus all system and core clocks are stopped. The COP and the RTI remain frozen.
  - Pseudo Stop Mode

    The oscillator continues to run and most of the system and core clocks are stopped. If the respective enable bits are set the COP and RTI will continue to run, else they remain frozen.
- Self Clock Mode

  Self Clock Mode will be entered if the Clock Monitor Enable Bit (CME) and the Self Clock Mode Enable Bit (SCME) are both asserted and the clock monitor in the oscillator block detects a loss of clock. As soon as Self Clock Mode is entered the S12XECRG starts to perform a clock quality check. Self Clock Mode remains active until the clock quality check indicates that the required quality of the incoming clock signal is met (frequency and amplitude). Self Clock Mode should be used for safety purposes only. It provides reduced functionality to the MCU in case a loss of clock is causing severe system conditions.

8.1.3 Block Diagram

Figure 8-1 shows a block diagram of the S12XECRG.

10.2 Signal Description

This section lists all inputs to the ADC12B16C block.

10.2.1 Detailed Signal Descriptions

10.2.1.1 AN*x* (*x* = 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

10.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connection of these inputs!

10.2.1.3 V_{RH}, V_{RL}

V_{RH} is the high reference voltage, V_{RL} is the low reference voltage for ATD conversion.

10.2.1.4 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ADC12B16C block.

10.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B16C.

10.3.1 Module Memory Map

Figure 10-3 gives an overview on all ADC12B16C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

10.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

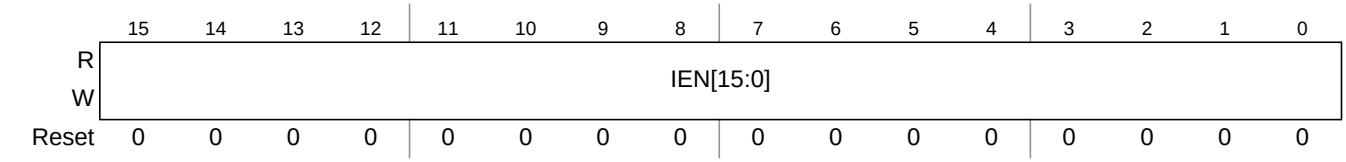

Figure 10-13. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 10-20. ATDDIEN Field Descriptions

Field	Description
15–0 IEN[15:0]	**ATD Digital Input Enable on channel *x* (*x*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register. 0 Disable digital input buffer to AN*x* pin 1 Enable digital input buffer on AN*x* pin. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

10.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

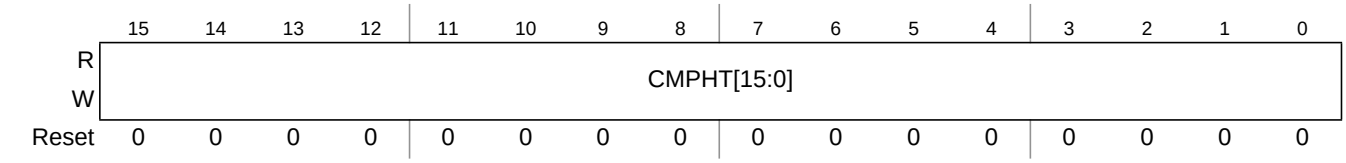

Figure 10-14. ATD Compare Higher Than Register (ATDCMPHT)

Table 10-21. ATDCMPHT Field Descriptions

Field	Description
15–0 CMPHT[15:0]	**Compare Operation Higher Than Enable for conversion number *n* (*n*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence** — This bit selects the operator for comparison of conversion results. 0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2

Table 10-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	0	Bit[11:4] = result, Bit[3:0]=0000
8-bit data	1	Bit[7:0] = result, Bit[11:8]=0000
10-bit data	0	Bit[11:2] = result, Bit[1:0]=00
10-bit data	1	Bit[9:0] = result, Bit[11:10]=00
12-bit data	X	Bit[11:0] = result

10.4 Functional Description

The ADC12B16C is structured into an analog sub-block and a digital sub-block.

10.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies V_{DDA} and V_{SSA} allow to isolate noise of other MCU circuitry from the analog sub-block.

10.4.1.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external world and stores them as capacitor charge on a storage node.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must fall within the potential range of V_{SSA} to V_{DDA}.

During the hold process the analog input is disconnected from the storage node.

10.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

10.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine is automatically powered down.

12.3.0.4 PIT Multiplex Register (PITMUX)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	0	0	0	PMUX3	PMUX2	PMUX1	PMUX0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-6. PIT Multiplex Register (PITMUX)

Read: Anytime

Write: Anytime

Table 12-5. PITMUX Field Descriptions

Field	Description
3:0 PMUX[3:0]	**PIT Multiplex Bits for Timer Channel 3:0** — These bits select if the corresponding 16-bit timer is connected to micro time base 1 or 0. If PMUX is modified, the corresponding 16-bit timer is switched to the other micro time base immediately. 0 The corresponding 16-bit timer counts with micro time base 0. 1 The corresponding 16-bit timer counts with micro time base 1.

12.3.0.5 PIT Interrupt Enable Register (PITINTE)

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	0	0	0	0	PINTE3	PINTE2	PINTE1	PINTE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-7. PIT Interrupt Enable Register (PITINTE)

Read: Anytime

Write: Anytime

Table 12-6. PITINTE Field Descriptions

Field	Description
3:0 PINTE[3:0]	**PIT Time-out Interrupt Enable Bits for Timer Channel 3:0** — These bits enable an interrupt service request whenever the time-out flag PTF of the corresponding PIT channel is set. When an interrupt is pending (PTF set) enabling the interrupt will immediately cause an interrupt. To avoid this, the corresponding PTF flag has to be cleared first. 0 Interrupt of the corresponding PIT channel is disabled. 1 Interrupt of the corresponding PIT channel is enabled.

is set, an interrupt service is requested whenever the corresponding time-out flag PTF in the PIT time-out flag (PITTF) register is set. The flag can be cleared by writing a one to the flag bit.

NOTE

Be careful when resetting the PITE, PINTE or PITCE bits in case of pending PIT interrupt requests, to avoid spurious interrupt requests.

12.4.3 Hardware Trigger

The PIT module contains four hardware trigger signal lines PITTRIG[3:0], one for each timer channel. These signals can be connected on SoC level to peripheral modules enabling e.g. periodic ATD conversion (please refer to the SoC Guide for the mapping of PITTRIG[3:0] signals to peripheral modules).

Whenever a timer channel time-out is reached, the corresponding PTF flag is set and the corresponding trigger signal PITTRIG triggers a rising edge. The trigger feature requires a minimum time-out period of two bus clock cycles because the trigger is asserted high for at least one bus clock cycle. For load register values PITLD = 0x0001 and PITMTLD = 0x0002 the flag setting, trigger timing and a restart with force load is shown in Figure 12-20.

12.5 Initialization

12.5.1 Startup

Set the configuration registers before the PITE bit in the PITCFLMT register is set. Before PITE is set, the configuration registers can be written in arbitrary order.

12.5.2 Shutdown

When the PITCE register bits, the PITINTE register bits or the PITE bit in the PITCFLMT register are cleared, the corresponding PIT interrupt flags are cleared. In case of a pending PIT interrupt request, a spurious interrupt can be generated. Two strategies, which avoid spurious interrupts, are recommended:

1. Reset the PIT interrupt flags only in an ISR. When entering the ISR, the I mask bit in the CCR is set automatically. The I mask bit must not be cleared before the PIT interrupt flags are cleared.
2. After setting the I mask bit with the SEI instruction, the PIT interrupt flags can be cleared. Then clear the I mask bit with the CLI instruction to re-enable interrupts.

12.5.3 Flag Clearing

A flag is cleared by writing a one to the flag bit. Always use store or move instructions to write a one in certain bit positions. Do not use the BSET instructions. Do not use any C-constructs that compile to BSET instructions. “BSET flag_register, #mask” must not be used for flag clearing because BSET is a read-modify-write instruction which writes back the “bit-wise or” of the flag_register and the mask into the flag_register. BSET would clear all flag bits that were set, independent from the mask.

For example, to clear flag bit 0 use: MOVB #$01,PITTF.

13.2.1 PWM7 — PWM Channel 7

This pin serves as waveform output of PWM channel 7 and as an input for the emergency shutdown feature.

13.2.2 PWM6 — PWM Channel 6

This pin serves as waveform output of PWM channel 6.

13.2.3 PWM5 — PWM Channel 5

This pin serves as waveform output of PWM channel 5.

13.2.4 PWM4 — PWM Channel 4

This pin serves as waveform output of PWM channel 4.

13.2.5 PWM3 — PWM Channel 3

This pin serves as waveform output of PWM channel 3.

13.2.6 PWM3 — PWM Channel 2

This pin serves as waveform output of PWM channel 2.

13.2.7 PWM3 — PWM Channel 1

This pin serves as waveform output of PWM channel 1.

13.2.8 PWM3 — PWM Channel 0

This pin serves as waveform output of PWM channel 0.

13.3 Memory Map and Register Definition

This section describes in detail all the registers and register bits in the PWM module.

The special-purpose registers and register bit functions that are not normally available to device end users, such as factory test control registers and reserved registers, are clearly identified by means of shading the appropriate portions of address maps and register diagrams. Notes explaining the reasons for restricting access to the registers and functions are also explained in the individual register descriptions.

13.3.1 Module Memory Map

This section describes the content of the registers in the PWM module. The base address of the PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated

13.6 Interrupts

The PWM module has only one interrupt which is generated at the time of emergency shutdown, if the corresponding enable bit (PWMIE) is set. This bit is the enable for the interrupt. The interrupt flag PWMIF is set whenever the input level of the PWM7 channel changes while PWM7ENA = 1 or when PWMENA is being asserted while the level at PWM7 is active.

In stop mode or wait mode (with the PSWAI bit set), the emergency shutdown feature will drive the PWM outputs to their shutdown output levels but the PWMIF flag will not be set.

A description of the registers involved and affected due to this interrupt is explained in Section 13.3.2.15, “PWM Shutdown Register (PWMSDN)”.

The PWM block only generates the interrupt and does not service it. The interrupt signal name is PWM interrupt signal.

14.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
  - Receive wakeup on active edge
  - Transmit collision detect supporting LIN
  - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

14.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run mode
- Wait mode
- Stop mode

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. If at any time software clears the TE bit in SCI control register 2 (SCICR2), the transmitter enable signal goes low and the transmit signal goes idle.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCIDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCIDRH/L.

14.4.5.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCICR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCICR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when there are 10 or 11(M = 0 or M = 1) consecutive zero received. Depending if the break detect feature is enabled or not receiving a break character has these effects on SCI registers.

If the break detect feature is disabled (BKDFE = 0):

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers (SCIDRH/L)
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see 3.4.4 and 3.4.5 SCI Status Register 1 and 2)

If the break detect feature is enabled (BKDFE = 1) there are two scenarios[1]

The break is detected right from a start bit or is detected during a byte reception.

- Sets the break detect interrupt flag, BKDIF
- Does not change the data register full flag, RDRF or overrun flag OR
- Does not change the framing error flag FE, parity error flag PE.
- Does not clear the SCI data registers (SCIDRH/L)
- May set noise flag NF, or receiver active flag RAF.

1. A Break character in this context are either 10 or 11 consecutive zero received bits

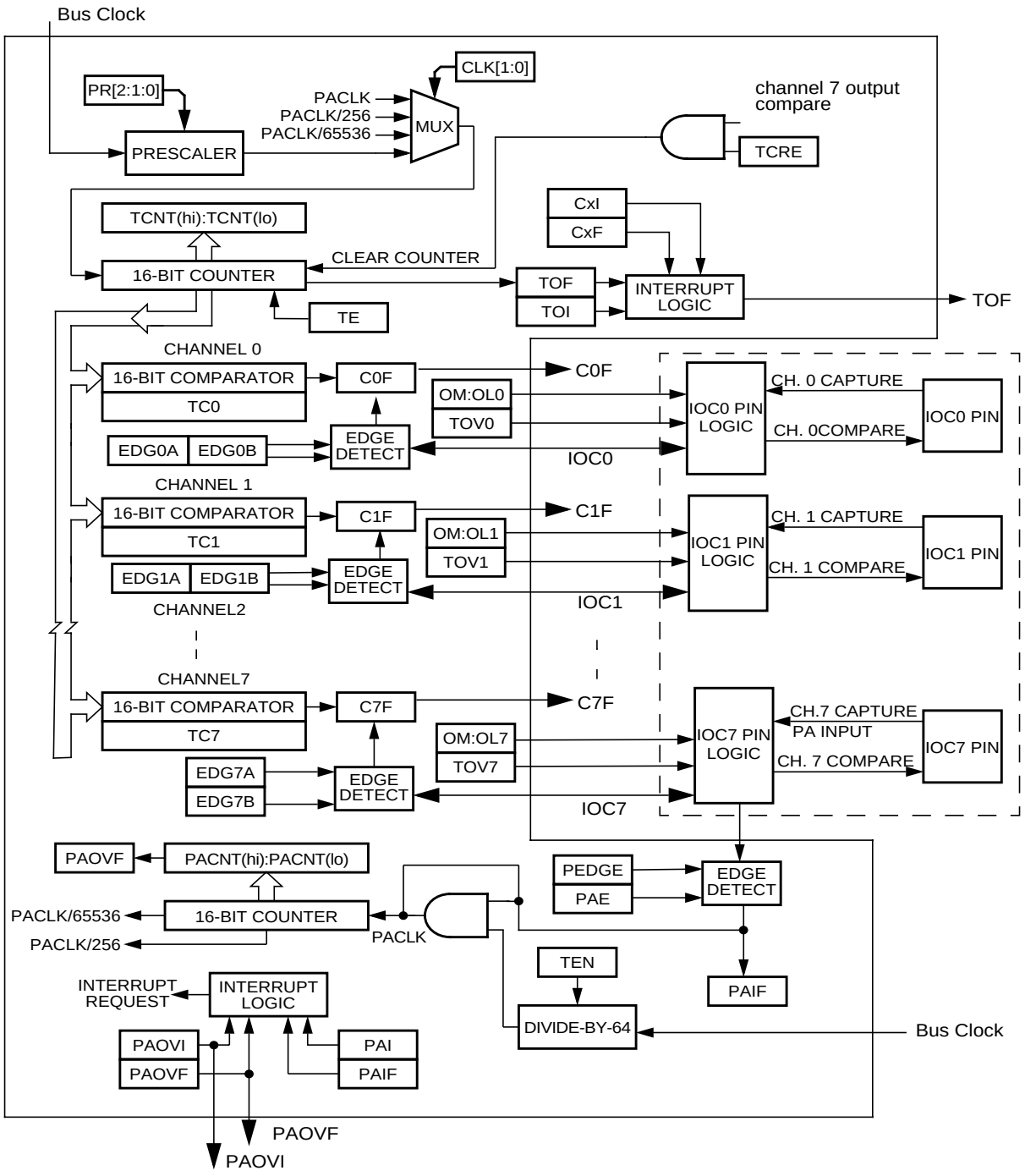

Figure 16-30. Detailed Timer Block Diagram

16.4.1 Prescaler

The prescaler divides the bus clock by 1,2,4,8,16,32,64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

Table 17-10. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms[1]
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * bus clock period
1	0001	4 * bus clock period
1	0002	6 * bus clock period
1	0003	8 * bus clock period
1	0004	10 * bus clock period
1	0005	12 * bus clock period
1	.....	.....
1	FFFD	131068 * bus clock period
1	FFFE	131070 * bus clock period
1	FFFF	131072 * bus clock period

1 When trimmed within specified accuracy. See electrical specifications for details.

The period can be calculated as follows depending of APICLK:

Period = 2*(APIR[15:0] + 1) * 0.1 ms or period = 2*(APIR[15:0] + 1) * bus clock period

It is possible to generate with the API a waveform at an external pin by enabling the API by setting APIFE and enabling the external access with setting APIEA. By setting APIES the waveform can be selected. If APIES is set, then at the external pin a clock is visible with 2 times the selected API Period (Table 17-10). If APIES is not set, then at the external pin will be a high pulse at the end of every selected period with the size of half of the min period (Table 17-10). See device level specification for connectivity.

17.4.9 Resets

This section describes how VREG_3V3 controls the reset of the MCU.The reset values of registers and signals are provided in Section 17.3, “Memory Map and Register Definition”. Possible reset sources are listed in Table 17-13.

Table 17-13. Reset Sources

Reset Source	Local Enable
Power-on reset	Always active
Low-voltage reset	Available only in Full Performance Mode

17.4.10 Description of Reset Operation

17.4.10.1 Power-On Reset (POR)

During chip power-up the digital core may not work if its supply voltage V_{DD} is below the POR deassertion level (V_{PORD}). Therefore, signal POR, which forces the other blocks of the device into reset, is kept high until V_{DD} exceeds V_{PORD}. The MCU will run the start-up sequence after POR deassertion. The power-on reset is active in all operation modes of VREG_3V3.

17.4.10.2 Low-Voltage Reset (LVR)

For details on low-voltage reset, see Section 17.4.5, “Low-Voltage Reset (LVR)”.

17.4.11 Interrupts

This section describes all interrupts originated by VREG_3V3.

The interrupt vectors requested by VREG_3V3 are listed in Table 17-14. Vector addresses and interrupt priorities are defined at MCU level.

Table 17-14. Interrupt Vectors

Interrupt Source	Local Enable
Low-voltage interrupt (LVI)	LVIE = 1; available only in Full Performance Mode
High Temperature Interrupt (HTI)	HTIE=1; available only in Full Performance Mode
Autonomous periodical interrupt (API)	APIE = 1

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x7F_FF0E located in P-Flash memory (see Table 18-3) as indicated by reset condition F in Figure 18-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 18-27. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

18.3.2.16 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-23. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

18.3.2.17 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-24. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

18.3.2.18 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Table 20-63. Erase D-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters
001	Global address [15:0] anywhere within the sector to be erased. See Section 20.1.2.2 for D-Flash sector size.

Upon clearing CCIF to launch the Erase D-Flash Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase D-Flash Sector operation has completed.

Table 20-64. Erase D-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-28)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.3 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 20-65. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

20.4.3.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with

Table A-6. Thermal Package Characteristics (9S12XS128)[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
LQFP 112							
1	D	Thermal resistance LQFP 112, single sided PCB[2]	θ_{JA}	—	—	58	°C/W
2	D	Thermal resistance LQFP 112, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	48	°C/W
3	D	Junction to Board LQFP 112	θ_{JB}	—	—	36	°C/W
4	D	Junction to Case LQFP 112[4]	θ_{JC}	—	—	14	°C/W
5	D	Junction to Package Top LQFP 112[5]	Ψ_{JT}	—	—	2	°C/W
QFP 80							
6	D	Thermal resistance QFP 80, single sided PCB[2]	θ_{JA}	—	—	56	°C/W
7	D	Thermal resistance QFP 80, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	43	°C/W
8	D	Junction to Board QFP 80	θ_{JB}	—	—	28	°C/W
9	D	Junction to Case QFP 80[4]	θ_{JC}	—	—	19	°C/W
10	D	Junction to Package Top QFP 80[5]	Ψ_{JT}	—	—	5	°C/W
LQFP 64							
11	D	Thermal resistance LQFP 64, single sided PCB[2]	θ_{JA}	—	—	64	°C/W
12	D	Thermal resistance LQFP 64, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	46	°C/W
13	D	Junction to Board LQFP 64	θ_{JB}	—	—	28	°C/W
14	D	Junction to Case LQFP 64[4]	θ_{JC}	—	—	13	°C/W
15	D	Junction to Package Top LQFP 64[5]	Ψ_{JT}	—	—	2	°C/W

1 The values for thermal resistance are achieved by package simulations

2 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection.

3 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-7 in a horizontal configuration in natural convection.

4 Junction to case thermal resistance was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. This basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.

5 Thermal characterization parameter Ψ_{JT} is the “resistance” from junction to reference point thermocouple on top center of the case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.

A.7 MSCAN

Table A-25. MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN wakeup dominant pulse filtered	t_{WUP}	—	—	1.5	µs
2	P	MSCAN wakeup dominant pulse pass	t_{WUP}	5	—	—	µs