



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12xs256j0mal">https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12xs256j0mal</a>

# Chapter 1

## Device Overview S12XS Family

### 1.1 Introduction

The new S12XS family of 16-bit micro controllers is a compatible, reduced version of the S12XE family. These families provide an easy approach to develop common platforms from low-end to high-end applications, minimizing the redesign of software and hardware.

Targeted at generic automotive applications and CAN nodes, some typical examples of these applications are: Body Controllers, Occupant Detection, Door Modules, RKE Receivers, Smart Actuators, Lighting Modules and Smart Junction Boxes amongst many others.

The S12XS family retains many of the features of the S12XE family including Error Correction Code (ECC) on Flash memory, a separate Data-Flash Module for code or data storage, a Frequency Modulated Locked Loop (IPLL) that improves the EMC performance and a fast ATD converter.

S12XS family delivers 32-bit performance with all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Freescale's existing 16-bit S12 and S12X MCU families. Like members of other S12X families, the S12XS family runs 16-bit wide accesses without wait states for all peripherals and memories.

The S12XS family is available in 112-pin LQFP, 80-pin QFP, 64-pin LQFP package options and maintains a high level of pin compatibility with the S12XE family. In addition to the I/O ports available in each module, up to 18 further I/O ports are available with interrupt capability allowing Wake-Up from stop or wait modes.

The peripheral set includes MSCAN, SPI, two SCIs, an 8-channel 24-bit periodic interrupt timer, 8-channel 16-bit Timer, 8-channel PWM and up to 16-channel 12-bit ATD converter.

Software controlled peripheral-to-port routing enables access to a flexible mix of the peripheral modules in the lower pin count package options.

#### 1.1.1 Features

Features of the S12XS Family are listed here. Please see Table D-1 for memory options and Table D-2 for the peripheral features that are available on the different family members.

- 16-bit CPU12X
  - Upward compatible with S12 instruction set with the exception of five Fuzzy instructions (MEM, WAV, WAVR, REV, REVW) which have been removed
  - Enhanced indexed addressing
  - Access to large data segments independent of PPAGE

- Time-out interrupt and peripheral triggers
- Start of timers can be aligned
- Up to 8 channel x 8-bit or 4 channel x 16-bit Pulse Width Modulator
  - Programmable period and duty cycle per channel
  - Center- or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
- Serial Peripheral Interface Module (SPI)
  - Configurable for 8 or 16-bit data size
  - Full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Master or Slave mode
  - MSB-first or LSB-first shifting
  - Serial clock phase and polarity options
- Two Serial Communication Interfaces (SCI)
  - Full-duplex or single wire operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
  - 13-bit baud rate selection
  - Programmable character length
  - Programmable polarity for transmitter and receiver
  - Receive wakeup on active edge
  - Break detect and transmit collision detect supporting LIN
- On-Chip Voltage Regulator
  - Two parallel, linear voltage regulators with bandgap reference
  - Low-voltage detect (LVD) with low-voltage interrupt (LVI)
  - Power-on reset (POR) circuit
  - Low-voltage reset (LVR)
- Low-power wake-up timer (API)
  - Internal oscillator driving a down counter
  - Trimmable to +/-5% accuracy
  - Time-out periods range from 0.2ms to ~13s with a 0.2ms resolution
- Input/Output
  - Up to 91 general-purpose input/output (I/O) pins depending on the package option and 2 input-only pins
  - Hysteresis and configurable pull up/pull down device on all input pins
  - Configurable drive strength on all output pins
- Package Options
  - 112-pin low-profile quad flat-pack (LQFP)
  - 80-pin quad flat-pack (QFP)

**Table 1-1. Device Register Memory Map (continued)**

Address	Module	Size (Bytes)
0x0368–0x07FF	Reserved	1176

**NOTE**

Reserved register space shown in Table 1-1 is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

### 1.1.5 Address Mapping

Figure 1-2 shows S12XS CPU and BDM local address translation to the global memory map. It indicates also the location of the internal resources in the memory map.

The clock generated by the PLL or oscillator provides the main system clock frequencies core clock and bus clock. As shown in Figure 1-6, these system clocks are used throughout the MCU to drive the core, the memories, and the peripherals.

The program Flash memory is supplied by the bus clock and the oscillator clock. The oscillator clock is used as a time base to derive the program and erase times for the NVMs.

The CAN modules may be configured to have their clock sources derived either from the bus clock or directly from the oscillator clock. This allows the user to select its clock based on the required jitter performance.

In order to ensure the presence of the clock the MCU includes an on-chip clock monitor connected to the output of the oscillator. The clock monitor can be configured to invoke the PLL self-clocking mode or to generate a system reset if it is allowed to time out as a result of no oscillator clock being present.

In addition to the clock monitor, the MCU also provides a clock quality checker which performs a more accurate check of the clock. The clock quality checker counts a predetermined number of clock edges within a defined time window to insure that the clock is running. The checker can be invoked following specific events such as on wake-up or clock monitor failure.

## 1.4 Modes of Operation

The MCU can operate in different modes. These are described in 1.4.1 Chip Configuration Summary.

The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in 1.4.2 Power Modes.

Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging. This is described in 1.4.3 Freeze Mode.

### 1.4.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 1-8). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of  $\overline{\text{RESET}}$ .

**Table 1-8. Chip Modes**

Chip Modes	MODC
Normal single chip	1
Special single chip	0

#### 1.4.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

**Table 6-4. DBGC1 Field Descriptions (continued)**

Field	Description
3 DBGBRK	<b>S12XDBG Breakpoint Enable Bit</b> — The DBGBRK bit controls whether the debugger will request a breakpoint to S12XCPU upon reaching the state sequencer Final State. If tracing is enabled, the breakpoint is generated on completion of the tracing session. If tracing is not enabled, the breakpoint is generated immediately. Please refer to Section 6.4.7 for further details. 0 No breakpoint on trigger. 1 Breakpoint on trigger
1–0 COMRV	<b>Comparator Register Visibility Bits</b> — These bits determine which bank of comparator register is visible in the 8-byte window of the S12XDBG module address map, located between 0x0028 to 0x002F. Furthermore these bits determine which register is visible at the address 0x0027. See Table 6-5.

**Table 6-5. COMRV Encoding**

COMRV	Visible Comparator	Visible Register at 0x0027
00	Comparator A	DBGSCR1
01	Comparator B	DBGSCR2
10	Comparator C	DBGSCR3
11	Comparator D	DBGMFR

### 6.3.2.2 Debug Status Register (DBGSR)

Address: 0x0021

	7	6	5	4	3	2	1	0
R	TBF	0	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

**Figure 6-4. Debug Status Register (DBGSR)**

Read: Anytime

Write: Never

**Table 6-6. DBGSR Field Descriptions**

Field	Description
7 TBF	<b>Trace Buffer Full</b> — The TBF bit indicates that the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines will be valid data, regardless of the value of DBGCNT bits CNT[6:0]. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit.
2–0 SSF[2:0]	<b>State Sequencer Flag Bits</b> — The SSF bits indicate in which state the State Sequencer is currently in. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal trigger, then the state sequencer returns to state0 and these bits are cleared to indicate that state0 was entered during the session. On arming the module the state sequencer enters state1 and these bits are forced to SSF[2:0] = 001. See Table 6-7.

### 10.1.3 Block Diagram

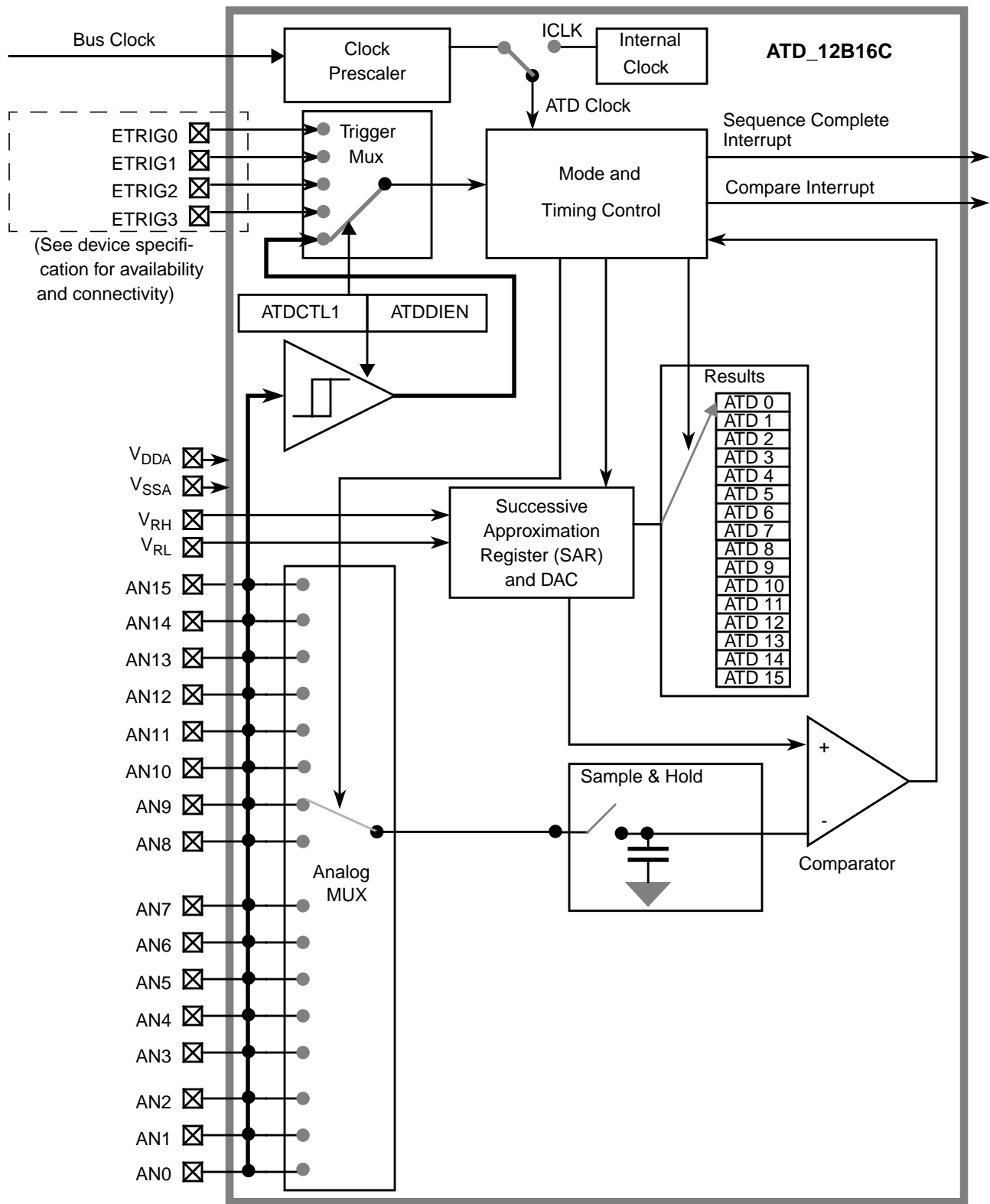


Figure 10-1. ADC12B16C Block Diagram

Table 10-10. Examples of ideal decimal ATD Results

Input Signal $V_{RL} = 0$ Volts $V_{RH} = 5.12$ Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	12-Bit Codes (transfer curve has 1.25mV offset) (resolution=1.25mV)
5.120 Volts	255	1023	4095
...	...	...	...
0.022	1	4	17
0.020	1	4	16
0.018	1	4	14
0.016	1	3	12
0.014	1	3	11
0.012	1	2	9
0.010	1	2	8
0.008	0	2	6
0.006	0	1	4
0.004	0	1	3
0.003	0	0	2
0.002	0	0	1
0.000	0	0	0

Table 10-11. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 10-12. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze



**Table 10-22. Conversion result mapping to ATDDRn**

A/D resolution	DJM	conversion result mapping to ATDDRn
8-bit data	0	Bit[11:4] = result, Bit[3:0]=0000
8-bit data	1	Bit[7:0] = result, Bit[11:8]=0000
10-bit data	0	Bit[11:2] = result, Bit[1:0]=00
10-bit data	1	Bit[9:0] = result, Bit[11:10]=00
12-bit data	X	Bit[11:0] = result

## 10.4 Functional Description

The ADC12B16C is structured into an analog sub-block and a digital sub-block.

### 10.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies  $V_{DDA}$  and  $V_{SSA}$  allow to isolate noise of other MCU circuitry from the analog sub-block.

#### 10.4.1.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external world and stores them as capacitor charge on a storage node.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must fall within the potential range of  $V_{SSA}$  to  $V_{DDA}$ .

During the hold process the analog input is disconnected from the storage node.

#### 10.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

#### 10.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine is automatically powered down.

Table 11-9. Time Segment 2 Values

TSEG22	TSEG21	TSEG20	Time Segment 2
0	0	0	1 Tq clock cycle <sup>(1)</sup>
0	0	1	2 Tq clock cycles
:	:	:	:
1	1	0	7 Tq clock cycles
1	1	1	8 Tq clock cycles

1. This setting is not valid. Please refer to Table 11-37 for valid settings.

Table 11-10. Time Segment 1 Values

TSEG13	TSEG12	TSEG11	TSEG10	Time segment 1
0	0	0	0	1 Tq clock cycle <sup>(1)</sup>
0	0	0	1	2 Tq clock cycles <sup>1</sup>
0	0	1	0	3 Tq clock cycles <sup>1</sup>
0	0	1	1	4 Tq clock cycles
:	:	:	:	:
1	1	1	0	15 Tq clock cycles
1	1	1	1	16 Tq clock cycles

1. This setting is not valid. Please refer to Table 11-37 for valid settings.

The bit time is determined by the oscillator frequency, the baud rate prescaler, and the number of time quanta (Tq) clock cycles per bit (as shown in Table 11-9 and Table 11-10).

*Eqn. 11-1*

$$\text{Bit Time} = \frac{(\text{Prescaler value})}{f_{\text{CANCLK}}} \cdot (1 + \text{TimeSegment1} + \text{TimeSegment2})$$

### 11.3.2.5 MSCAN Receiver Flag Register (CANRFLG)

A flag can be cleared only by software (writing a 1 to the corresponding bit position) when the condition which caused the setting is no longer valid. Every flag has an associated interrupt enable bit in the CANIER register.

Module Base + 0x0004

Access: User read/write<sup>(1)</sup>

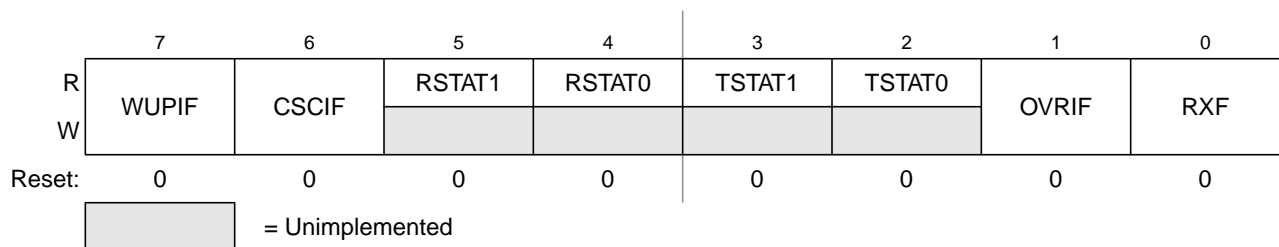


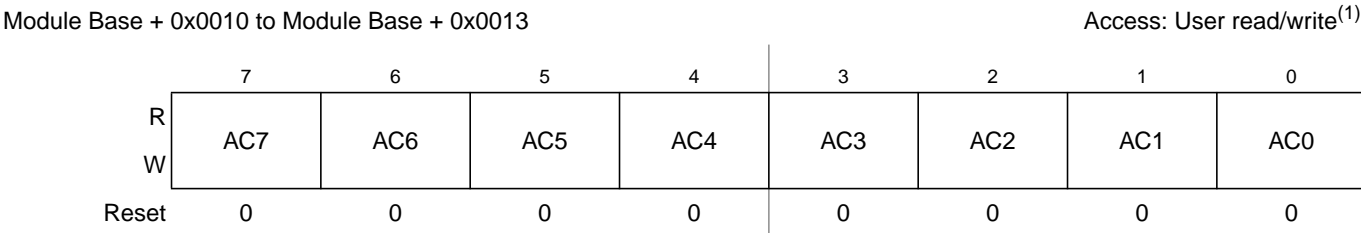
Figure 11-8. MSCAN Receiver Flag Register (CANRFLG)

### 11.3.2.17 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 11.3.3.1, “Identifier Registers (IDR0–IDR3)”) of incoming messages in a bit by bit manner (see Section 11.4.3, “Identifier Acceptance Filter”).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

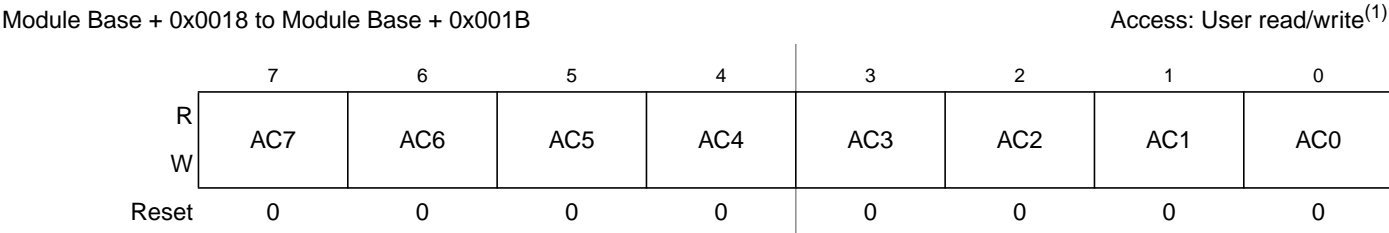


**Figure 11-20. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3**

1. Read: Anytime  
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

**Table 11-22. CANIDAR0–CANIDAR3 Register Field Descriptions**

Field	Description
7-0 AC[7:0]	<b>Acceptance Code Bits</b> — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.



**Figure 11-21. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7**

1. Read: Anytime  
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

### 11.4.5.5 MSCAN Sleep Mode

The CPU can request the MSCAN to enter this low power mode by asserting the SLPRQ bit in the CANCTL0 register. The time when the MSCAN enters sleep mode depends on a fixed synchronization delay and its current activity:

- If there are one or more message buffers scheduled for transmission (TXEx = 0), the MSCAN will continue to transmit until all transmit message buffers are empty (TXEx = 1, transmitted successfully or aborted) and then goes into sleep mode.
- If the MSCAN is receiving, it continues to receive and goes into sleep mode as soon as the CAN bus next becomes idle.
- If the MSCAN is neither transmitting nor receiving, it immediately goes into sleep mode.

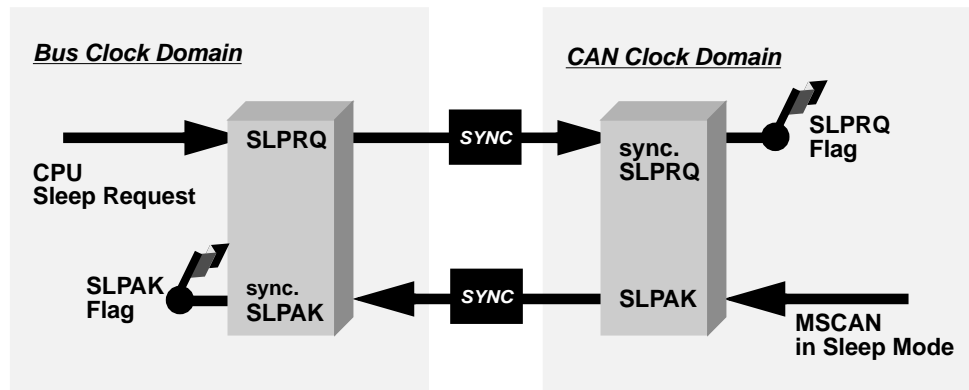


Figure 11-46. Sleep Request / Acknowledge Cycle

#### NOTE

The application software must avoid setting up a transmission (by clearing one or more TXEx flag(s)) and immediately request sleep mode (by setting SLPRQ). Whether the MSCAN starts transmitting or goes into sleep mode directly depends on the exact sequence of operations.

If sleep mode is active, the SLPRQ and SLPK bits are set (Figure 11-46). The application software must use SLPK as a handshake indication for the request (SLPRQ) to go into sleep mode.

When in sleep mode (SLPRQ = 1 and SLPK = 1), the MSCAN stops its internal clocks. However, clocks that allow register accesses from the CPU side continue to run.

If the MSCAN is in bus-off state, it stops counting the 128 occurrences of 11 consecutive recessive bits due to the stopped clocks. TXCAN remains in a recessive state. If RXF = 1, the message can be read and RXF can be cleared. Shifting a new message into the foreground buffer of the receiver FIFO (RxFG) does not take place while in sleep mode.

It is possible to access the transmit buffers and to clear the associated TXE flags. No message abort takes place while in sleep mode.

### 12.3.0.4 PIT Multiplex Register (PITMUX)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	0	0	0	PMUX3	PMUX2	PMUX1	PMUX0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-6. PIT Multiplex Register (PITMUX)

Read: Anytime

Write: Anytime

Table 12-5. PITMUX Field Descriptions

Field	Description
3:0 PMUX[3:0]	<b>PIT Multiplex Bits for Timer Channel 3:0</b> — These bits select if the corresponding 16-bit timer is connected to micro time base 1 or 0. If PMUX is modified, the corresponding 16-bit timer is switched to the other micro time base immediately. 0 The corresponding 16-bit timer counts with micro time base 0. 1 The corresponding 16-bit timer counts with micro time base 1.

### 12.3.0.5 PIT Interrupt Enable Register (PITINTE)

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	0	0	0	0	PINTE3	PINTE2	PINTE1	PINTE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-7. PIT Interrupt Enable Register (PITINTE)

Read: Anytime

Write: Anytime

Table 12-6. PITINTE Field Descriptions

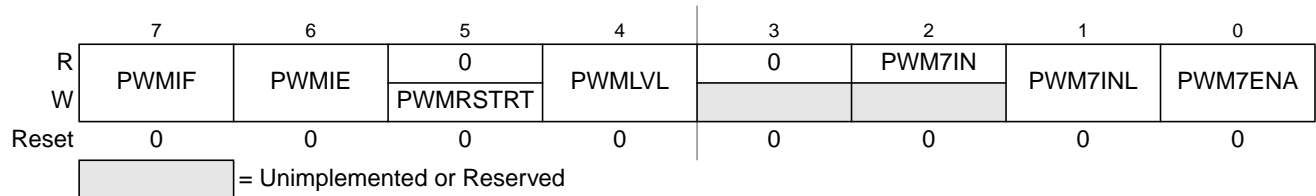
Field	Description
3:0 PINTE[3:0]	<b>PIT Time-out Interrupt Enable Bits for Timer Channel 3:0</b> — These bits enable an interrupt service request whenever the time-out flag PTF of the corresponding PIT channel is set. When an interrupt is pending (PTF set) enabling the interrupt will immediately cause an interrupt. To avoid this, the corresponding PTF flag has to be cleared first. 0 Interrupt of the corresponding PIT channel is disabled. 1 Interrupt of the corresponding PIT channel is enabled.

Write: Anytime

### 13.3.2.15 PWM Shutdown Register (PWMSDN)

The PWMSDN register provides for the shutdown functionality of the PWM module in the emergency cases. For proper operation, channel 7 must be driven to the active level for a minimum of two bus clocks.

Module Base + 0x0024



**Figure 13-17. PWM Shutdown Register (PWMSDN)**

Read: Anytime

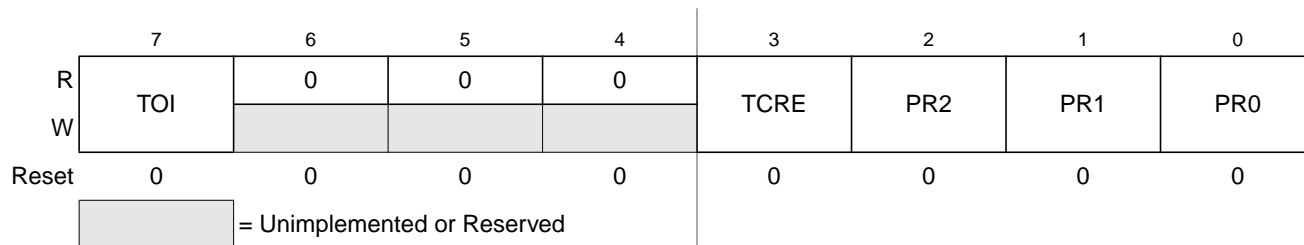
Write: Anytime

**Table 13-9. PWMSDN Field Descriptions**

Field	Description
7 PWMIF	<b>PWM Interrupt Flag</b> — Any change from passive to asserted (active) state or from active to passive state will be flagged by setting the PWMIF flag = 1. The flag is cleared by writing a logic 1 to it. Writing a 0 has no effect. 0 No change on PWM7IN input. 1 Change on PWM7IN input
6 PWMIE	<b>PWM Interrupt Enable</b> — If interrupt is enabled an interrupt to the CPU is asserted. 0 PWM interrupt is disabled. 1 PWM interrupt is enabled.
5 PWMRSTRT	<b>PWM Restart</b> — The PWM can only be restarted if the PWM channel input 7 is de-asserted. After writing a logic 1 to the PWMRSTRT bit (trigger event) the PWM channels start running after the corresponding counter passes next “counter == 0” phase. Also, if the PWM7ENA bit is reset to 0, the PWM do not start before the counter passes \$00. The bit is always read as “0”.
4 PWMLVL	<b>PWM Shutdown Output Level</b> If active level as defined by the PWM7IN input, gets asserted all enabled PWM channels are immediately driven to the level defined by PWMLVL. 0 PWM outputs are forced to 0 1 Outputs are forced to 1.
2 PWM7IN	<b>PWM Channel 7 Input Status</b> — This reflects the current status of the PWM7 pin.
1 PWM7INL	<b>PWM Shutdown Active Input Level for Channel 7</b> — If the emergency shutdown feature is enabled (PWM7ENA = 1), this bit determines the active level of the PWM7channel. 0 Active level is low 1 Active level is high
0 PWM7ENA	<b>PWM Emergency Shutdown Enable</b> — If this bit is logic 1, the pin associated with channel 7 is forced to input and the emergency shutdown feature is enabled. All the other bits in this register are meaningful only if PWM7ENA = 1. 0 PWM emergency feature disabled. 1 PWM emergency feature is enabled.

### 16.3.2.11 Timer System Control Register 2 (TSCR2)

Module Base + 0x000D



**Figure 16-19. Timer System Control Register 2 (TSCR2)**

Read: Anytime

Write: Anytime.

**Table 16-14. TSCR2 Field Descriptions**

Field	Description
7 TOI	<b>Timer Overflow Interrupt Enable</b> 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
3 TCRE	<b>Timer Counter Reset Enable</b> — This bit allows the timer counter to be reset by a successful output compare 7 event. This mode of operation is similar to an up-counting modulus counter. 0 Counter reset inhibited and counter free runs. 1 Counter reset by a successful output compare 7. <b>Note:</b> If TC7 = 0x0000 and TCRE = 1, TCNT will stay at 0x0000 continuously. If TC7 = 0xFFFF and TCRE = 1, TOF will never be set when TCNT is reset from 0xFFFF to 0x0000. <b>Note:</b> TCRE=1 and TC7!=0, the TCNT cycle period will be TC7 x "prescaler counter width" + "1 Bus Clock", for a more detail explanation please refer to Section 16.4.3, "Output Compare"
2 PR[2:0]	<b>Timer Prescaler Select</b> — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 16-15.

**Table 16-15. Timer Clock Selection**

PR2	PR1	PR0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

### 17.3.2.5 Autonomous Periodical Interrupt Rate High and Low Register (VREGAPIRH / VREGAPIRL)

The VREGAPIRH and VREGAPIRL register allows the configuration of the VREG\_3V3 autonomous periodical interrupt rate.

0x02F4

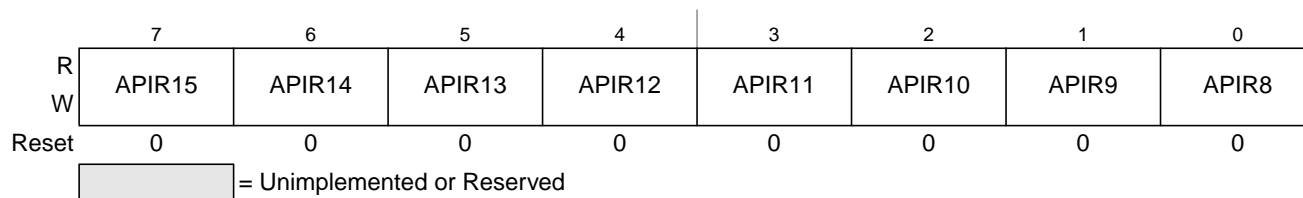


Figure 17-5. Autonomous Periodical Interrupt Rate High Register (VREGAPIRH)

0x02F5

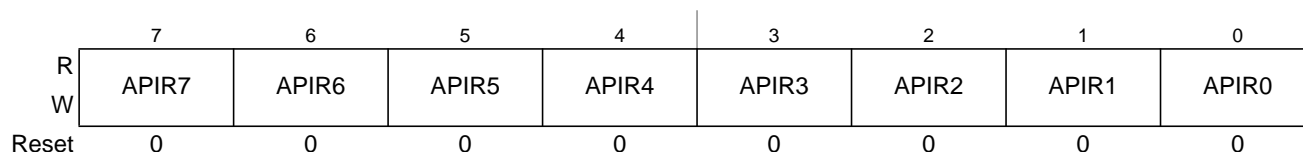


Figure 17-6. Autonomous Periodical Interrupt Rate Low Register (VREGAPIRL)

Table 17-9. VREGAPIRH / VREGAPIRL Field Descriptions

Field	Description
15-0 APIR[15:0]	<b>Autonomous Periodical Interrupt Rate Bits</b> — These bits define the timeout period of the API. See Table 17-10 for details of the effect of the autonomous periodical interrupt rate bits. Writable only if APIFE = 0 of VREGAPICL register.



P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

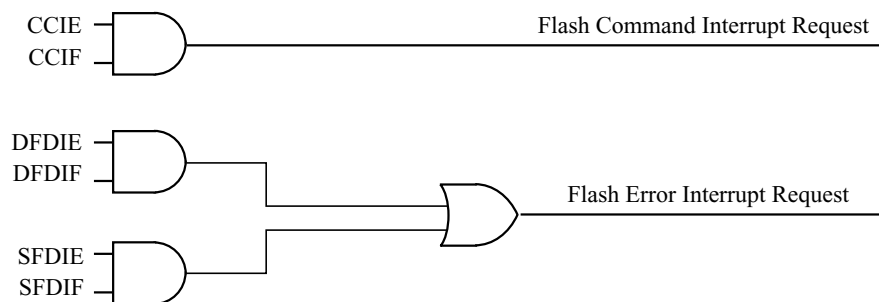
Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.

**Table 18-22. DFPROT Field Descriptions**

Field	Description
7 DPOPEN	<b>D-Flash Protection Control</b> 0 Enables D-Flash memory protection from program and erase with protected address range defined by DPS bits 1 Disables D-Flash memory protection from program and erase
4–0 DPS[4:0]	<b>D-Flash Protection Size</b> — The DPS[4:0] bits determine the size of the protected area in the D-Flash memory as shown in Table 18-23.

**Table 18-23. D-Flash Protection Address Range**

DPS[4:0]	Global Address Range	Protected Size
0_0000	0x10_0000 – 0x10_00FF	256 bytes
0_0001	0x10_0000 – 0x10_01FF	512 bytes
0_0010	0x10_0000 – 0x10_02FF	768 bytes
0_0011	0x10_0000 – 0x10_03FF	1024 bytes
0_0100	0x10_0000 – 0x10_04FF	1280 bytes
0_0101	0x10_0000 – 0x10_05FF	1536 bytes
0_0110	0x10_0000 – 0x10_06FF	1792 bytes
0_0111	0x10_0000 – 0x10_07FF	2048 bytes
0_1000	0x10_0000 – 0x10_08FF	2304 bytes
0_1001	0x10_0000 – 0x10_09FF	2560 bytes
0_1010	0x10_0000 – 0x10_0AFF	2816 bytes
0_1011	0x10_0000 – 0x10_0BFF	3072 bytes
0_1100	0x10_0000 – 0x10_0CFF	3328 bytes
0_1101	0x10_0000 – 0x10_0DFF	3584 bytes
0_1110	0x10_0000 – 0x10_0EFF	3840 bytes
0_1111	0x10_0000 – 0x10_0FFF	4096 bytes
1_0000	0x10_0000 – 0x10_10FF	4352 bytes
1_0001	0x10_0000 – 0x10_11FF	4608 bytes
1_0010	0x10_0000 – 0x10_12FF	4864 bytes
1_0011	0x10_0000 – 0x10_13FF	5120 bytes
1_0100	0x10_0000 – 0x10_14FF	5376 bytes
1_0101	0x10_0000 – 0x10_15FF	5632 bytes



**Figure 18-27. Flash Module Interrupts Implementation**

### 18.4.4 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 18.4.3, “Interrupts”).

### 18.4.5 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the CPU is allowed to enter stop mode.

## 18.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 18-10). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x7F\_FF0F.

The security state out of reset can be permanently changed by programming the security byte of the Flash configuration field. This assumes that you are starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take effect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

### 18.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x7F\_FF00–0x7F\_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 18.3.2.2), the Verify Backdoor Access Key command (see Section 18.4.2.11) allows the user to present four prospective keys for comparison to the

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x7F\_FF0E located in P-Flash memory (see Table 19-3) as indicated by reset condition F in Figure 19-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

**Table 19-27. FOPT Field Descriptions**

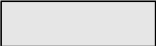
Field	Description
7–0 NV[7:0]	<b>Nonvolatile Bits</b> — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

### 19.3.2.16 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 19-23. Flash Reserved2 Register (FRSV2)**

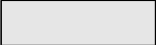
All bits in the FRSV2 register read 0 and are not writable.

### 19.3.2.17 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 19-24. Flash Reserved3 Register (FRSV3)**

All bits in the FRSV3 register read 0 and are not writable.

### 19.3.2.18 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag. Valid margin level settings for the Set Field Margin Level command are defined in Table 19-57.

**Table 19-57. Valid Set Field Margin Level Settings**

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level <sup>1</sup>
0x0002	User Margin-0 Level <sup>2</sup>
0x0003	Field Margin-1 Level <sup>1</sup>
0x0004	Field Margin-0 Level <sup>2</sup>

<sup>1</sup> Read margin to the erased state

<sup>2</sup> Read margin to the programmed state

**Table 19-58. Set Field Margin Level Command Error Handling**

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 19-28)
		Set if an invalid global address [22:16] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

### CAUTION

Field margin levels must only be used during verify of the initial factory programming.

### NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

#### 19.4.2.14 Erase Verify D-Flash Section Command

The Erase Verify D-Flash Section command will verify that a section of code in the D-Flash is erased. The Erase Verify D-Flash Section command defines the starting point of the data to be verified and the number of words.

**Table A-1. Absolute Maximum Ratings<sup>1</sup>**

Num	Rating	Symbol	Min	Max	Unit
1	I/O, regulator and analog supply voltage	$V_{DD35}$	-0.3	6.0	V
2	Digital logic supply voltage <sup>2</sup>	$V_{DD}$	-0.3	2.16	V
3	PLL supply voltage <sup>2</sup>	$V_{DDPLL}$	-0.3	2.16	V
4	NVM supply voltage <sup>2</sup>	$V_{DDF}$	-0.3	3.6	V
5	Voltage difference $V_{DDX}$ to $V_{DDA}$	$\Delta V_{DDX}$	-6.0	0.3	V
6	Voltage difference $V_{SSX}$ to $V_{SSA}$	$\Delta V_{SSX}$	-0.3	0.3	V
7	Digital I/O input voltage	$V_{IN}$	-0.3	6.0	V
8	Analog reference	$V_{RH}, V_{RL}$	-0.3	6.0	V
9	EXTAL, XTAL	$V_{ILV}$	-0.3	2.16	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins <sup>3</sup>	$I_D$	-25	+25	mA
12	Instantaneous maximum current Single pin limit for EXTAL, XTAL <sup>4</sup>	$I_{DL}$	-25	+25	mA
14	Maximum current Single pin limit for power supply pins	$I_{DV}$	-100	+100	mA
15	Storage temperature range	$T_{stg}$	-65	155	°C

<sup>1</sup> Beyond absolute maximum ratings device might be damaged.

<sup>2</sup> The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.

<sup>3</sup> All digital I/O pins are internally clamped to  $V_{SSX}$  and  $V_{DDX}$ , or  $V_{SSA}$  and  $V_{DDA}$ .

<sup>4</sup> Those pins are internally clamped to  $V_{SSPLL}$  and  $V_{DDPLL}$ .

## A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.