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#### Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12К х 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
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Port Integration Module (S12XSPIMV1)

# 2.3.7 PIM Reserved Registers





<sup>1</sup> Read: Always reads 0x00 Write: Unimplemented

# 2.3.8 Port E Data Register (PORTE)

Address 0x0008 (PRR) Access: User read/write<sup>1</sup> 7 6 5 4 3 2 0 1 R PE1 PE0 PE2 PE7 PE6 PE5 PE4 PE3 W Altern. **XCLKS** ECLK IRQ XIRQ Function ECLKX2 \_\_\_\_ \_\_\_\_ \_\_\_\_ \_ \_\_\_\_ 2 2 Reset 0 0 0 0 0 0 = Unimplemented or Reserved

### Figure 2-6. Port E Data Register (PORTE)

<sup>1</sup> Read: Anytime, the data source depends on the data direction value Write: Anytime

<sup>2</sup> These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.



Port Integration Module (S12XSPIMV1)

# 2.3.53 Port H Reduced Drive Register (RDRH)



### Table 2-50. RDRH Register Field Descriptions

Field	Description
7-0 RDRH	<ul> <li>Port H reduced drive—Select reduced drive for output pin</li> <li>This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin.</li> <li>1 Reduced drive selected (approx. 1/5 of the full drive strength)</li> <li>0 Full drive strength enabled</li> </ul>

# 2.3.54 Port H Pull Device Enable Register (PERH)



Write: Anytime

Table 2-51. PERH Register Field Descriptions

Field	Description
7-0 PERH Port H pull device enable—Enable p This bit controls whether a pull device no effect. The polarity is selected by the 1 Pull device enabled	ull device on input pin on the associated port input pin is active. If a pin is used as output this bit has ne related polarity select register bit.

Interrupt (S12XINTV2)

Priority	XILVL2	XILVL1	XILVL0	Meaning
	0	0	0	Interrupt request is disabled
low	0	0	1	Priority level 1
	0	1	0	Priority level 2
	0	1	1	Priority level 3
	1	0	0	Priority level 4
	1	0	1	Priority level 5
	1	1	0	Priority level 6
high	1	1	1	Priority level 7

#### Table 4-6. XGATE Interrupt Priority Levels

### 4.3.2.3 Interrupt Request Configuration Address Register (INT\_CFADDR)

Address: 0x0127





Read: Anytime

Write: Anytime

### Table 4-7. INT\_CFADDR Field Descriptions

Field	Description
7–4 INT_CFADDR[7:4]	Interrupt Request Configuration Data Register Select Bits — These bits determine which of the 128 configuration data registers are accessible in the 8 register window at INT_CFDATA0-7. The hexadecimal value written to this register corresponds to the upper nibble of the lower byte of the address of the interrupt vector, i.e., writing 0xE0 to this register selects the configuration data register block for the 8 interrupt vector requests starting with vector at address (vector base + 0x00E0) to be accessible as INT_CFDATA0-7. Note: Writing all 0s selects non-existing configuration registers. In this case write accesses to INT_CFDATA0-7 will be ignored and read accesses will return all 0.

## 4.3.2.4 Interrupt Request Configuration Data Registers (INT\_CFDATA0-7)

The eight register window visible at addresses INT\_CFDATA0-7 contains the configuration data for the block of eight interrupt requests (out of 128) selected by the interrupt configuration address register (INT\_CFADDR) in ascending order. INT\_CFDATA0 represents the interrupt configuration data register of the vector with the lowest address in this block, while INT\_CFDATA7 represents the interrupt configuration data register of the vector with the highest address, respectively.



# 5.4.3 BDM Hardware Commands

Hardware commands are used to read and write target system memory locations and to enter active background debug mode. Target system memory includes all memory that is accessible by the CPU on the SOC which can be on-chip RAM, non-volatile memory (e.g. EEPROM, Flash EEPROM), I/O and control registers, and all external memory.

Hardware commands are executed with minimal or no CPU intervention and do not require the system to be in active BDM for execution, although, they can still be executed in this mode. When executing a hardware command, the BDM sub-block waits for a free bus cycle so that the background access does not disturb the running application program. If a free cycle is not found within 128 clock cycles, the CPU is momentarily frozen so that the BDM can steal a cycle. When the BDM finds a free cycle, the operation does not intrude on normal CPU operation provided that it can be completed in a single cycle. However, if an operation requires multiple cycles the CPU is frozen until the operation is complete, even though the BDM found a free cycle.

The BDM hardware commands are listed in Table 5-6.

The READ\_BD and WRITE\_BD commands allow access to the BDM register locations. These locations are not normally in the system memory map but share addresses with the application in memory. To distinguish between physical memory locations that share the same address, BDM memory resources are enabled just for the READ\_BD and WRITE\_BD access cycle. This allows the BDM to access BDM locations unobtrusively, even if the addresses conflict with the application memory map.

Command	Opcode (hex)	Data	Description
BACKGROUND	90	None	Enter background mode if firmware is enabled. If enabled, an ACK will be issued when the part enters active background mode.
ACK_ENABLE	D5	None	Enable Handshake. Issues an ACK pulse after the command is executed.
ACK_DISABLE	D6	None	Disable Handshake. This command does not issue an ACK pulse.
READ_BD_BYTE	E4	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
READ_BD_WORD	EC	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Must be aligned access.
READ_BYTE	E0	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
READ_WORD	E8	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Must be aligned access.
WRITE_BD_BYTE	C4	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
WRITE_BD_WORD	СС	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Must be aligned access.
WRITE_BYTE	C0	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.

### Table 5-6. Hardware Commands



#### Background Debug Module (S12XBDMV2)

cycle to recognize this edge. The target measures delays from this perceived start of the bit time while the host measures delays from the point it actually drove BKGD low to start the bit up to one target clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 5-8 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later that eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.



Figure 5-8. BDM Host-to-Target Serial Bit Timing

The receive cases are more complicated. Figure 5-9 shows the host receiving a logic 1 from the target system. Since the host is asynchronous to the target, there is up to one clock-cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.



#### S12X Debug (S12XDBGV3) Module

next state for the state sequencer following a match. The three debug state control registers are located at the same address in the register address map (0x0027). Each register can be accessed using the COMRV bits in DBGC1 to blend in the required register. The COMRV = 11 value blends in the match flag register (DBGMFR).

Table 6-18.	State Control	<b>Register A</b>	ccess Encodina
14010 0 101	••••••••••••		

COMRV	Visible State Control Register
00	DBGSCR1
01	DBGSCR2
10	DBGSCR3
11	DBGMFR

### 6.3.2.7.1 Debug State Control Register 1 (DBGSCR1)

Address: 0x0027



Figure 6-9. Debug State Control Register 1 (DBGSCR1)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and S12XDBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 00. The state control register 1 selects the targeted next state whilst in State1. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.8.1. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

### Table 6-19. DBGSCR1 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State1, based upon the match event.

### Table 6-20. State1 Sequencer Next State Selection

SC[3:0]	Description
0000	Any match triggers to state2
0001	Any match triggers to state3
0010	Any match triggers to Final State
0011	Match2 triggers to State2 Other matches have no effect
0100	Match2 triggers to State3 Other matches have no effect
0101	Match2 triggers to Final State Other matches have no effect
0110	Match0 triggers to State2 Match1 triggers to State3 Other matches have no effect

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Figure 8-1. Block diagram of S12XECRG

# 8.2 Signal Description

This section lists and describes the signals that connect off chip.

# 8.2.1 V<sub>DDPLL</sub>, V<sub>SSPLL</sub>

These pins provides operating voltage ( $V_{DDPLL}$ ) and ground ( $V_{SSPLL}$ ) for the IPLL circuitry. This allows the supply voltage to the IPLL to be independently bypassed. Even if IPLL usage is not required  $V_{DDPLL}$  and  $V_{SSPLL}$  must be connected to properly.

# 8.2.2 **RESET**

**RESET** is an active low bidirectional reset pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an system reset (internal to MCU) has been triggered.



Field	Description
7 RTIF	<ul> <li>Real Time Interrupt Flag — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request.</li> <li>0 RTI time-out has not yet occurred.</li> <li>1 RTI time-out has occurred.</li> </ul>
6 PORF	<ul> <li>Power on Reset Flag — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect.</li> <li>0 Power on reset has not occurred.</li> <li>1 Power on reset has occurred.</li> </ul>
5 LVRF	<ul> <li>Low Voltage Reset Flag — LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect.</li> <li>0 Low voltage reset has not occurred.</li> <li>1 Low voltage reset has occurred.</li> </ul>
4 LOCKIF	<ul> <li>IPLL Lock Interrupt Flag — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE=1), LOCKIF causes an interrupt request.</li> <li>0 No change in LOCK bit.</li> <li>1 LOCK bit has changed.</li> </ul>
3 LOCK	<ul> <li>Lock Status Bit — LOCK reflects the current state of IPLL lock condition. This bit is cleared in Self Clock Mode.</li> <li>Writes have no effect.</li> <li>VCOCLK is not within the desired tolerance of the target frequency.</li> <li>VCOCLK is within the desired tolerance of the target frequency.</li> </ul>
2 ILAF	Illegal Address Reset Flag — ILAF is set to 1 when an illegal address reset occurs. Refer to S12XMMC BlockGuide for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect.0 Illegal address reset has not occurred.1 Illegal address reset has occurred.
1 SCMIF	<ul> <li>Self Clock Mode Interrupt Flag — SCMIF is set to 1 when SCM status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (SCMIE=1), SCMIF causes an interrupt request.</li> <li>0 No change in SCM bit.</li> <li>1 SCM bit has changed.</li> </ul>
0 SCM	<ul> <li>Self Clock Mode Status Bit — SCM reflects the current clocking mode. Writes have no effect.</li> <li>MCU is operating normally with OSCCLK available.</li> <li>MCU is operating in Self Clock Mode with OSCCLK in an unknown state. All clocks are derived from PLLCLK running at its minimum frequency f<sub>SCM</sub>.</li> </ul>

### Table 8-4. CRGFLG Field Descriptions

# 8.3.2.5 S12XECRG Interrupt Enable Register (CRGINT)

This register enables S12XECRG interrupt requests.

Module Base + 0x0004



### Figure 8-7. S12XECRG Interrupt Enable Register (CRGINT)

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# 8.4.1.5 Computer Operating Properly Watchdog (COP)

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus a system reset is initiated (see Section 8.4.1.5, "Computer Operating Properly Watchdog (COP)"). The COP runs with a gated OSCCLK. Three control bits in the COPCTL register allow selection of seven COP time-out periods.

When COP is enabled, the program must write \$55 and \$AA (in this order) to the ARMCOP register during the selected time-out period. Once this is done, the COP time-out period is restarted. If the program fails to do this and the COP times out, the part will reset. Also, if any value other than \$55 or \$AA is written, the part is immediately reset.

Windowed COP operation is enabled by setting WCOP in the COPCTL register. In this mode, writes to the ARMCOP register to clear the COP timer must occur in the last 25% of the selected time-out period. A premature write will immediately reset the part.

If PCE bit is set, the COP will continue to run in Pseudo Stop Mode.

## 8.4.1.6 Real Time Interrupt (RTI)

The RTI can be used to generate a hardware interrupt at a fixed periodic rate. If enabled (by setting RTIE=1), this interrupt will occur at the rate selected by the RTICTL register. The RTI runs with a gated OSCCLK. At the end of the RTI time-out period the RTIF flag is set to one and a new RTI time-out period starts immediately.

A write to the RTICTL register restarts the RTI time-out period.

If the PRE bit is set, the RTI will continue to run in Pseudo Stop Mode.

# 8.4.2 Operation Modes

### 8.4.2.1 Normal Mode

The S12XECRG block behaves as described within this specification in all normal modes.

## 8.4.2.2 Self Clock Mode

If the external clock frequency is not available due to a failure or due to long crystal start-up time, the Bus Clock and the Core Clock are derived from the PLLCLK running at self clock mode frequency  $f_{SCM}$ ; this mode of operation is called Self Clock Mode. This requires CME = 1 and SCME = 1, which is the default after reset. If the MCU was clocked by the PLLCLK prior to entering Self Clock Mode, the PLLSEL bit will be cleared. If the external clock signal has stabilized again, the S12XECRG will automatically select OSCCLK to be the system clock and return to normal mode. See Section 8.4.1.4, "Clock Quality Checker" for more information on entering and leaving Self Clock Mode.



Pulse-Width Modulator (S12PWM8B8CV1)

## 14.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
  - Receive wakeup on active edge
  - Transmit collision detect supporting LIN
  - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

## 14.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run mode
- Wait mode
- Stop mode

# 14.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register locations do not have any effect and reads of these locations return a zero. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SCIBDH <sup>1</sup>	R W	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
0x0001 SCIBDL <sup>1</sup>	R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x0002 SCICR1 <sup>1</sup>	R W	LOOPS	SCISWAI	RSRC	М	WAKE	ILT	PE	PT
0x0000 SCIASR1 <sup>2</sup>	R W	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
0x0001 SCIACR1 <sup>2</sup>	R W	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
0x0002	R	0	0	0	0	0	BERRM1	BERRMO	BKDEE
SCIACR2 <sup>2</sup>	w						BERRIN	BERRING	BRBTE
0x0003 SCICR2	R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x0004	R	TDRE	тс	RDRF	IDLE	OR	NF	FE	PF
SCISR1	w								
0x0005 SCISR2	R W	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
0x0006	R	R8	To	0	0	0	0	0	0
SCIDRH	w		18						
0x0007	R	R7	R6	R5	R4	R3	R2	R1	R0
SCIDRL	w	T7	Т6	T5	T4	Т3	T2	T1	Т0

1. These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2, These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

= Unimplemented or Reserved

Figure 14-2. SCI Register Summary

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Serial Peripheral Interface (S12SPIV5)

# 15.2.3 SS — Slave Select Pin

This pin is used to output the select signal from the SPI module to another peripheral with which a data transfer is to take place when it is configured as a master and it is used as an input to receive the slave select signal when the SPI is configured as slave.

# 15.2.4 SCK — Serial Clock Pin

In master mode, this is the synchronous output clock. In slave mode, this is the synchronous input clock.

# 15.3 Memory Map and Register Definition

This section provides a detailed description of address space and registers used by the SPI.

## 15.3.1 Module Memory Map

The memory map for the SPI is given in Figure 15-2. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level. Reads from the reserved bits return zeros and writes to the reserved bits have no effect.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SPICR1	R W	SPIE	SPE	SPTIE	MSTR	CPOL	СРНА	SSOE	LSBFE
0x0001 SPICR2	R W	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
0x0002 SPIBR	R W	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
0x0003 SPISR	R W	SPIF	0	SPTEF	MODF	0	0	0	0
0x0004 SPIDRH	R W	R15 T15	R14 T14	R13 T13	R12 T12	R11 T11	R10 T10	R9 T9	R8 T8
0x0005 SPIDRL	R W	R7 T7	R6 T6	R5 T5	R4 T4	R3 T3	R2 T2	R1 T1	R0 T0
0x0006 Reserved	R W								
0x0007 Reserved	R W								
	ſ		= Unimplem	ented or Res	erved				

Figure 15-2. SPI Register Summary



### CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

FCMD	Command	Function on D-Flash Memory
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.

#### Table 19-30. D-Flash Commands

# 19.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 19.3.2.7).

### CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

### 19.4.2.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and D-Flash blocks have been erased.

Table 19-31. Erase Verify All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB P	arameters
000	0x01	Not required

#### 128 KByte Flash Module (S12XFTMR128K1V1)

CCOBIX[2:0]	FCCOB P	arameters
000	0x09	Global address [22:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Register	Error Bit	Error Condition
	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 19-28)
		Set if an invalid global address [22:16] is supplied
FSTAT		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 19-46. Erase Flash Block Command Error Handling

### 19.4.2.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 19-47. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB	Parameters
000	0x0A	Global address [22:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 19.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.



64 KByte Flash Module (S12XFTMR64K1V1)

## 20.4.2.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 20-9). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 20-3). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

CCOBIX[2:0]	FCCOB P	arameters	
000	0x0C	Not required	
001	Ke	y 0	
010	Key 1		
011	Key 2		
100	Key 3		

 Table 20-51. Verify Backdoor Access Key Command FCCOB Requirements

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x7F\_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 20-52. Verily backuoor Access Rey Commanu Error nanuling	Table 20-52. Verif	y Backdoor Access Ke	ey Command Error Handling
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Register	Error Bit	Error Condition
		Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
	ACCERR	Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 20.3.2.2)
FSTAT		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

### 20.4.2.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of a specific P-Flash or D-Flash block.



**Detailed Register Address Map** 

### 0x0040–0x006F Timer Module (TIM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0057	TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0058	TC4H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0059	TC4L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005A	TC5H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005B	TC5L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005C	TC6H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005D	TC6L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005E	TC7H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005F	TC7L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0060	PACTL	R W	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
0x0061	PAFLG	R W	0	0	0	0	0	0	PAOVF	PAIF
0x0062	PACNTH	R W	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
0x0063	PACNTL	R W	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
0x0064-	Reserved	R	0	0	0	0	0	0	0	0
0x006B		W								
0x006C	OCPD	W	OCPD7	OCPD6	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
0x006D	Reserved	R W								
0x006E	PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x006F	Reserved	R W	0	0	0	0	0	0	0	0

## 0x0070–0x00C7 Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0070- 0x00C7	Reserved	R	0	0	0	0	0	0	0	0
		W								



**Detailed Register Address Map** 

### Detailed MSCAN Foreground Receive and Transmit Buffer Layout (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xXX1F		R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
	CANALISKE	w								

### 0x0180–0x023F Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180-	Percentred	R	0	0	0	0	0	0	0	0
0x023F	Reserved	W								

### 0x0240–0x027F Port Integration Module (PIM) Map 5 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R W	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
0v02/1	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
070241	1 111	W								
0x0242	DDRT	R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
0x0243	RDRT	R W	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
0x0244	PERT	R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
0x0245	PPST	R W	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
0x0246	Reserved	R	0	0	0	0	0	0	0	0
	Reserved	W								
0x0247	PTTRR	R W	PTTRR7	PTTRR6	PTTRR5	PTTRR4	0	PTTRR2	PTTRR1	PTTRR0