Renesas Electronics America Inc - R5F21346UDFP#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART, USB
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21346udfp-v0

1.3 Block Diagram

Figure 1.3 and Figure 1.4 show a Block Diagram of Each Group.

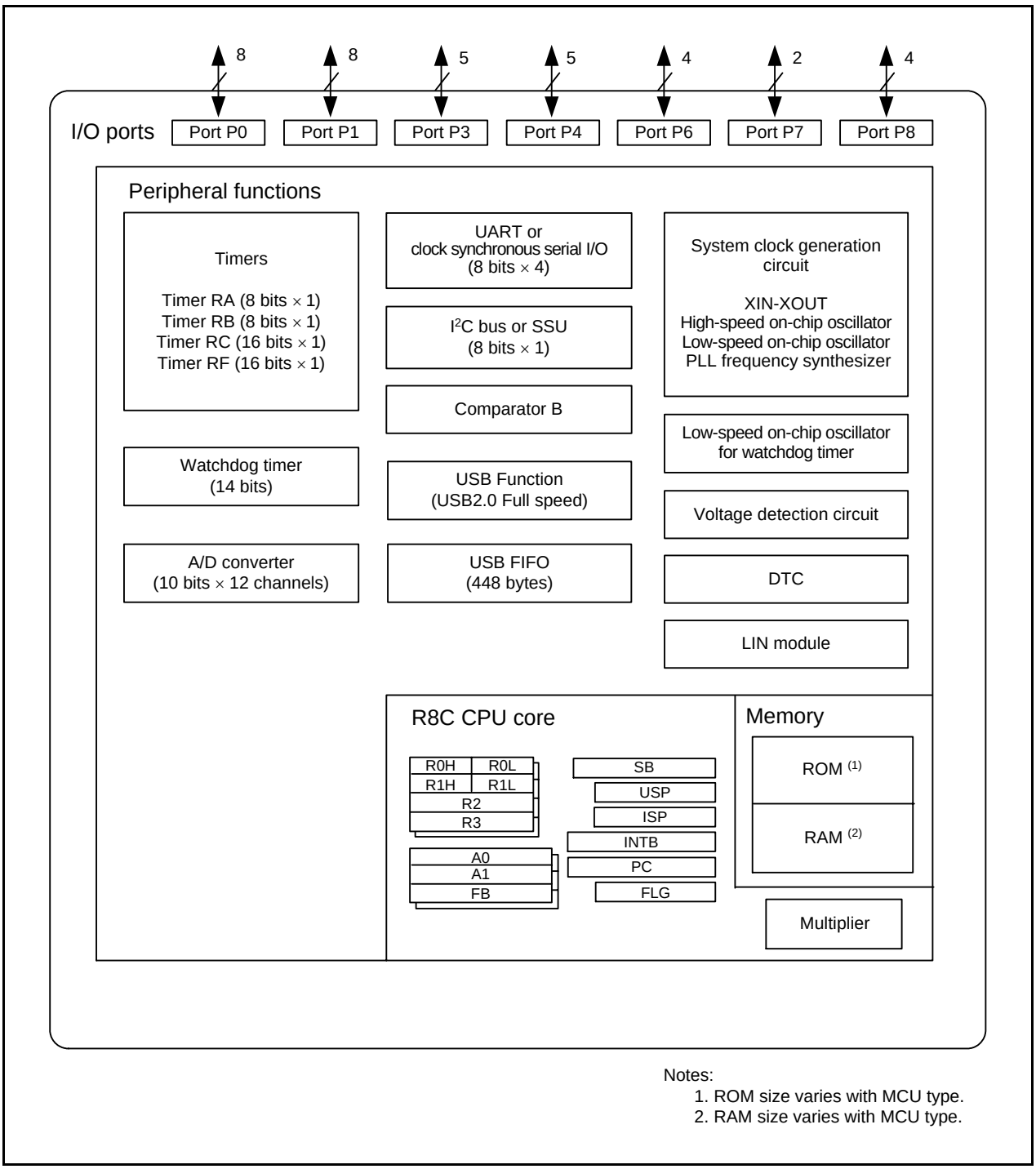


Figure 1.3 Block Diagram of R8C/34U Group

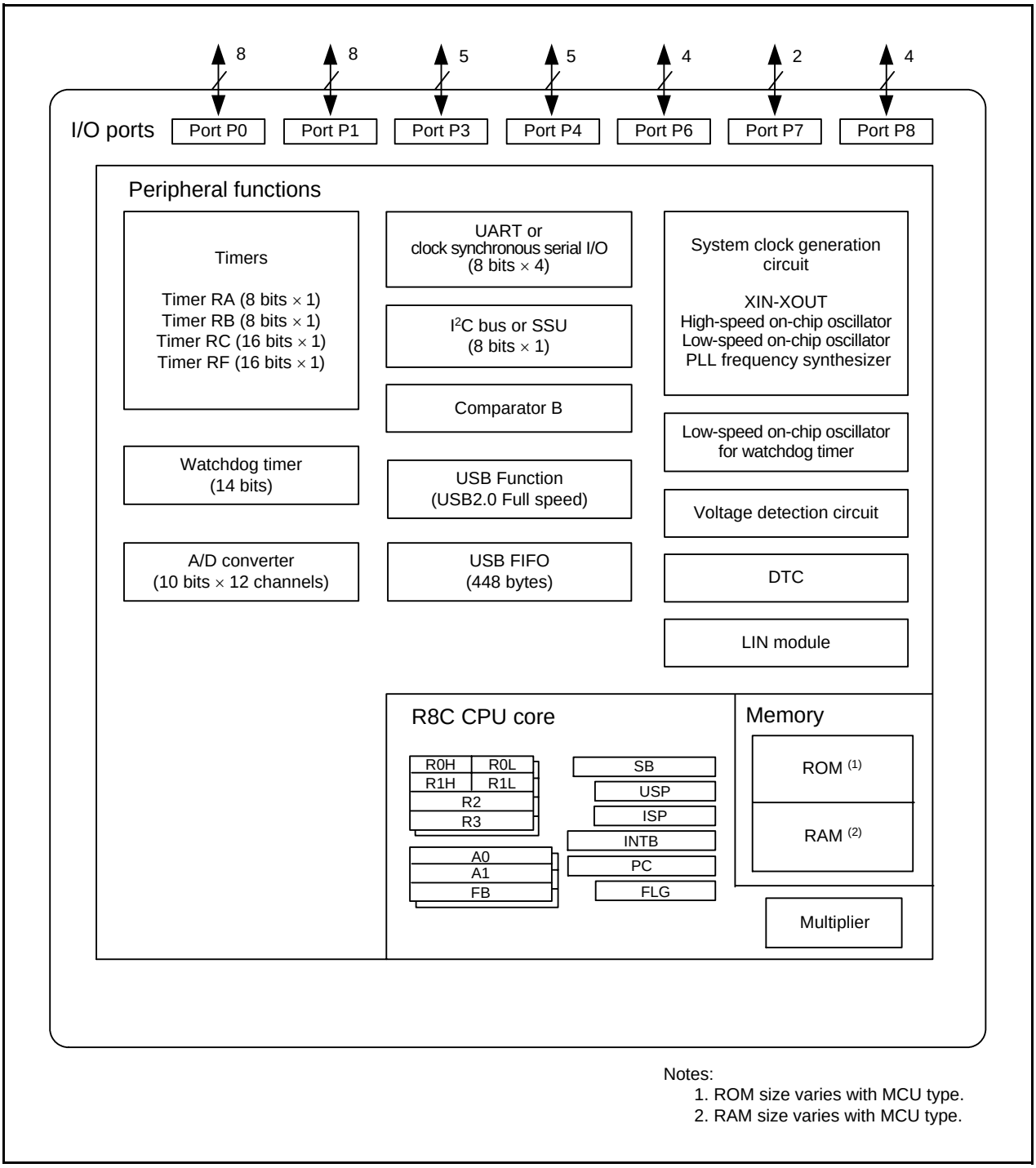
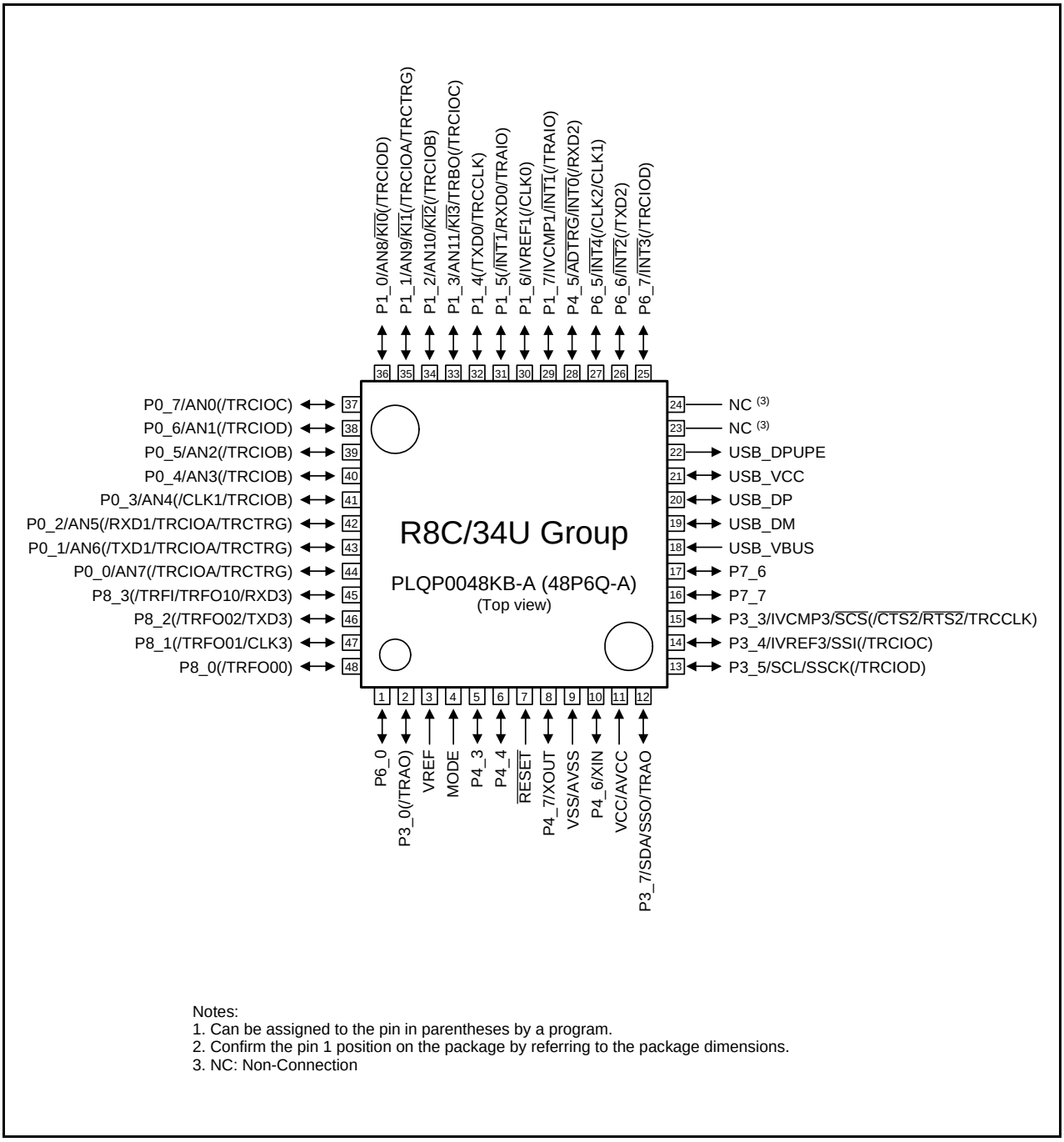


Figure 1.4 Block Diagram of R8C/34K Group

1.4 Pin Assignment

Figure 1.5 and Figure 1.6 show Pin Assignment (Top View) of Each Group. Tables 1.6 and 1.7 outline the Pin Name Information by Pin Number.

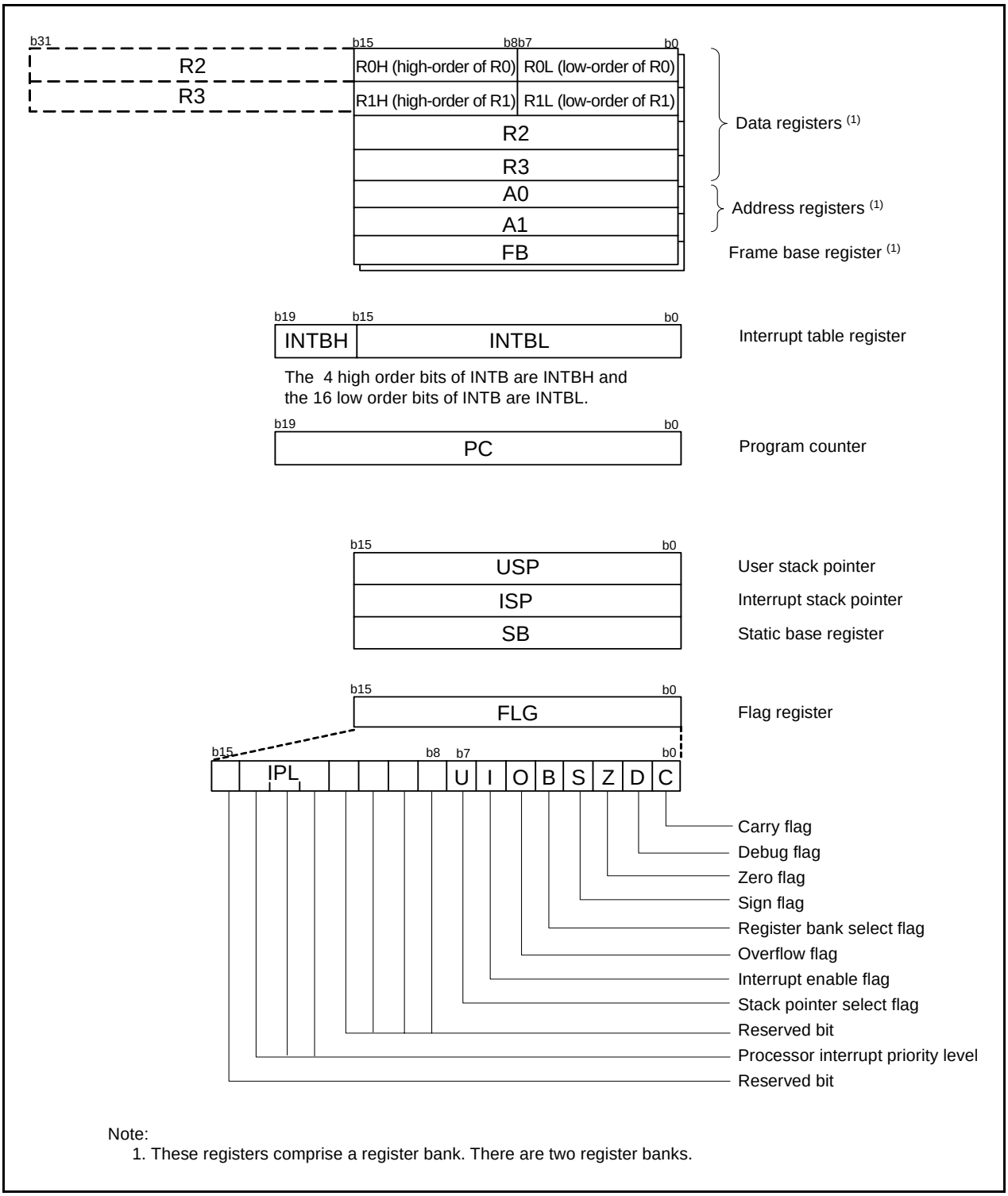


Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.
3. NC: Non-Connection

Figure 1.5 Pin Assignment (Top View) of R8C/34U Group

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



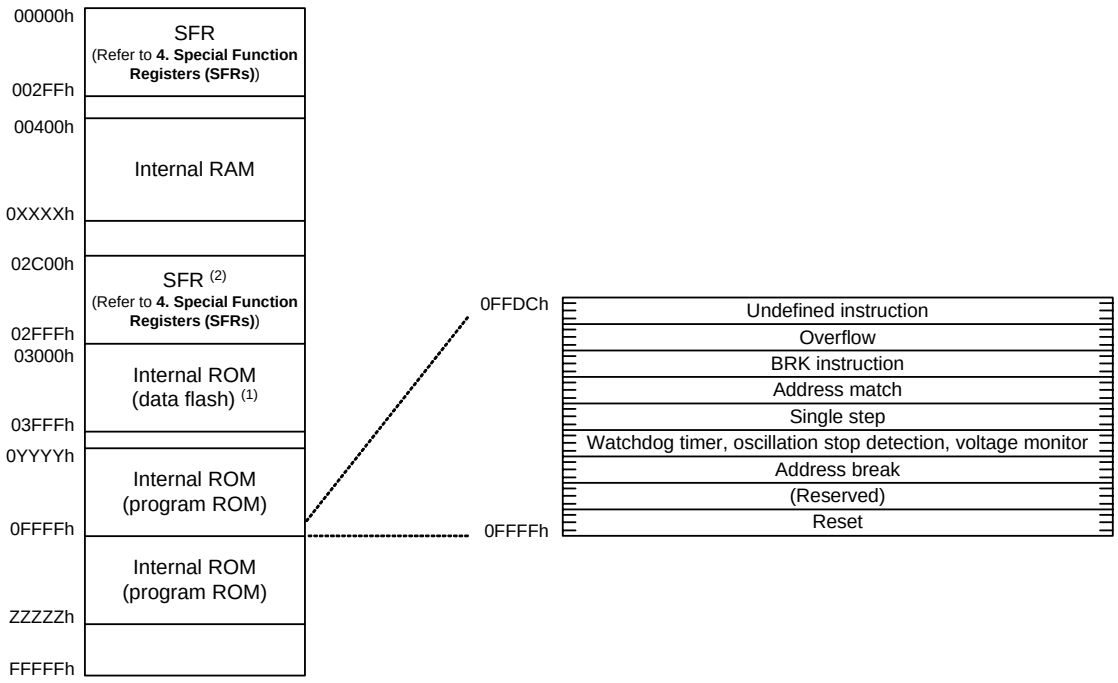
Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

3. Memory

3.1 R8C/34U Group

Figure 3.2 is a Memory Map of R8C/34U Group. The R8C/34U Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 8-Kbyte internal RAM area is allocated addresses 00400h to 023FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



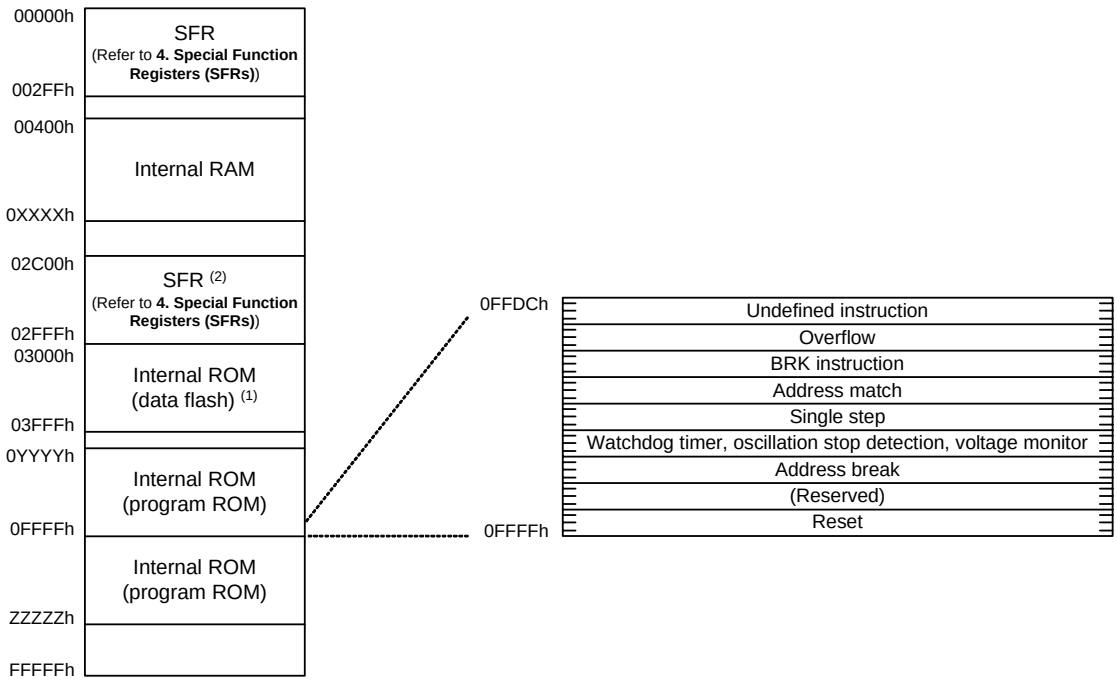
Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21346UNFP, R5F21346UDFP R5F21346UNXXXFP, R5F21346UDXXXFP	32 Kbytes	08000h	-	4 Kbytes	013FFh
R5F21348UNFP, R5F21348UDFP R5F21348UNXXXFP, R5F21348UDXXXFP	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh

Figure 3.1 Memory Map of R8C/34U Group

3.2 R8C/34K Group

Figure 3.2 is a Memory Map of R8C/34K Group. The R8C/34K Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. A 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 8-Kbyte internal RAM area is allocated addresses 00400h to 023FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21348KNFP, R5F21348KDFP R5F21348KNXXXFP, R5F21348KDXXXFP	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh
R5F2134CKNFP, R5F2134CKDFP R5F2134CKNXXXFP, R5F213CKDXXXFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/34K Group

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h	USB RESUME Interrupt Control Register	USBRSMIC	XXXXX000b
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h	Timer RF Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	USB INT Interrupt Control Register	USBINTIC	XXXXX000b
006Ch	UART3 Transmit Interrupt Control Register	S3RIC	XXXXX000b
006Dh	UART3 Receive Interrupt Control Register	S3TIC	XXXXX000b
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2E30h	Interrupt Enable Register 0	INTENB0	00h
2E31h			00h
2E32h	Interrupt Enable Register 1 (2)	INTENB1	00h
2E33h			00h
2E34h			
2E35h			
2E36h	BRDY Interrupt Enable Register	BRDYENB	00h
2E37h			00h
2E38h	NRDY Interrupt Enable Register	NRDYENB	00h
2E39h			00h
2E3Ah	BEMP Interrupt Enable Register	BEMPENB	00h
2E3Bh			00h
2E3Ch	SOF Output Configuration Register	SOFCFG	00h
2E3Dh			00h
2E3Eh			
2E3Fh			
2E40h	Interrupt Status Register 0	INTSTS0	X0000000b
2E41h			X0000000b
2E42h	Interrupt Status Register 1 (2)	INTSTS1	00h
2E43h			00h
2E44h			
2E45h			
2E46h	BRDY Interrupt Status Register	BRDYSTS	00h
2E47h			00h
2E48h	NRDY Interrupt Status Register	NRDYSTS	00h
2E49h			00h
2E4Ah	BEMP Interrupt Status Register	BEMPSTS	00h
2E4Bh			00h
2E4Ch	Frame Number Register	FRMNUM	00h
2E4Dh			00h
2E4Eh			
2E4Fh			
2E50h	USB Address Register	USBADDR	00h
2E51h			00h
2E52h			
2E53h			
2E54h	USB Request Type Register	USBREQ	00h
2E55h			00h
2E56h	USB Request Value Register	USBVAL	00h
2E57h			00h
2E58h	USB Request Index Register	USBINDX	00h
2E59h			00h
2E5Ah	USB Request Length Register	USBLENG	00h
2E5Bh			00h
2E5Ch	DCP Configuration Register	DCPCFG	00h
2E5Dh			00h
2E5Eh	DCP Max Packet Size Register	DCPMAXP	40h
2E5Fh			00h
2E60h	DCP Control Register	DCPCTR	40h
2E61h			00h
2E62h			
2E63h			
2E64h	Pipe Window Select Register	PIPESEL	00h
2E65h			00h
2E66h			
2E67h			
2E68h	Pipe Window Configuration Register	PIPECFG	00h
2E69h			00h
2E6Ah			
2E6Bh			
2E6Ch	Pipe Max Packet Size Register	PIPEMAXP	00h
2E6Dh			00h
2E6Eh	Pipe Period Control Register (2)	PIPEPERI	00h
2E6Fh			00h

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/34U Group.

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

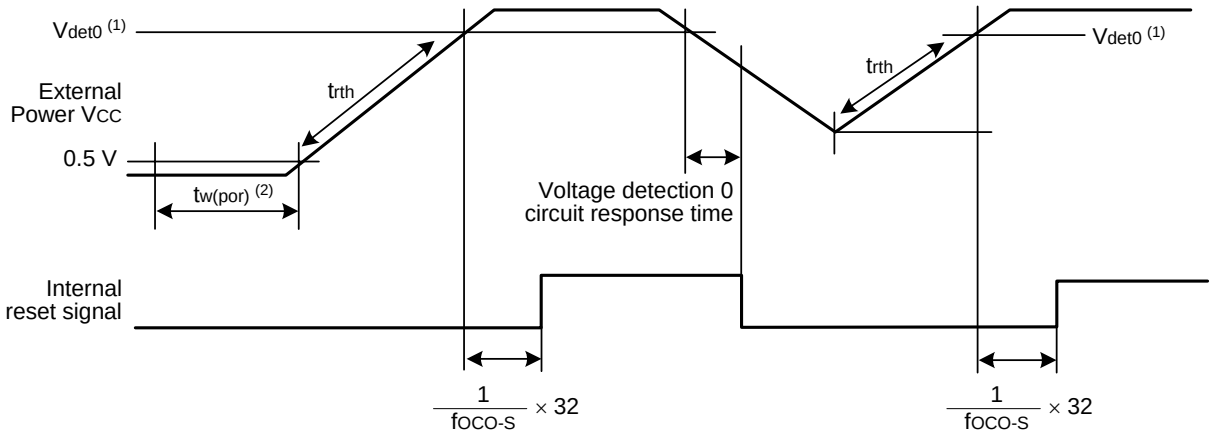
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of V_{CC} from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.5 Power-on Reset Circuit Electrical Characteristics

Table 5.31 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRFI, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, $\overline{SSO}$, $\overline{SSCK}$, $\overline{SCS}$			0.05	0.20	—	V
		$\overline{RESET}$			0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.2 V, V_{CC} = 2.2 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 2.2 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V, T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 5.41 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	V_{CC} + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	$V_I = V_{ref} \pm 100$ mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	—	17.5	—	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.44 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 (7)	—	85	°C
—	Data hold time (8)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. –40 °C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

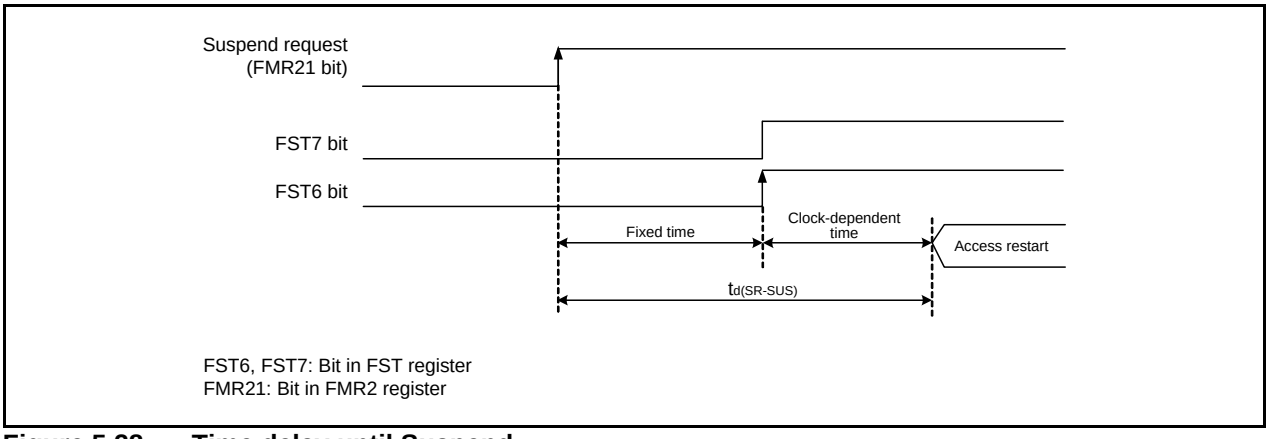


Figure 5.28 Time delay until Suspend

Table 5.47 Voltage Detection 2 Circuit Electrical Characteristics

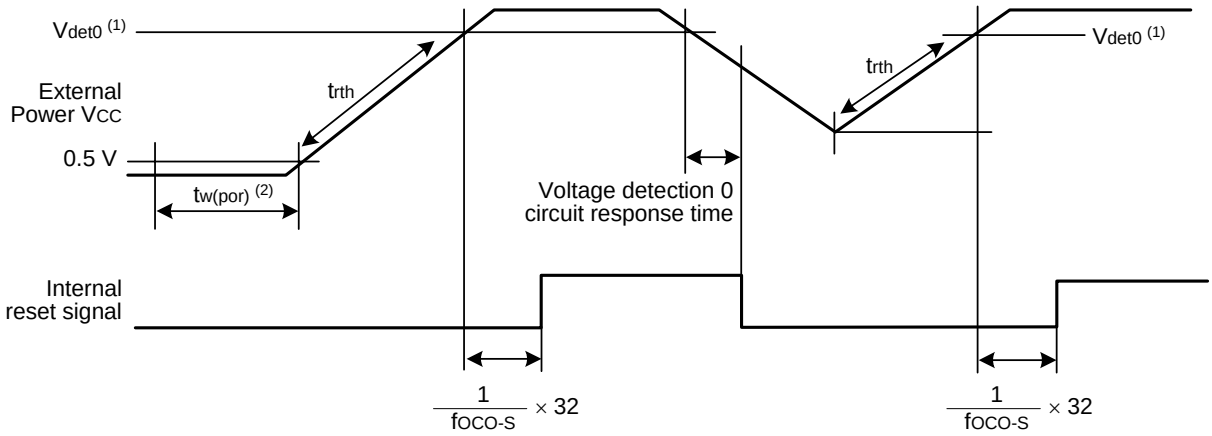
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of V_{CC} from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.48 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.29 Power-on Reset Circuit Electrical Characteristics

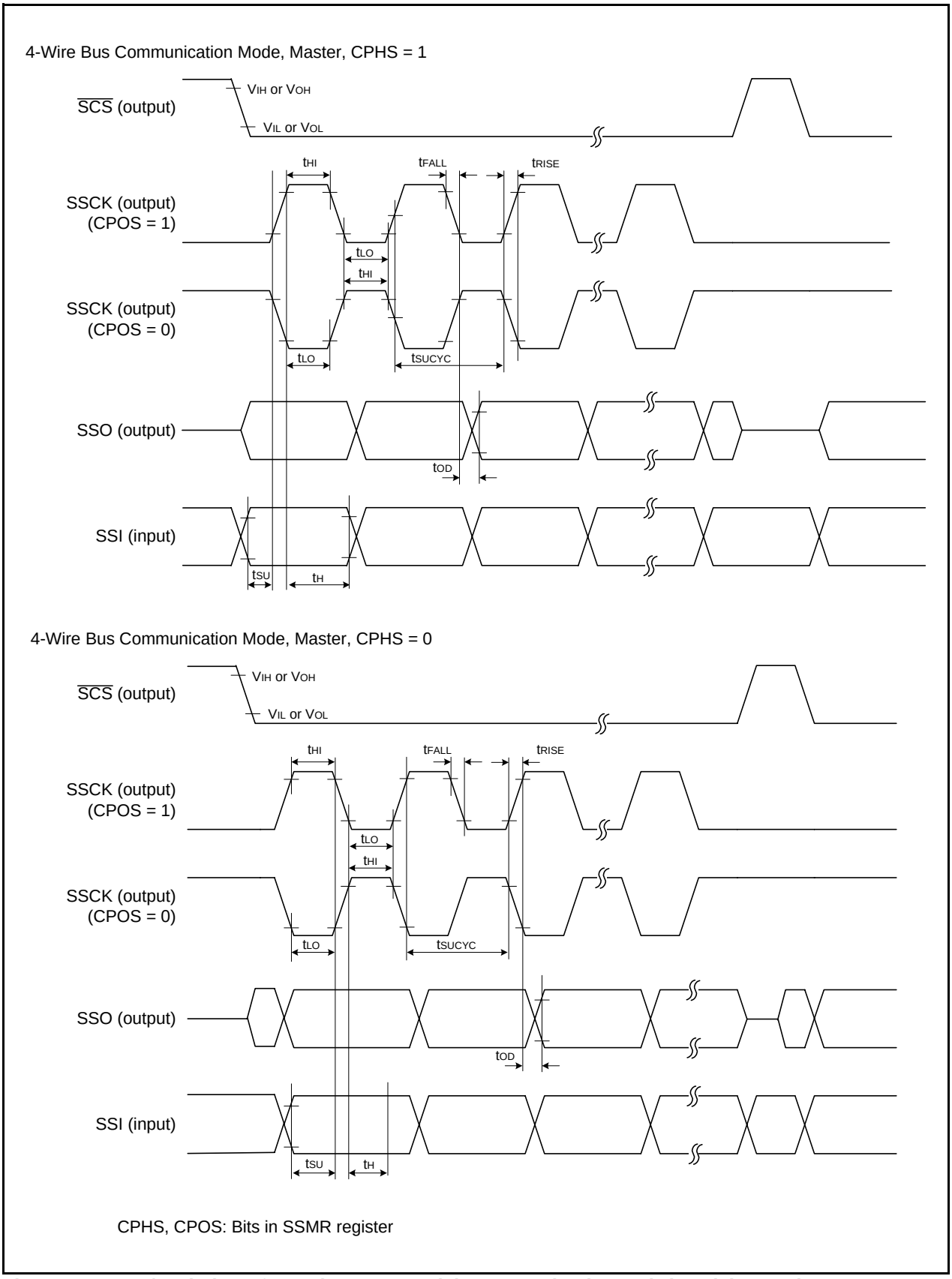
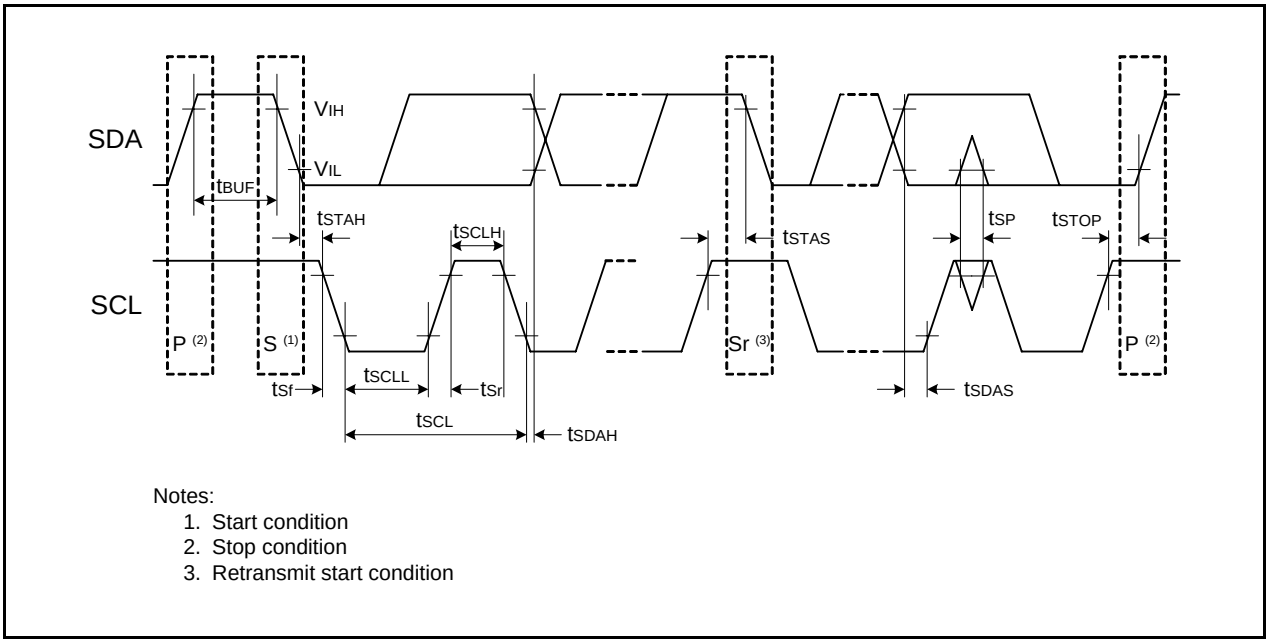


Figure 5.30 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.53 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.33 I/O Timing of I²C bus Interface

Table 5.55 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing Requirements (Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 5.56 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

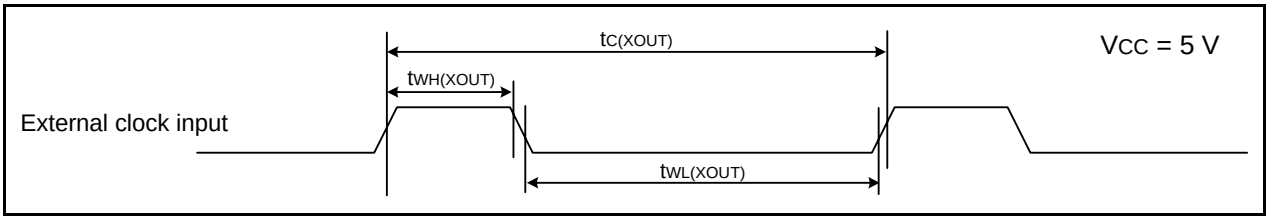


Figure 5.34 External Clock Input Timing Diagram when V_{CC} = 5 V

Table 5.57 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	—	ns

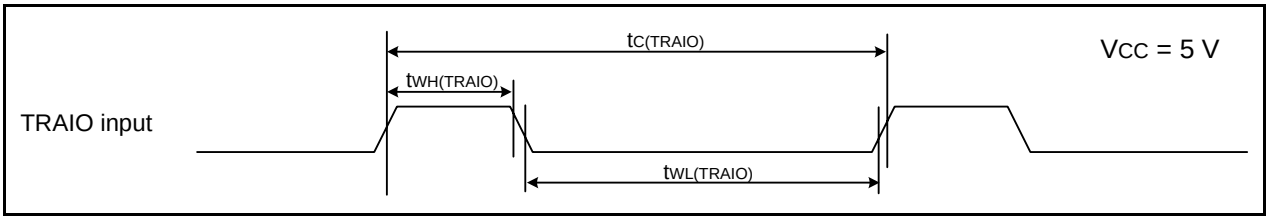


Figure 5.35 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.58 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 (1)	—	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200 (2)	—	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200 (2)	—	ns

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

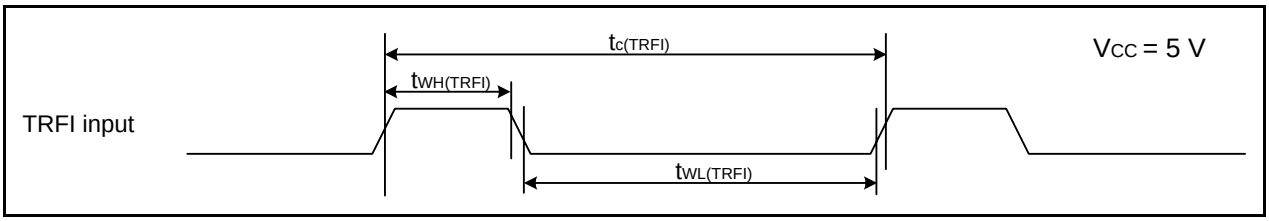


Figure 5.36 TRFI Input Timing Diagram when V_{CC} = 5 V

Table 5.66 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input “H” width	150	—	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

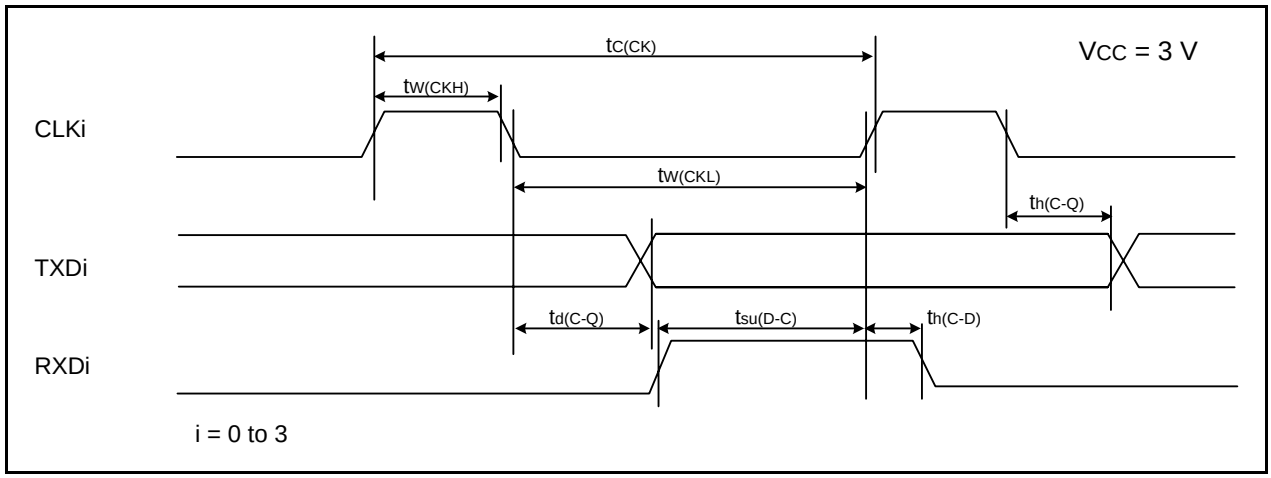


Figure 5.42 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.67 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

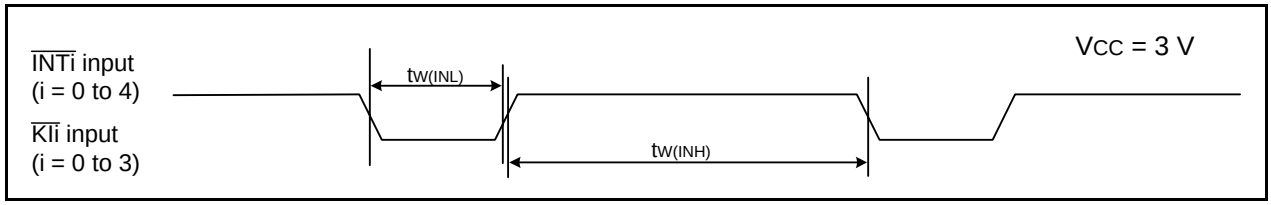


Figure 5.43 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

REVISION HISTORY	R8C/34U Group, R8C/34K Group Datasheet

Rev.	Date	Description	
		Page	Summary
• R8C/34U Group Datasheet (R01DS0039EJ0100)			
0.01	Nov 08, 2010	—	First Edition issued
1.00	Feb 25, 2011	All pages	“Preliminary”, “Under development” deleted
		3	Table 1.2 revised
		4	Table 1.3, Figure 1.1 revised
		5	Figure 1.2 revised
		6	Figure 1.3 revised
		7	Table 1.4 revised
		9	Table 1.6 revised
		10	Table 1.7 revised
		14	3.1 revised, Figure 3.1 “Part Number” added
		15	Table 4.1 0026h revised
		16	Table 4.2 0041h revised, 0050h, 005Bh, 005Ch and 005Fh added
		17	Table 4.3 0090h and 00BBh revised
		21	Table 4.7 0181h revised
		26	Table 4.12 2E04h and 2E05h revised
		27	Table 4.13 2E40h and 2E41h revised 2E42h, 2E43h, 2E6Eh and 2E6Fh deleted
		29	Table 4.15 2F04h, 2F11h and 2F13h deleted, 2F10h added
		30 to 57	5. Electrical Characteristics added
• R8C/34K Group Datasheet (R01DS0040EJ0100)			
0.01	Nov 08, 2010	—	First Edition issued
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		3	Table 1.2 revised
		4	Table 1.3, Figure 1.1 revised
		5	Figure 1.2 revised
		6	Figure 1.3 revised
		7	Table 1.4 revised
		9	Table 1.6 revised
		10	Table 1.7 revised
		14	3.1 revised, Figure 3.1 “Part Number” added
		15	Table 4.1 0026h revised
		16	Table 4.2 0050h, 005Bh, 005Ch and 005Fh added
		17	Table 4.3 0090h and 00BBh revised
		21	Table 4.7 0181h revised
		26	Table 4.12 2E04h and 2E05h revised
		27	Table 4.13 2E3Ch and 2E3Dh added, 2E40h and 2E41h revised
		28	Table 4.14 2ED2h to 2ED7h deleted
		29	Table 4.15 2F04h and 2F13h deleted
		30 to 57	5. Electrical Characteristics added