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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I <sup>2</sup> C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 15x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf364lpmc-g-jne2">https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf364lpmc-g-jne2</a>



Pin No		Pin Name	I/O circuit type	Pin state type
LQFP64 QFN64	LQFP48 QFN48			
9	5	P57	N	K
		DTTIOX_0		
		INT07_0		
		TIOB3_0		
		SCK3_0 (SCL3_0)		
		ADTG_0		
10	6	P30	G	K
		RTO00_0		
		AIN0_1		
		INT08_0		
		TIOA4_0		
		SIN2_0		
11	7	P31	G	K
		RTO01_0		
		BIN0_1		
		INT09_0		
		TIOB4_0		
		SOT2_0 (SDA2_0)		
12	8	P32	G	K
		RTO02_0		
		ZIN0_1		
		INT10_0		
		TIOA5_0		
		SCK2_0 (SCL2_0)		
13	9	P33	G	K
		RTO03_0		
		INT11_0		
		TIOB5_0		
		SIN4_1		
14	10	P34	G	K
		RTO04_0		
		INT12_0		
		TIOA6_0		
		SOT4_1 (SDA4_1)		
15	11	P35	G	Q
		WKUP2		
		RTO05_0		
		INT13_0		
		TIOB6_0		
		SCK4_1 (SCL4_1)		

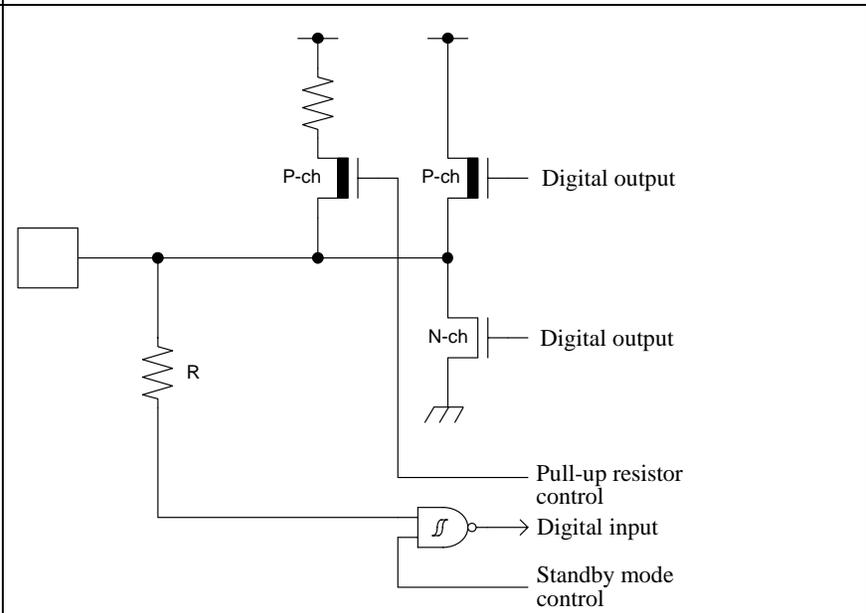
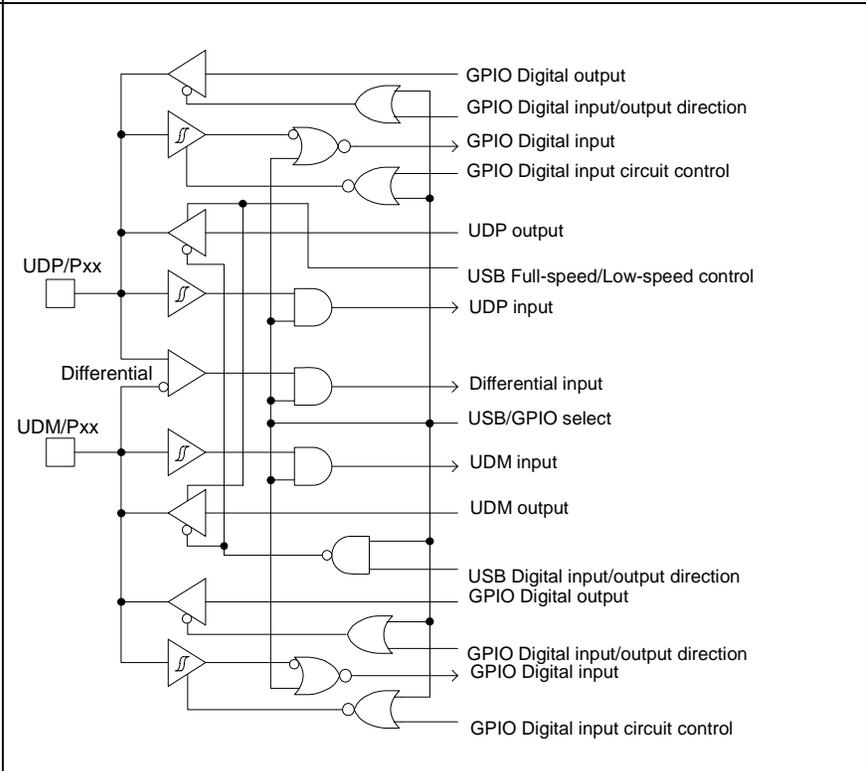
#### 4.2 List of Pin Functions

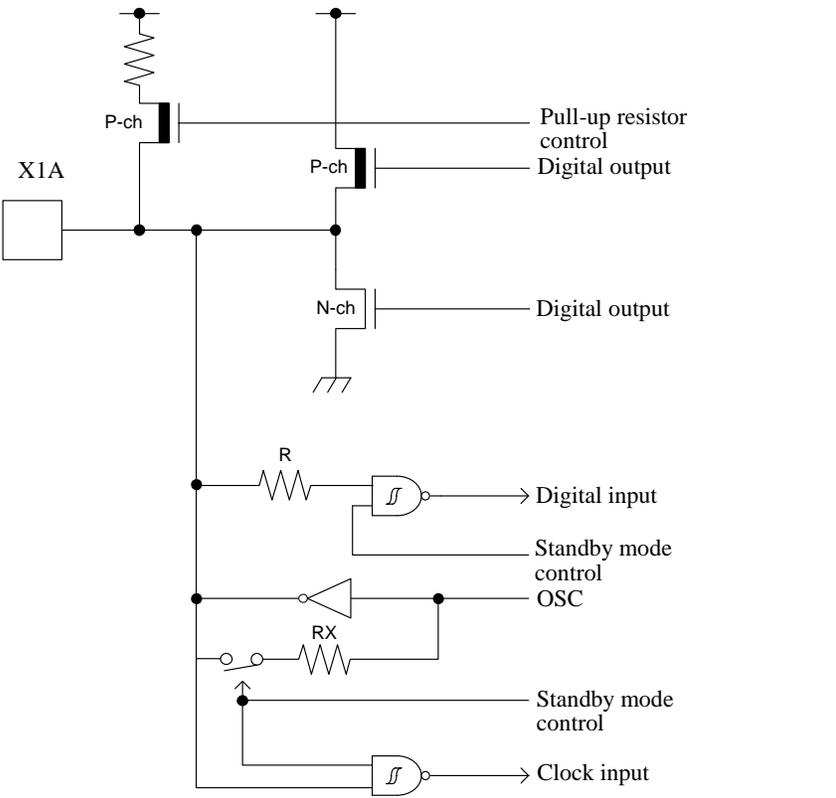
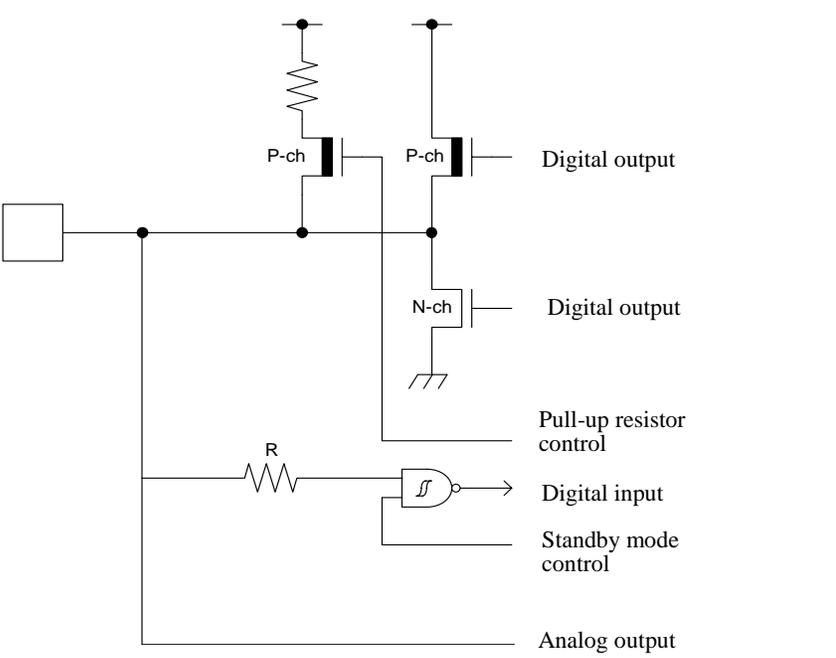
The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
ADC	ADTG_0	A/D converter external trigger input pin	9	5
	ADTG_1		27	-
	ADTG_2		35	26
	ADTG_3		43	34
	ADTG_4		57	-
	ADTG_5		59	43
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	36	27
	AN01		37	28
	AN02		38	29
	AN03		43	34
	AN04		44	35
	AN05		45	36
	AN06		46	-
	AN07		47	-
	AN08		48	-
	AN09		54	42
	AN10		55	-
	AN11		56	-
	AN12		57	-
	AN13		58	-
AN14	59	43		
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	2	-
	TIOA0_1		38	29
	TIOB0_0	Base timer ch.0 TIOB pin	3	-
	TIOB0_1		43	34
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	4	-
	TIOA1_1		44	35
	TIOB1_0	Base timer ch.1 TIOB pin	5	-
	TIOB1_1		45	36
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	6	2
	TIOA2_1		55	-
	TIOB2_0	Base timer ch.2 TIOB pin	7	3
	TIOB2_1		56	-
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	8	4
	TIOA3_1		57	-
	TIOB3_0	Base timer ch.3 TIOB pin	9	5
	TIOB3_1		58	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	10	6
	TIOA4_1		34	25
	TIOB4_0	Base timer ch.4 TIOB pin	11	7
	TIOB4_1		35	26
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	12	8
	TIOB5_0	Base timer ch.5 TIOB pin	13	9

Pin function	Pin name	Function description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	43	34
	SIN0_1		57	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	44	35
	SOT0_1 (SDA0_1)		56	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation modes 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4).	45	36
	SCK0_1 (SCL0_1)		55	-
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	48	-
	SIN1_1		58	-
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	47	-
	SOT1_1 (SDA1_1)		59	43
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	46	-
	SCK1_1 (SCL1_1)		60	44
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	10	6
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I <sup>2</sup> C (operation mode 4).	11	7
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I <sup>2</sup> C (operation mode 4).	12	8

Pin function	Pin name	Function description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	7	3
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	8	4
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	9	5
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	4	-
	SIN4_1		13	9
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I <sup>2</sup> C (operation mode 4).	5	-
	SOT4_1 (SDA4_1)		14	10
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I <sup>2</sup> C (operation mode 4).	6	-
	SCK4_1 (SCL4_1)		15	11
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	2	-
RTS4_0	Multi-function serial interface ch.4 RTS output pin	3	-	
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	38	29
	SOT6_0 (SDA6_0)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I <sup>2</sup> C (operation mode 4).	37	28
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I <sup>2</sup> C (operation mode 4).	36	27
	SCS6_0	Multi-function serial interface ch.6 serial chip select pin	35	26

Type	Circuit	Remarks
G	 <p>The diagram shows a pull-up resistor R connected to a node that branches into a P-ch transistor (Digital output) and an N-ch transistor (Digital output). A Digital input signal is connected to the node through an AND gate controlled by a Standby mode control signal. A Pull-up resistor control signal is also connected to the node.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>
H	 <p>The diagram shows a complex circuit with multiple inputs and outputs. Inputs include UDP/Pxx, Differential, and UDM/Pxx. Outputs include GPIO Digital output, GPIO Digital input/output direction, GPIO Digital input, GPIO Digital input circuit control, UDP output, USB Full-speed/Low-speed control, UDP input, Differential input, USB/GPIO select, UDM input, UDM output, USB Digital input/output direction, and GPIO Digital output. The circuit uses various logic gates and buffers.</p>	<p>It is possible to select the USB I/O / GPIO function.</p> <p>When the USB I/O is selected.</p> <ul style="list-style-type: none"> <li>• Full-speed, Low-speed control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby mode control</li> <li>• <math>I_{OH} = -20.5 \text{ mA}</math>, <math>I_{OL} = 18.5 \text{ mA}</math></li> </ul>

Type	Circuit	Remarks
Q	 <p>             X1A              Pull-up resistor control              Digital output (P-ch)              Digital output (N-ch)              Digital input (with R)              Standby mode control              OSC (with RX)              Standby mode control              Clock input           </p>	<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately 10 MΩ</li> <li>• With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• For I/O setting, refer to VBAT Domain in the Peripheral Manual</li> </ul>
R	 <p>             X1A              Digital output (P-ch)              Digital output (N-ch)              Pull-up resistor control              Digital input (with R)              Standby mode control              Analog output           </p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math> (4.5 V to 5.5 V)</li> <li>• <math>I_{OH} = -8 \text{ mA}</math>, <math>I_{OL} = 8 \text{ mA}</math> (2.7 V to 4.5 V)</li> </ul>

### Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 M $\Omega$ ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

#### 1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

#### 2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

#### 3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

#### 4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

#### 5. Smoke, Flame

**CAUTION:** Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 7. Handling Devices

### Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between VCC and VSS near this device.

### Power Supply Pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  at a momentary fluctuation such as switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.

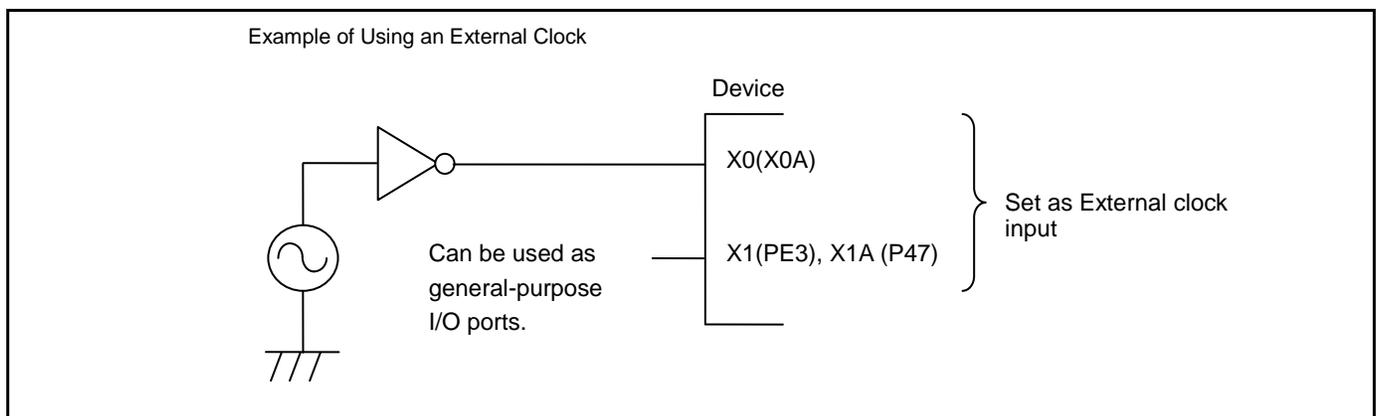
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size : More than 3.2 mm  $\times$  1.5 mm
  - Load capacitance : Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance : Approximately 6 pF to 7 pF

### Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1 (PE3) can be used as a general-purpose I/O port.

Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

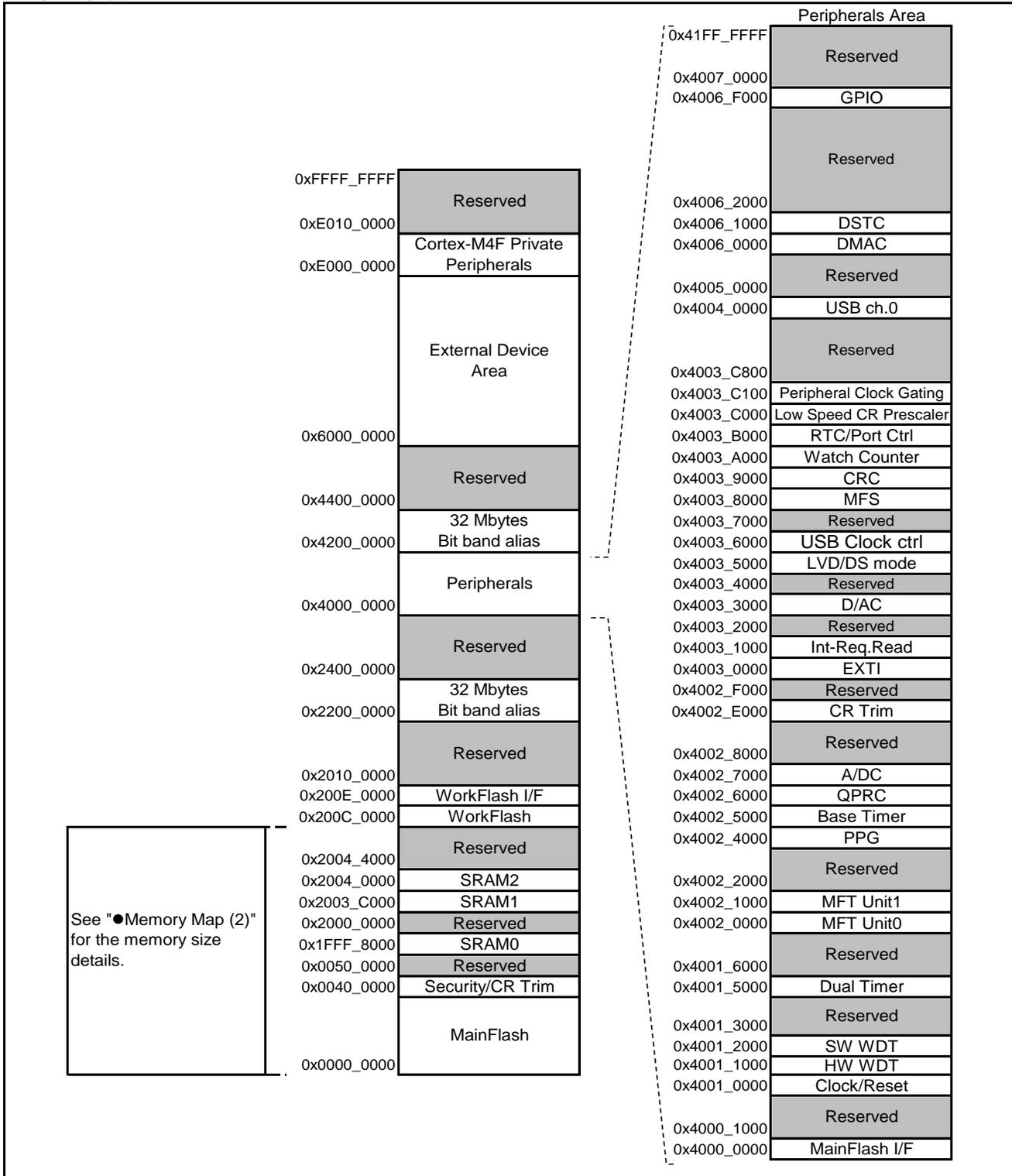


## 9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

## 10. Memory Map

### Memory Map (1)



Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z Input enabled	Hi-Z Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
GPIO selected										
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	GPIO selected									

**List of VBAT Domain Pin Status**

VBAT Pin Status Type	Function Group	VBAT Power-on Reset	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected	Setting prohibition	-
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal Input fixed at "0"	Hi-Z / Internal Input fixed at "0"	Maintain previous state	Maintain previous state/ When oscillation stops*, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*, Hi-Z/ Internal input fixed at "0"	Maintain previous state/ When oscillation stops*, Hi-Z/ Internal input fixed at "0"	Maintain previous state/ When oscillation stops*, Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

\*: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation (PLL)	160 MHz	28	58	mA	* <sup>3</sup> When all peripheral clocks are ON
				144 MHz	25	55		
				120 MHz	21	50		
				100 MHz	18	46		
				80 MHz	15	43		
				60 MHz	12	39		
				40 MHz	8.8	36		
				20 MHz	5.6	32		
				8 MHz	3.8	30		
				4 MHz	3.2	29		
				160 MHz	14	44	mA	* <sup>3</sup> When all peripheral clocks are OFF
				144 MHz	13	43		
				120 MHz	11	40		
				100 MHz	9.7	38		
				80 MHz	8.1	36		
				60 MHz	6.7	34		
				40 MHz	5.2	32		
				20 MHz	3.7	30		
8 MHz	2.9	29						
4 MHz	2.6	29						

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>5</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation (PLL)	72 MHz	19	47	mA	* <sup>3</sup> When all peripheral clocks are ON
				60 MHz	16	43		
				48 MHz	13	40		
				36 MHz	10	37		
				24 MHz	7.8	34		
				12 MHz	5.2	31		
				8 MHz	4.3	30		
				4 MHz	3.5	29		
				72 MHz	8.8	36		
				60 MHz	7.7	35		
				48 MHz	6.6	34		
				36 MHz	5.5	32		
				24 MHz	4.4	31		
				12 MHz	3.4	30		
				8 MHz	3	29		
				4 MHz	2.7	29		

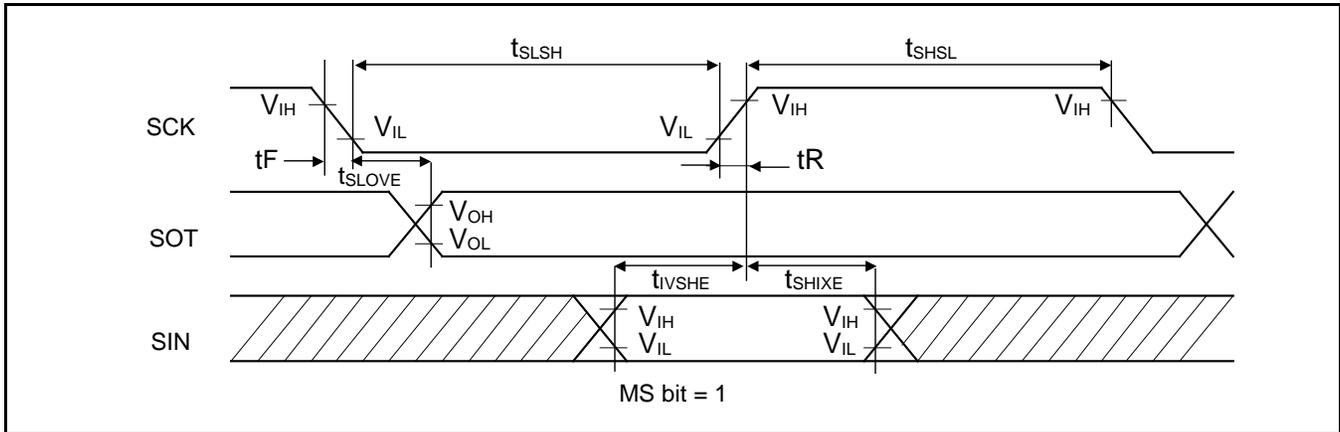
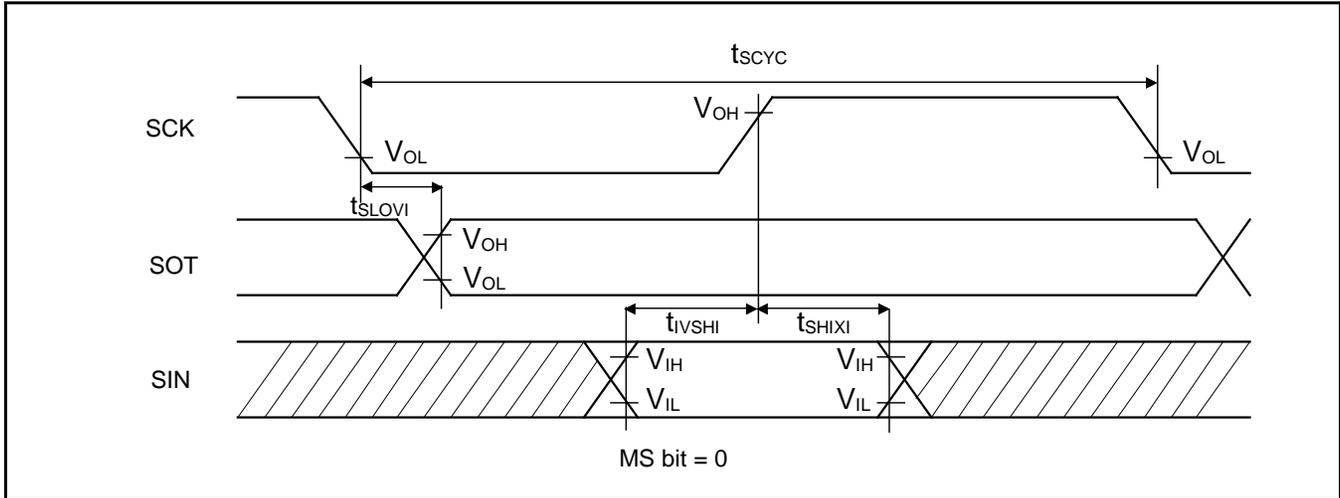
\*1: T<sub>A</sub>=+25 °C, V<sub>CC</sub>=3.3 V

\*2: T<sub>j</sub>=+125 °C, V<sub>CC</sub>=5.5 V

\*3: When all ports are fixed.

\*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

\*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK



**When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t <sub>CSDI</sub>		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-20+5t <sub>CYCP</sub>	(*3)+20+5t <sub>CYCP</sub>	(*3)-20+5t <sub>CYCP</sub>	(*3)+20+5t <sub>CYCP</sub>	ns
SCS↑→SCK↑setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCK↓→SCS↓ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	25	-	25	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**12.4.14 I<sup>2</sup>C Timing**
**Typical Mode, High-speed Mode**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	Typical Mode		High-speed Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F <sub>SCL</sub>	C <sub>L</sub> = 30 pF, R = (V <sub>p</sub> /I <sub>OL</sub> )* <sup>1</sup>	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	-	0.6	-	μs	
SCL clock "L" width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCL clock "H" width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>	2 MHz ≤ t <sub>CYCP</sub> < 40 MHz	2t <sub>CYCP</sub> * <sup>4</sup>	-	2t <sub>CYCP</sub> * <sup>4</sup>	-	ns	*5
		40 MHz ≤ t <sub>CYCP</sub> < 60 MHz	4t <sub>CYCP</sub> * <sup>4</sup>	-	4t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		60 MHz ≤ t <sub>CYCP</sub> < 80 MHz	6t <sub>CYCP</sub> * <sup>4</sup>	-	6t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		80 MHz ≤ t <sub>CYCP</sub> < 100 MHz	8t <sub>CYCP</sub> * <sup>4</sup>	-	8t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		100 MHz ≤ t <sub>CYCP</sub> < 120 MHz	10t <sub>CYCP</sub> * <sup>4</sup>	-	10t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		120 MHz ≤ t <sub>CYCP</sub> < 140 MHz	12t <sub>CYCP</sub> * <sup>4</sup>	-	12t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		140 MHz ≤ t <sub>CYCP</sub> < 160 MHz	14t <sub>CYCP</sub> * <sup>4</sup>	-	14t <sub>CYCP</sub> * <sup>4</sup>	-	ns	
		160 MHz ≤ t <sub>CYCP</sub> < 180 MHz	16t <sub>CYCP</sub> * <sup>4</sup>	-	16t <sub>CYCP</sub> * <sup>4</sup>	-	ns	

\*1: R and C<sub>L</sub> represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

\*2: The maximum t<sub>HDDAT</sub> must satisfy that it does not extend at least "L" period (t<sub>LOW</sub>) of device's SCL signal.

\*3: A high-speed mode I<sup>2</sup>C bus device can be used on a typical mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of t<sub>SUDAT</sub> ≥ 250 ns.

\*4: t<sub>CYCP</sub> is the APB bus clock cycle time.

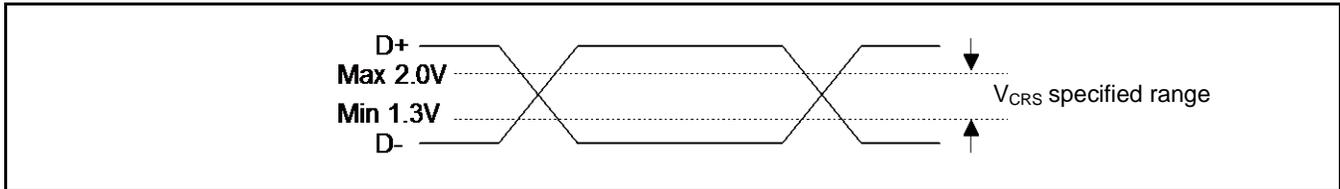
About the APB bus number that I<sup>2</sup>C is connected to, see "8. Block Diagram" in this data sheet.

\*5: The noise filter time can be changed by register settings.

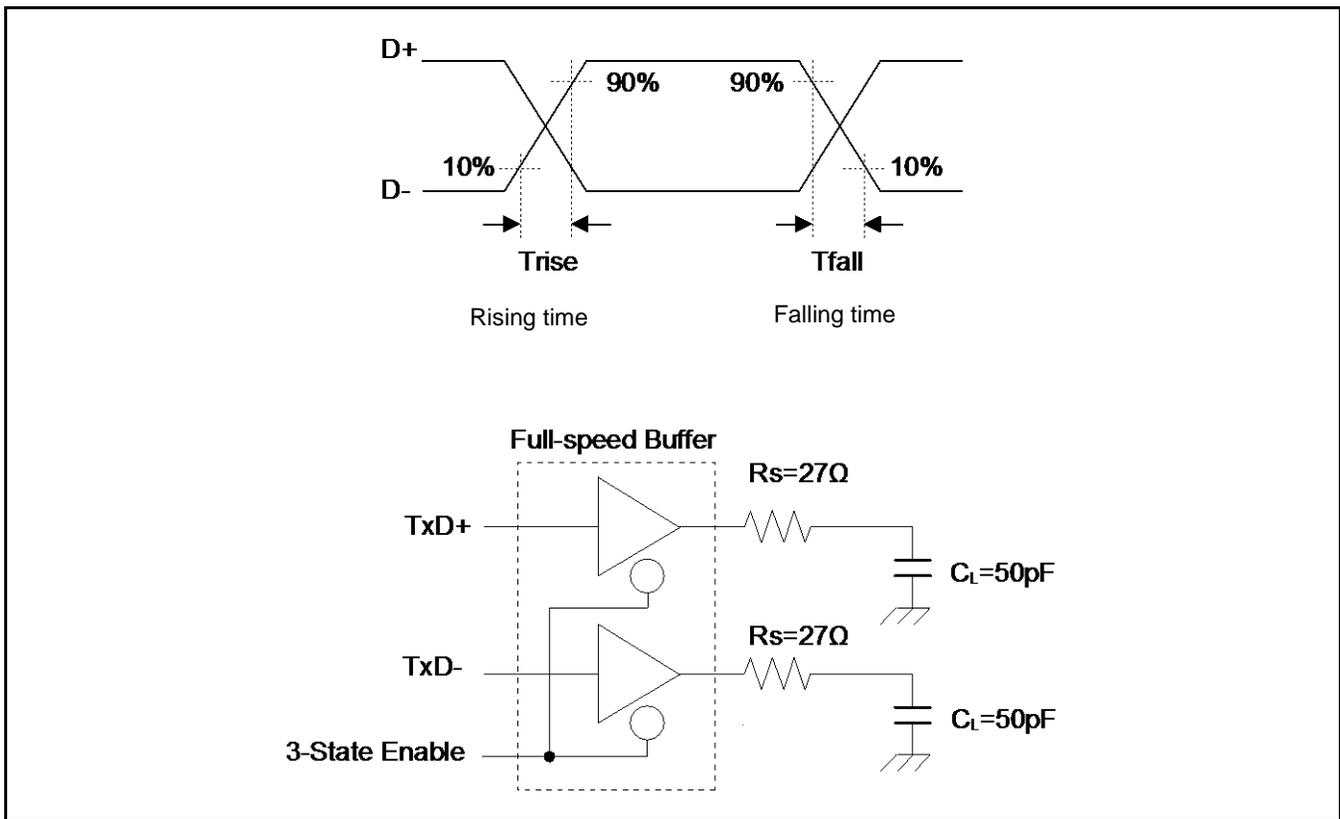
Change the number of the noise filter steps according to APB bus clock frequency.

\*3: The output drive capability of the driver is below 0.3 V at Low-State ( $V_{OL}$ ) (to 3.6 V and 1.5 k $\Omega$  load), and 2.8 V or above (to the  $V_{SS}$  and 1.5 k $\Omega$  load) at High-State ( $V_{OH}$ ).

\*4: The cross voltage of the external differential output signal (D + /D -) of USB I/O buffer is within 1.3 V to 2.0 V.



\*5: They indicate rising time ( $T_{rise}$ ) and falling time ( $T_{fall}$ ) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer,  $T_r/T_f$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.



Page	Section	Change Results
116	■ ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (1) Recovery cause: Interrupt/WKUP	<ul style="list-style-type: none"> <li>• Revised the value of TBD</li> <li>• Revised the table of Recovery count time</li> </ul>
118	■ ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (2) Recovery cause: Reset	<ul style="list-style-type: none"> <li>• Revised the value of TBD</li> <li>• Revised the table of Recovery count time</li> </ul>

**NOTE: Please see “Document History” about later revised information.**