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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451ccu3

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3.4 Embedded Flash memory

STM32L451xx devices feature up to 512 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

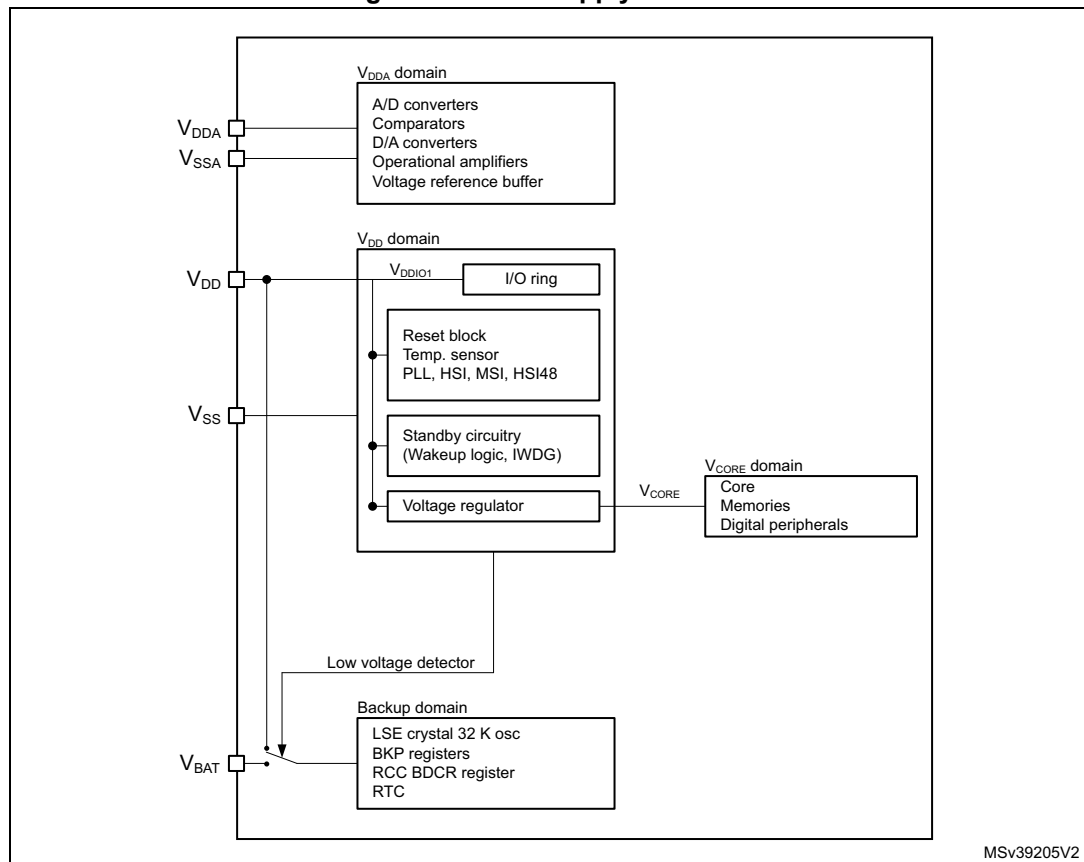
Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽¹⁾	No	No	N/A ⁽¹⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes ⁽¹⁾	No	No	No ⁽¹⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

Figure 2. Power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below $V_{DD} + 300$ mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

- **Shutdown mode**

The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

The system clock after wakeup is MSI at 4 MHz.

Table 5. Functionalities depending on the working mode⁽¹⁾ (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9) 5 pins (10)	(11) 5 pins (10)	-	-	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.23.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
 - Internal clock sources: LSE, LSI, HSI16 or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.23.5 Infrared interface (IRTIM)

The STM32L451xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM15 and TIM16 output channels to generate output signal waveforms on IR_OUT pin.

3.23.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.23.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

Table 14. SAI implementation

SAI features	Support ⁽¹⁾
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/Mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO Size	X (8 Word)
SPDIF	X

1. X: supported

3.30 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s
- Transmission
 - Three transmit mailboxes
 - Configurable transmit priority
- Reception
 - Two receive FIFOs with three stages
 - 14 Scalable filter banks
 - Identifier list feature
 - Configurable FIFO overrun
- Time-triggered communication option
 - Disable automatic retransmission mode
 - 16-bit free running timer
 - Time Stamp sent in last two data bytes
- Management
 - Maskable interrupts
 - Software-efficient mailbox mapping at a unique address space

3.31 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

3.34 Development support

3.34.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.34.2 Embedded Trace Macrocell™

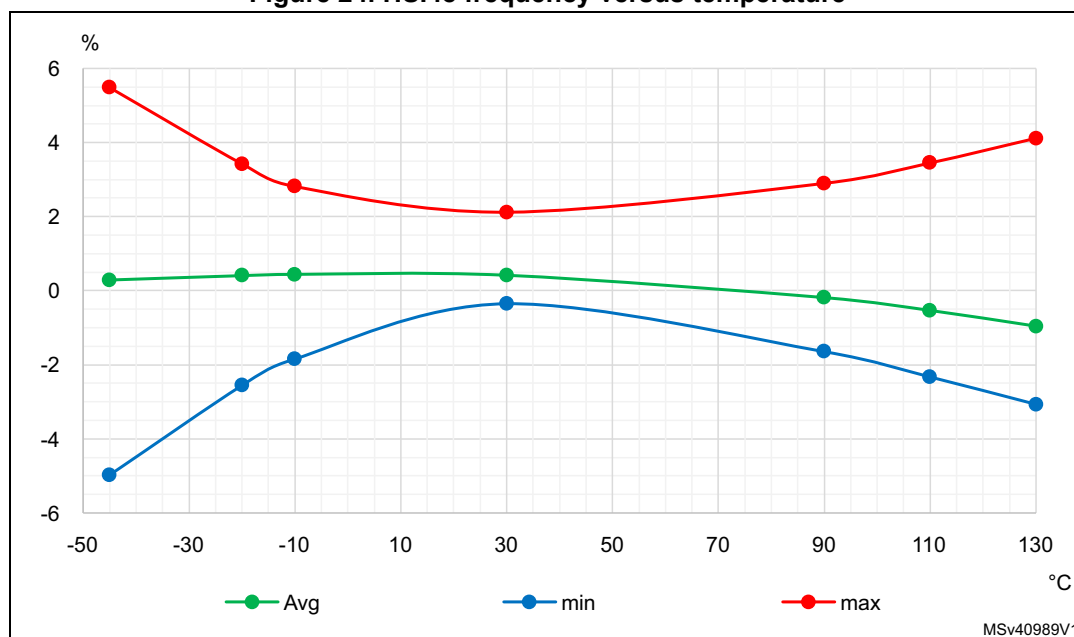
The Arm® Embedded Trace Macrocell™ provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L451xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell™ operates with third party debugger software tools.

Table 18. Alternate function AF8 to AF15⁽¹⁾ (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_ BK1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS _DE	-	QUADSPI_ BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	-	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PB5	-	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	CAN1_TX	TSC_G2_IO3	-	-	-	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	-	-	-	-	EVENTOUT
	PB8	-	CAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	-	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_ BK1_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS _DE	TSC_G1_IO1	CAN1_RX	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	CAN1_TX	-	-	SAI1_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI1_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	-	SAI1_SD_A	TIM15_CH2	EVENTOUT

Figure 24. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 52. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	$V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{A}} = 30 \text{ }^{\circ}\text{C}$	31.04	-	32.96	kHz
		$V_{\text{DD}} = 1.62 \text{ to } 3.6 \text{ V}$, $T_{\text{A}} = -40 \text{ to } 125 \text{ }^{\circ}\text{C}$	29.5	-	34	
$t_{\text{SU}}(\text{LSI})^{(2)}$	LSI oscillator start-up time	-	-	80	130	μs
$t_{\text{STAB}}(\text{LSI})^{(2)}$	LSI oscillator stabilization time	5% of final frequency	-	125	180	μs
$I_{\text{DD}}(\text{LSI})^{(2)}$	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.

2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in [Table 53](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 23: General operating conditions](#).

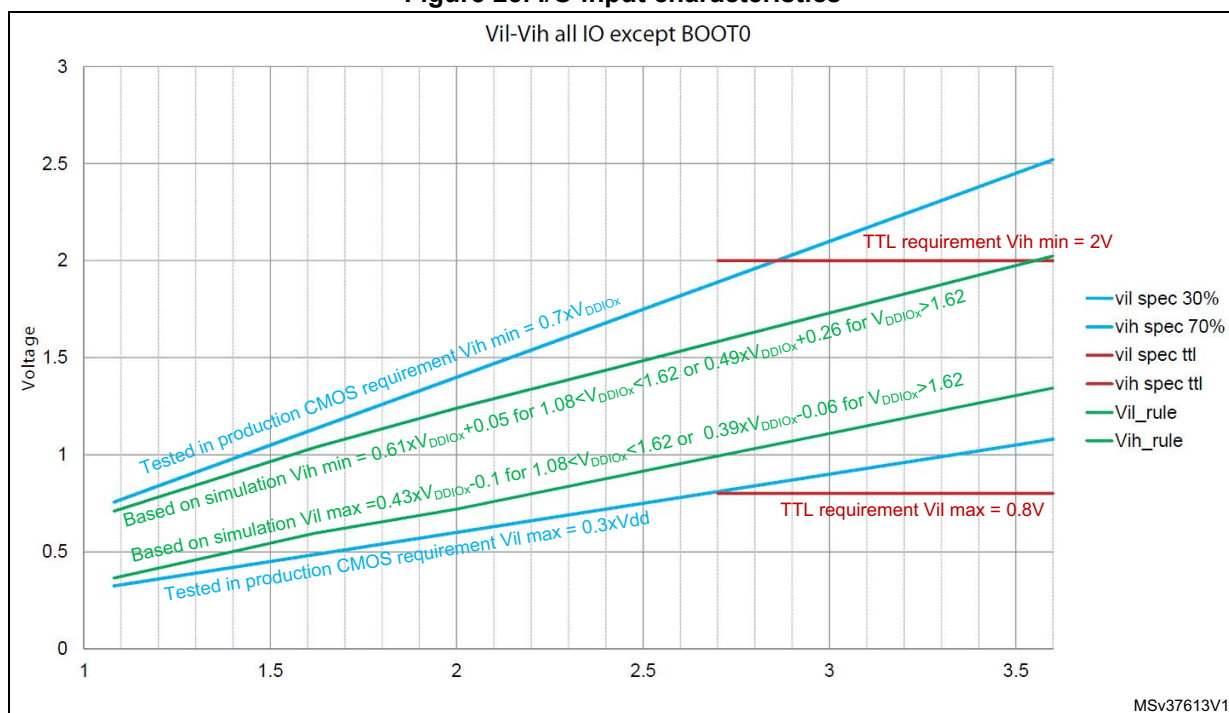
Table 53. PLL, PLLSAI1 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{PLL_IN}}$	PLL input clock ⁽²⁾	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%

1. Refer to [Figure 25: I/O input characteristics](#).
2. Tested in production.
3. Guaranteed by design.
4. All FT_xx IO except PA11, PA12 and PC3 I/O.
5. $\text{Max}(V_{DDXX})$ is the maximum value of all the I/O supplies.
6. To sustain a voltage higher than $\text{Min}(V_{DD}, V_{DDA}) + 0.3 \text{ V}$, the internal Pull-up and Pull-Down resistors must be disabled.
7. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:
 $I_{\text{Total_leak_max}} = 10 \mu\text{A} + [\text{number of IOs where } V_{IN} \text{ is applied on the pad}] \times I_{\text{IKG}}(\text{Max})$.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 25](#) for standard I/Os, and in [Figure 25](#) for 5 V tolerant I/Os.

Figure 25. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to $\pm 8 \text{ mA}$, and sink or source up to $\pm 20 \text{ mA}$ (with a relaxed V_{OL}/V_{OH}).

6.3.20 Voltage reference buffer characteristics

Table 75. VREFBUF characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046 ⁽³⁾	2.048	2.049 ⁽³⁾	
			$V_{RS} = 1$	2.498 ⁽³⁾	2.5	2.502 ⁽³⁾	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
			$V_{RS} = 1$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	± 0.05	± 0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	μF
esr	Equivalent Serial Resistor of Cloud	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	$2.8 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	$I_{load} = 500 \mu\text{A}$	-	200	1000	ppm/V
			$I_{load} = 4 \text{ mA}$	-	100	500	
I_{load_reg}	Load regulation	$500 \mu\text{A} \leq I_{load} \leq 4 \text{ mA}$	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	$-40^\circ\text{C} < T_J < +125^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	ppm/ $^\circ\text{C}$
		$0^\circ\text{C} < T_J < +50^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	$CL = 0.5 \mu\text{F}^{(4)}$		-	300	350	μs
		$CL = 1.1 \mu\text{F}^{(4)}$		-	500	650	
		$CL = 1.5 \mu\text{F}^{(4)}$		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase ⁽⁵⁾	-	-	-	8	-	mA

6.3.24 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	k Ω
Q	Ratio on V_{BAT} measurement	-	3	-	-
$Er^{(1)}$	Error on Q	-10	-	10	%
$t_{S_vbat}^{(1)}$	ADC sampling time when reading the VBAT	12	-	-	μ s

1. Guaranteed by design.

Table 80. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	k Ω
		VBRS = 1	-	1.5	-	

6.3.25 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 81. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80$ MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 80$ MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80$ MHz	0.0125	819.2	μ s
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80$ MHz	-	53.68	s

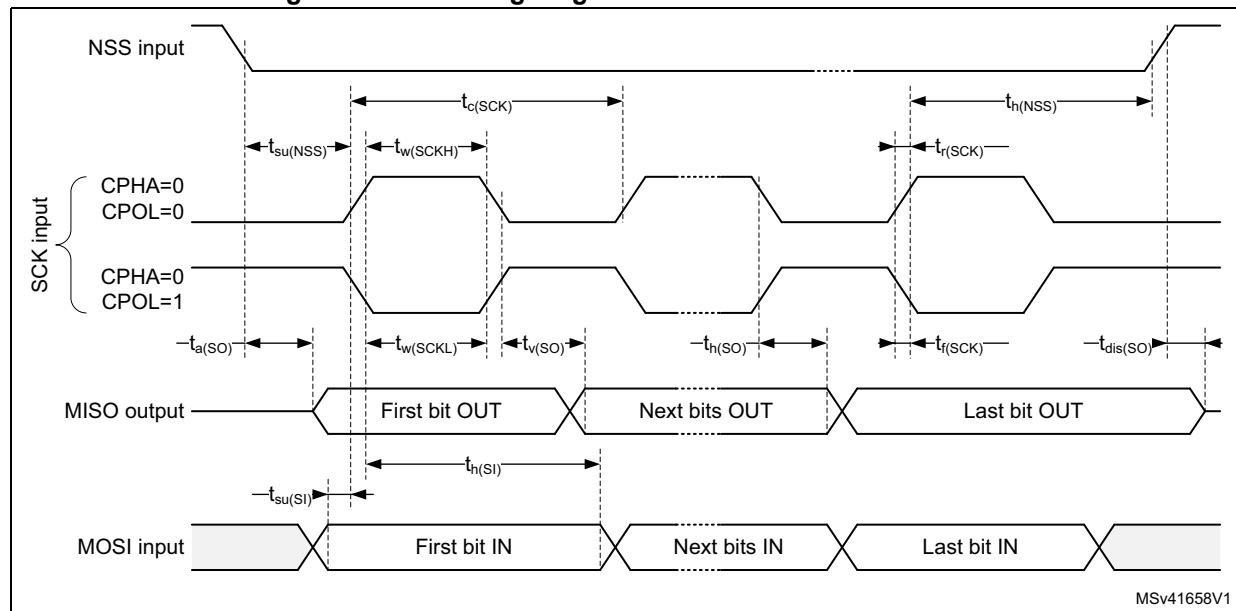
1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 85. SPI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	13.5	ns
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	24	
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50 %.

Figure 31. SPI timing diagram - slave mode and CPHA = 0



MSv41658V1

Table 88. SAI characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{V(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Slave transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	34	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{V(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	27	ns
		Master transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 36. SAI master timing waveforms

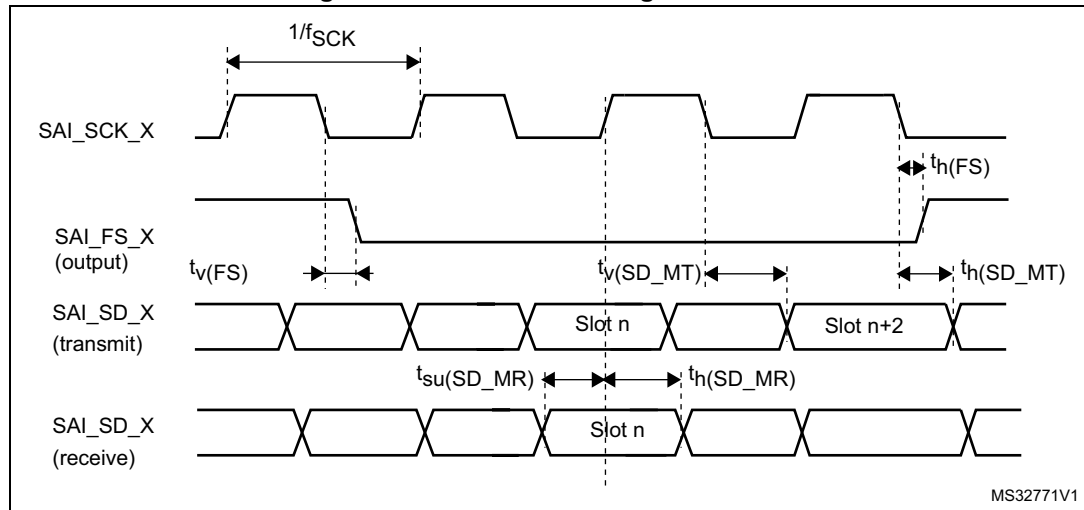
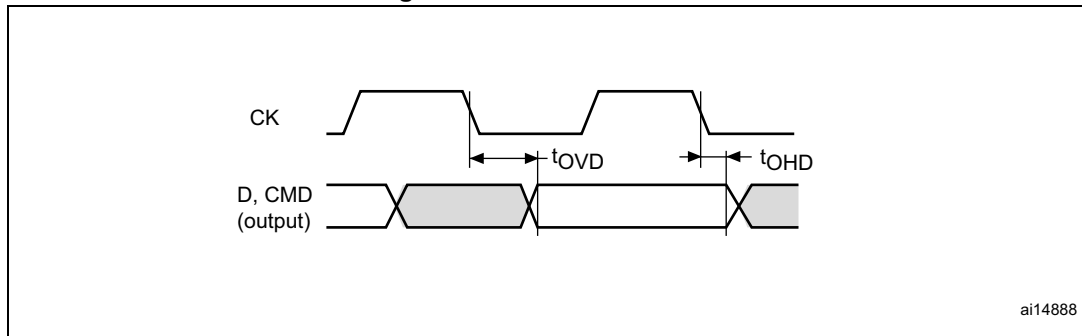


Figure 39. SD default mode



CAN (controller area network) interface

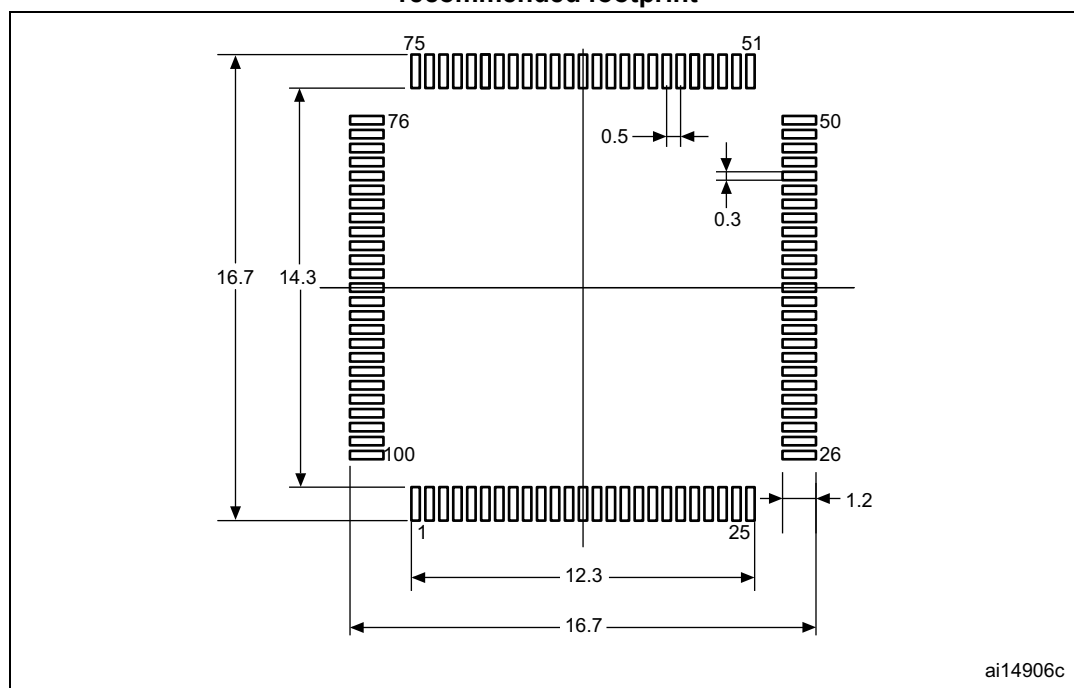
Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Table 91. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

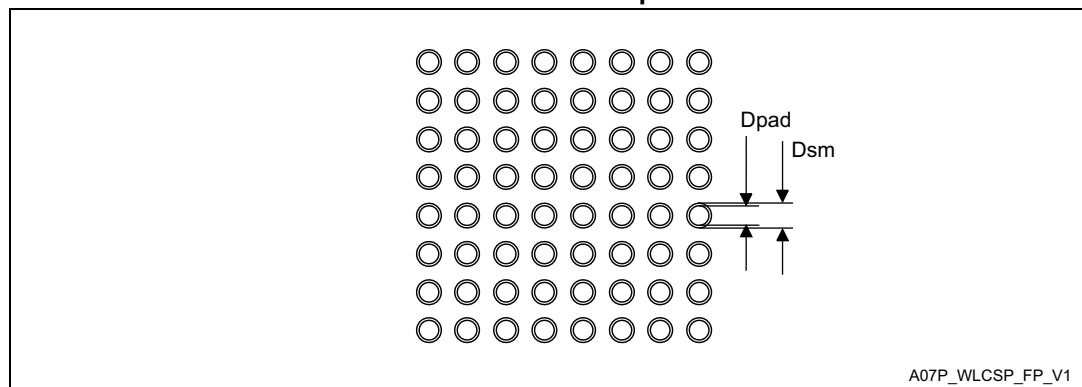


1. Dimensions are expressed in millimeters.

Table 97. WLCSP64 - 64-ball, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.322	3.357	3.392	0.1308	0.1322	0.1335
E	3.622	3.657	3.692	0.1426	0.1440	0.1454
e	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
e2	-	2.800	-	-	0.1102	-
F	-	0.278	-	-	0.0109	-
G	-	0.428	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. WLCSP64 - 64-pin, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale recommended footprint

1. Dimensions are expressed in millimeters.

8 Ordering information

Table 101. STM32L451xx ordering information scheme

Example:	STM32	L	451	C	C	T	6	TR								
Device family																
STM32 = Arm [®] based 32-bit microcontroller																
Product type																
L = ultra-low-power																
Device subfamily																
451: STM32L451xx																
Pin count																
C = 48 pins																
R = 64 pins																
V = 100 pins																
Flash memory size																
C = 256 KB of Flash memory																
E = 512 KB of Flash memory																
Package																
T = LQFP ECOPACK [®] 2																
U = QFN ECOPACK [®] 2																
I = UFBGA ECOPACK [®] 2																
Y = CSP ECOPACK [®] 2																
Temperature range																
6 = Industrial temperature range, -40 to 85 °C (105 °C junction)																
3 = Industrial temperature range, -40 to 125 °C (130 °C junction)																
Packing																
TR = tape and reel																
xxx = programmed parts																

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.