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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451ccu3tr

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2 Description

The STM32L451xx devices are the ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L451xx devices embed high-speed memories (Flash memory up to 512 Kbyte, 160 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L451xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, one DAC channel, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, one UART and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN

The STM32L451xx operates in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators. A VBAT input allows to backup the RTC and backup registers.

The STM32L451xx family offers six packages from 48 to 100-pin packages.

Table 5. Functionalities depending on the working mode[(1)] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

Figure 4. Clock tree

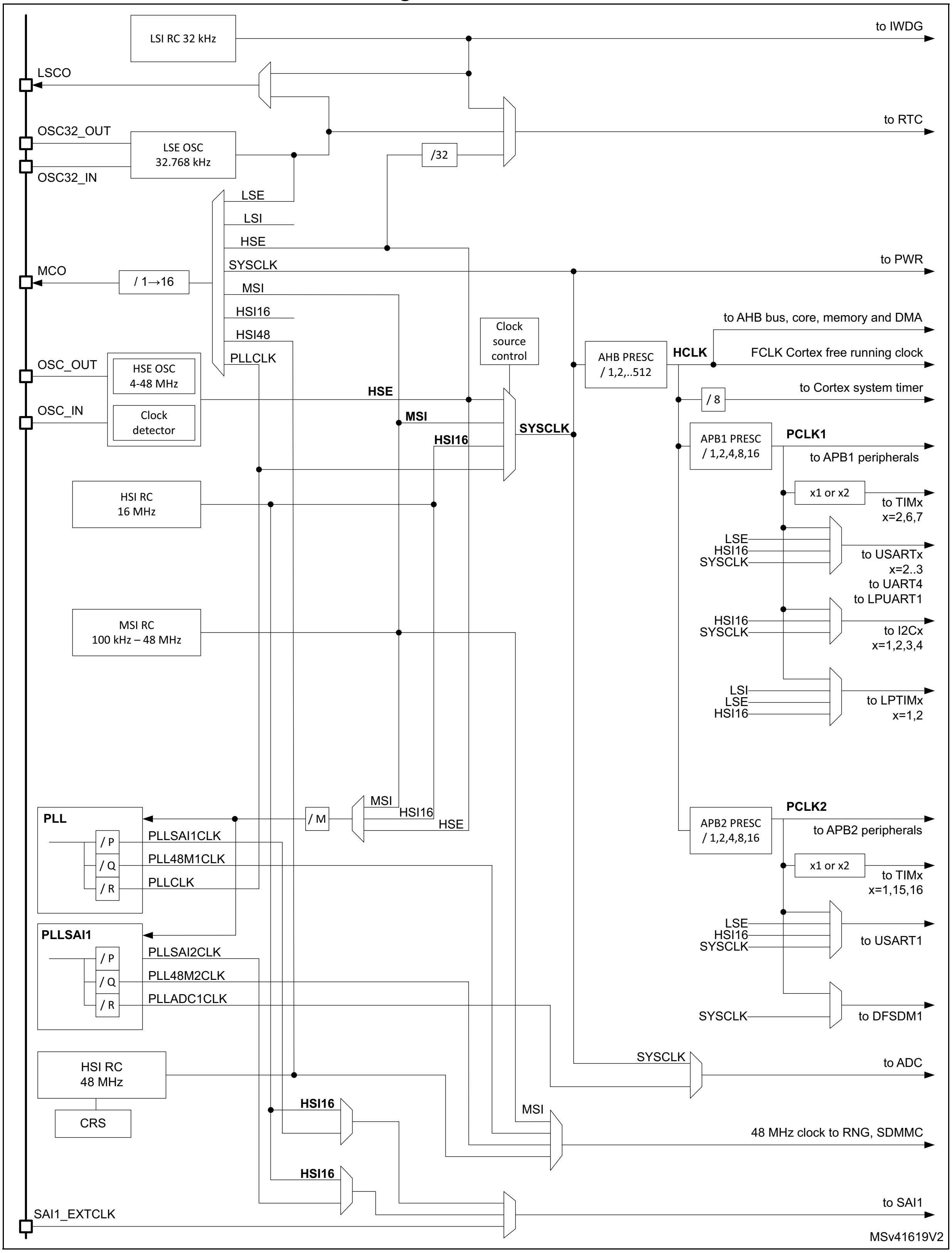


Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.15.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18 or ADC3_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.16 Digital to analog converter (DAC)

One 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

3.28 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.29 Serial audio interfaces (SAI)

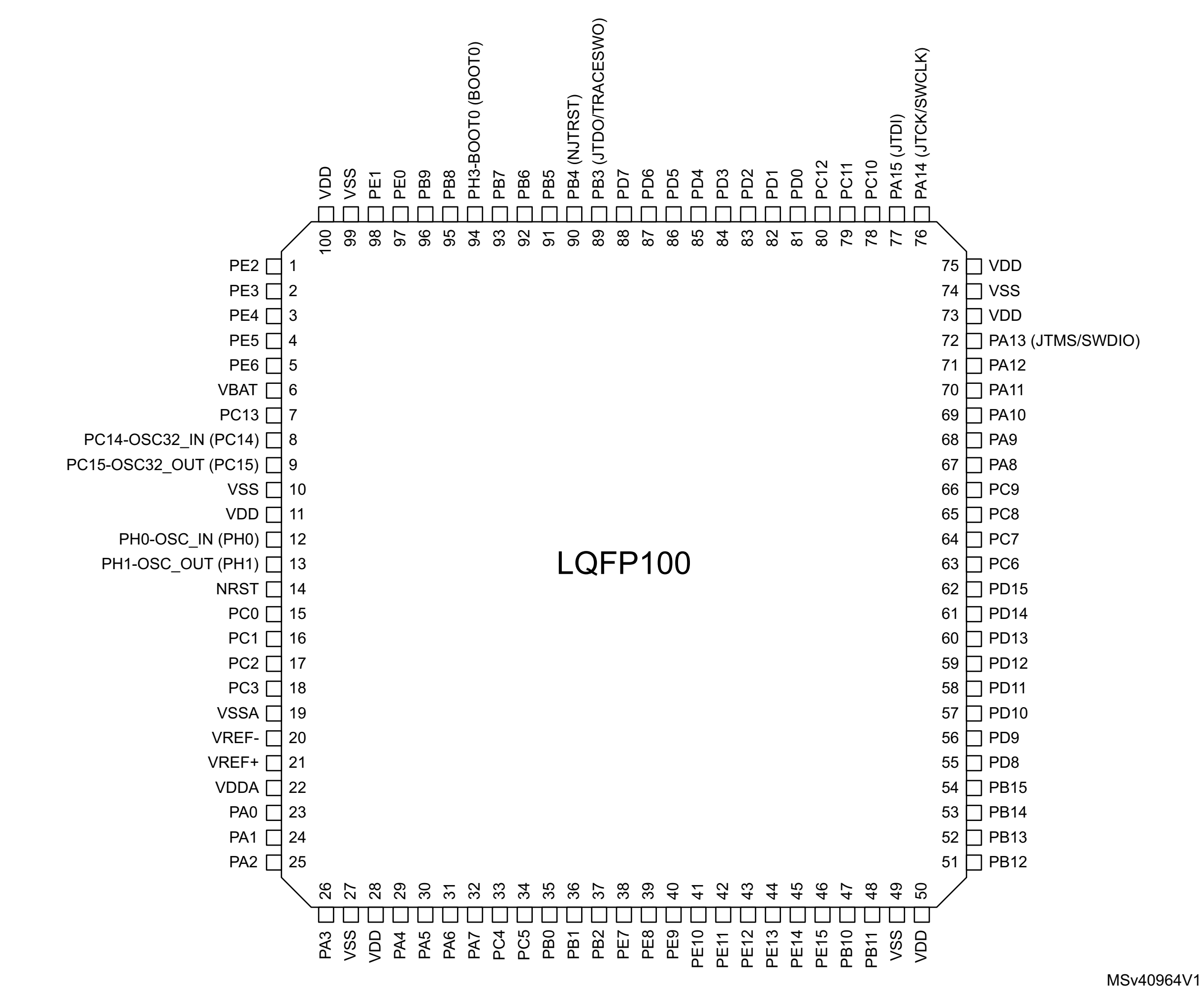
The device embeds 1 SAI. Refer to *Table 14: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

4 Pinouts and pin description

Figure 6. STM32L451Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 21. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	140	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(4)	
	Injected current on PA4, PA5	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 35. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See [3].	3 V	1.85	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See [3].	3 V	1.50	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See [3].	3 V	1.55	-	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 42: Low-power mode wakeup timings*.

Table 37. Current consumption in Stop 0

Symbol	Parameter	Conditions	TYP					MAX[1]					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	125	150	240	390	645	145	190	350	600	1150	µA
		2.4 V	125	150	240	390	645	150	195	355	605	1150	
		3 V	125	150	245	395	650	155	195	360	610	1150	
		3.6 V	125	155	245	400	655	155	200	365	615	1150[2]	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 41*. The MCU is placed under the following conditions:

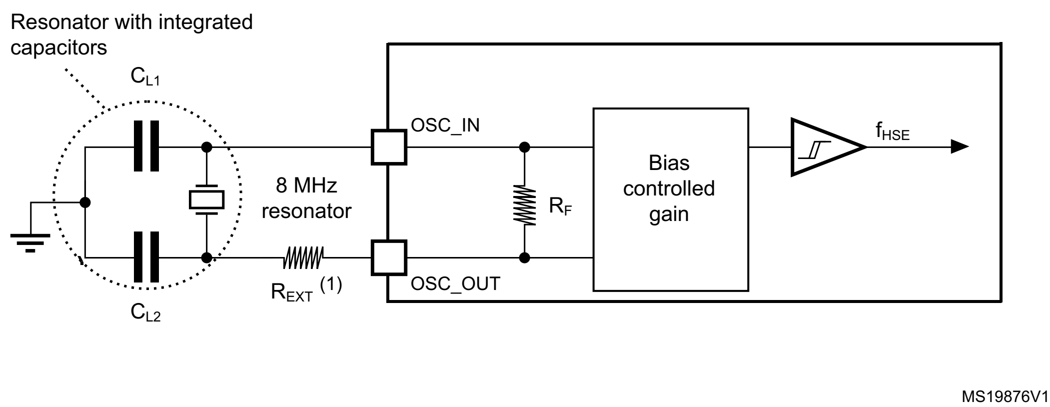
- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 20: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 41*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 41. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	3.2	2.9	3.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA(2)	1.7	1.4	1.6	
	GPIOB(2))	1.6	1.3	1.6	
	GPIOC(2)	1.7	1.5	1.6	
	GPIOD(2)	1.8	1.6	1.7	
	GPIOE(2)	1.7	1.6	1.6	
	GPIOH(2)	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	N/A	N/A	
	RNG clock domain	0.5	N/A	N/A	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge(3)	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	
	DAC1	2.4	1.8	2.2	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 48*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 48. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when $V_{DDA} \geq 2.4$ V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 73. DAC characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC1_OUT1 for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001	CL ≤ 50 pF, RL ≥ 5 kΩ		1	-	-	µs
	DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 10 pF		1.4			
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DAC1_OUT1 reaches final value ±1LSB)	DAC1_OUT1 pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC1_OUT1 pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC1_OUT1 pin connected		-	-	-[3]	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA}(DAC)$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) [4]	670 x Ton/(Ton +Toff) [4]	

Figure 34. Quad SPI timing diagram - SDR mode

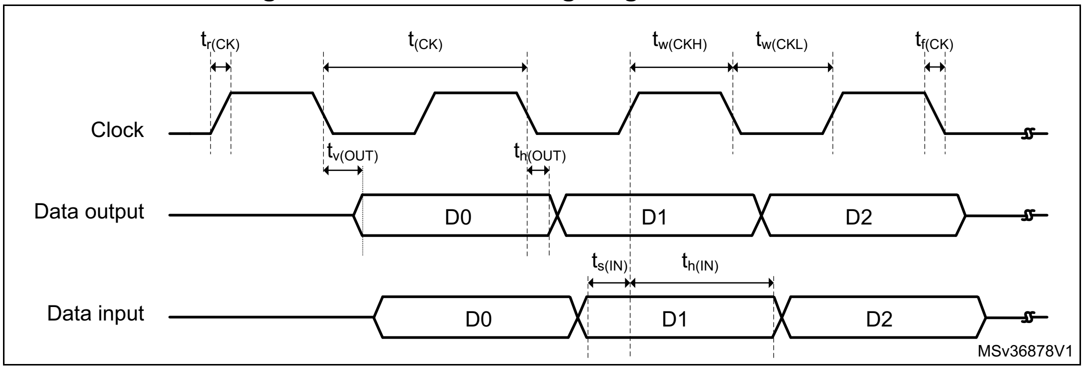


Figure 35. Quad SPI timing diagram - DDR mode

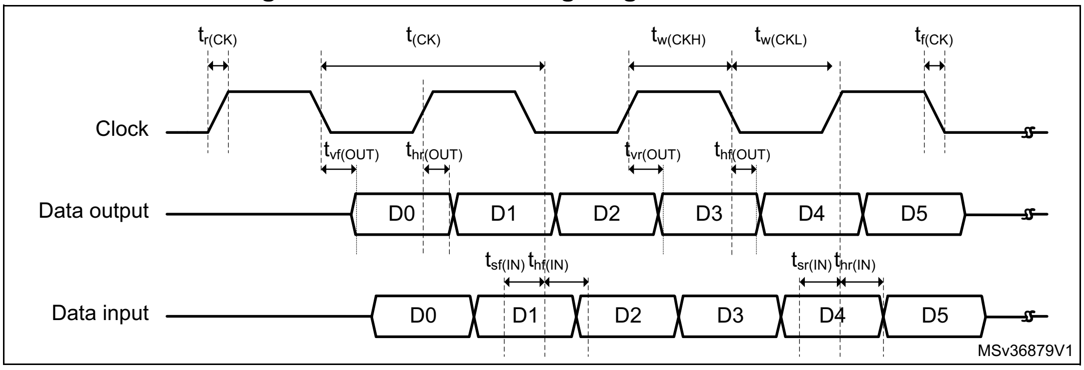
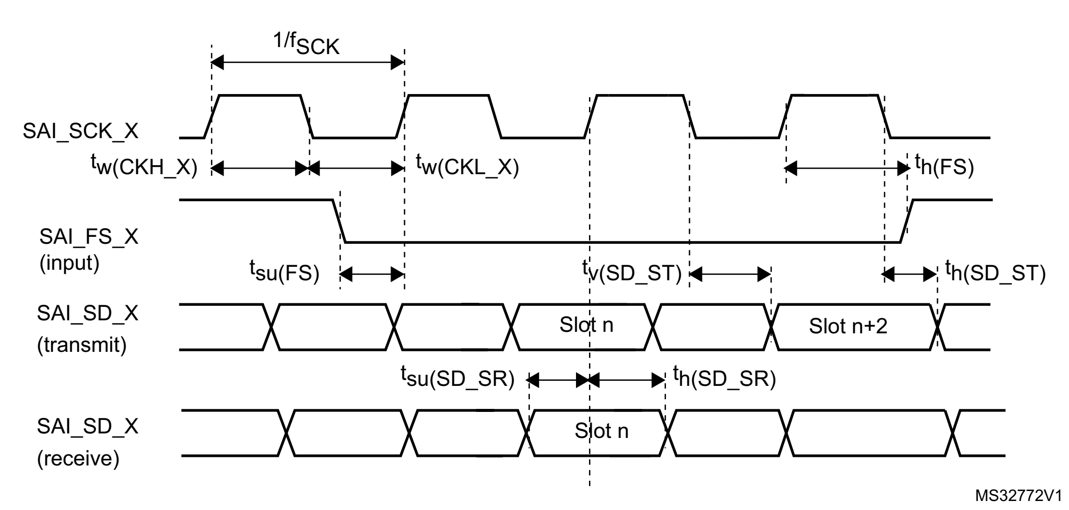


Figure 37. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 89* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

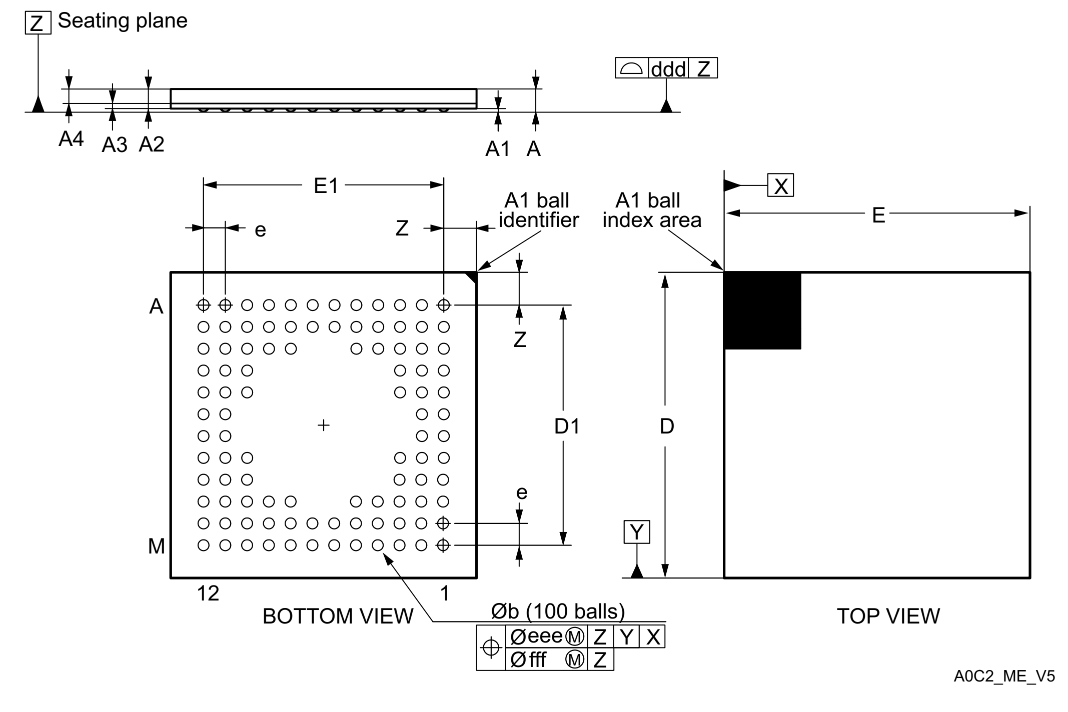
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 89. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	10	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	3	-	-	ns

7.2 UFBGA100 package information

Figure 43. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 92. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 75 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

T_{Jmax} = 75 °C + (58 °C/W × 447 mW) = 75 °C + 25.926 °C = 100.926 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 3).

Suffix 6: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 105-25.926 = 79.074 °C

Suffix 3: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 130-25.926 = 104.074 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

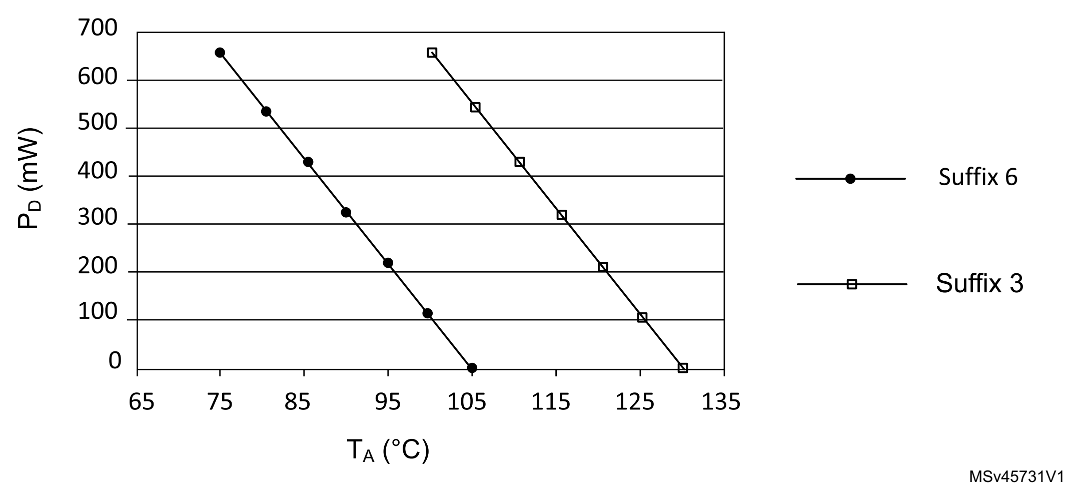
T_{Jmax} = 100 °C + (58 °C/W × 134 mW) = 100 °C + 7.772 °C = 107.772 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 58* to select the required temperature range (suffix 6 or 3) according to your ambient temperature or power requirements.

Figure 58. LQFP64 P_D max vs. T_A



8 Ordering information

Table 101. STM32L451xx ordering information scheme

Example: STM32 L 451 C C T 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

451: STM32L451xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

C = 256 KB of Flash memory

E = 512 KB of Flash memory

Package

T = LQFP ECOPACK®2

U = QFN ECOPACK®2

I = UFBGA ECOPACK®2

Y = CSP ECOPACK®2

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.