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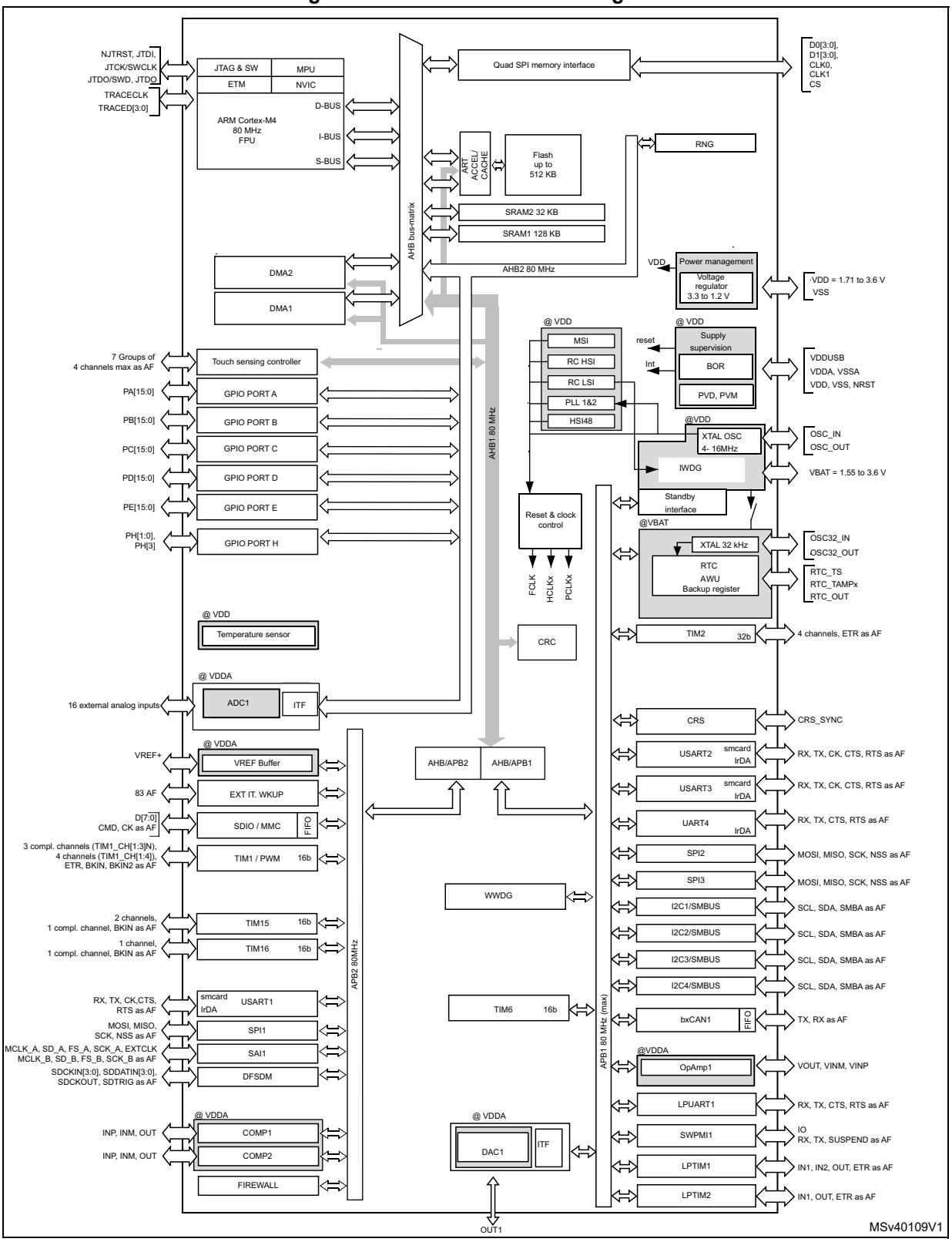
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451ccu6

Figure 1. STM32L451xx block diagram



Note: AF: alternate function on I/O pins.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI or CAN.

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDA} = 1.62 V (ADC/COMPs) / 1.8 (DAC/OPAMP) / 2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, DAC, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with V_{DDIO1} = V_{DD}.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.32 Clock recovery system (CRS)

The STM32L451xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

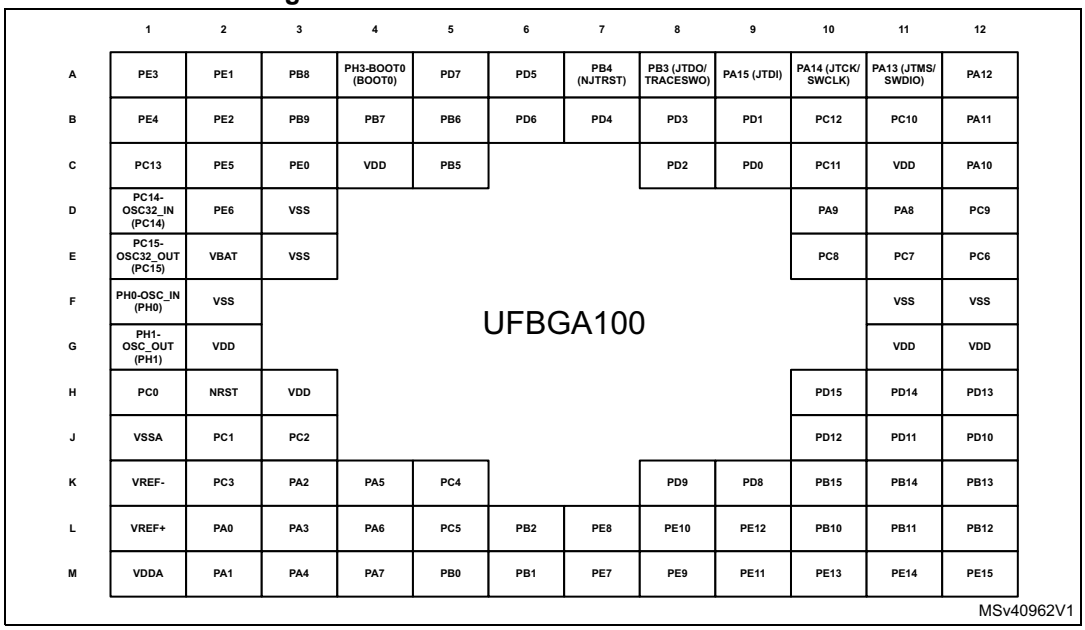
3.33 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

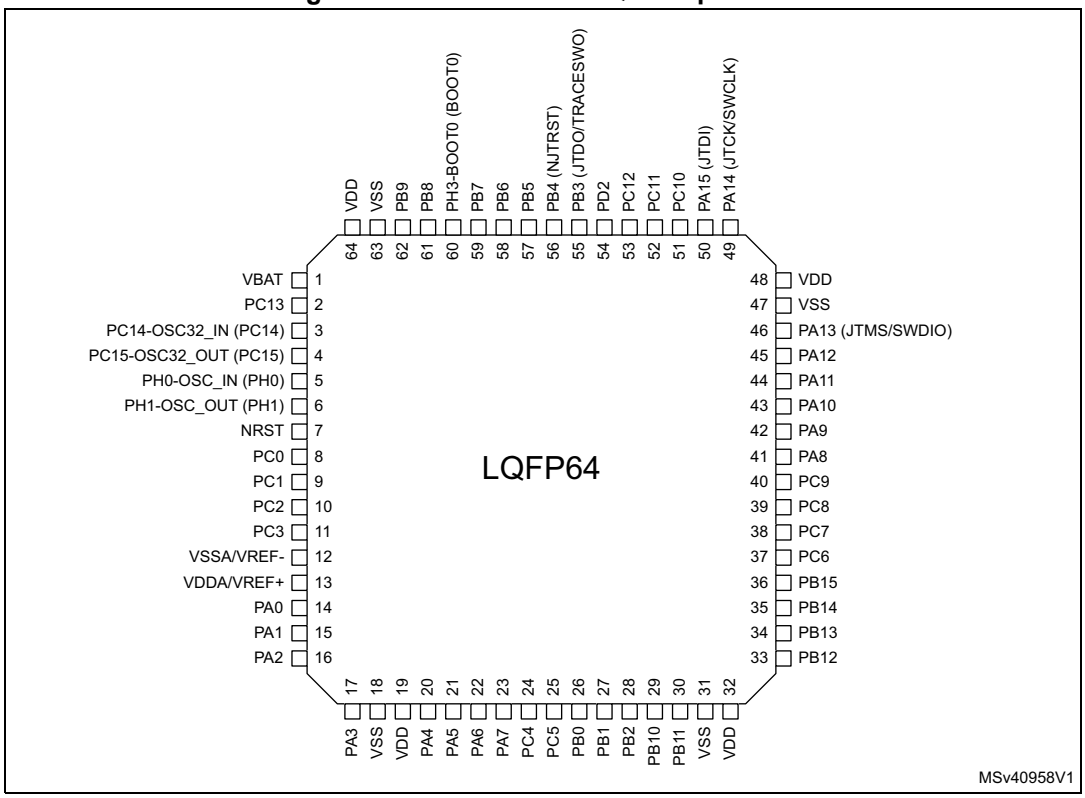
Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

Figure 7. STM32L451Vx UFBGA100 ballout(1)



1. The above figure shows the package top view.

Figure 8. STM32L451Rx LQFP64 pinout(1)



1. The above figure shows the package top view.

Table 16. STM32L451xx pin definitions

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	1	B2	PE2	I/O	FT	-	TRACECK, TIM3_ETR, TSC_G7_IO1, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	2	A1	PE3	I/O	FT	-	TRACED0, TIM3_CH1, TSC_G7_IO2, SAI1_SD_B, EVENTOUT	-
-	-	-	-	3	B1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM1_DATIN3, TSC_G7_IO3, SAI1_FS_A, EVENTOUT	-
-	-	-	-	4	C2	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	5	D2	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_SD_A, EVENTOUT	RTC_TAMP3, WKUP3
1	B7	1	B2	6	E2	VBAT	S	-	-	-	-
2	B8	2	A2	7	C1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	C8	3	A1	8	D1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	C7	4	B1	9	E1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	10	F2	VSS	S	-	-	-	-
-	-	-	-	11	G2	VDD	S	-	-	-	-
5	D8	5	C1	12	F1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	E8	6	D1	13	G1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	F8	7	E1	14	H2	NRST	I/O	RST	-	-	-
-	D7	8	E3	15	H1	PC0	I/O	FT_fa	-	LPTIM1_IN1, I2C4_SCL, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, EVENTOUT	ADC1_IN1

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	D5	9	E2	16	J2	PC1	I/O	FT_fa	-	TRACED0, LPTIM1_OUT, I2C4_SDA, I2C3_SDA, LPUART1_TX, EVENTOUT	ADC1_IN2
-	D6	10	F2	17	J3	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, EVENTOUT	ADC1_IN3
-	E7	11	G1	18	K2	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	-	19	J1	VSSA	S	-	-	-	-
-	-	-	-	20	K1	VREF-	S	-	-	-	-
8	G8	12	F1	-	-	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	22	M1	VDDA	S	-	-	-	-
9	F7	13	H1	-	-	VDDA/ VREF+	S	-	-	-	-
10	H8	14	G2	23	L2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, UART4_TX, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM, ADC1_IN5, RTC_TAMP2, WKUP1
11	E6	15	H2	24	M2	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP, ADC1_IN6
12	G7	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4,LSCO
13	F6	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	18	C2	27	E3	VSS	S	-	-	-	-
-	H7	19	D2	28	H3	VDD	S	-	-	-	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, SAI1_FS_B, EVENTOUT	-
-	-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, EVENTOUT	-
21	H4	29	G7	47	L10	PB10	I/O	FT_f	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
22	H3	30	H7	48	L11	PB11	I/O	FT_f	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, EVENTOUT	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	74	F11	VSS	S	-	-	-	-
-	B2	-	-	75	G11	VDD	S	-	-	-	-
37	C3	49	A7	76	A10	PA14 (JTCK/ SWCLK)	I/O	FT	(3)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, SAI1_FS_B, EVENTOUT	-
38	A2	50	A6	77	A9	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, EVENTOUT	-
-	D4	51	B7	78	B11	PC10	I/O	FT	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, EVENTOUT	-
-	B3	52	B6	79	C10	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, SDMMC1_D3, EVENTOUT	-
-	A3	53	C5	80	B10	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, TSC_G3_IO4, SDMMC1_CK, EVENTOUT	-
-	-	-	-	81	C9	PD0	I/O	FT	-	SPI2_NSS, CAN1_RX, EVENTOUT	-
-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK, CAN1_TX, EVENTOUT	-
-	C4	54	B5	83	C8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	84	B8	PD3	I/O	FT	-	SPI2_MISO, DFSDM1_DATIN0, USART2_CTS, QUADSPI_BK2_NCS, EVENTOUT	-
-	-	-	-	85	B7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, QUADSPI_BK2_IO0, EVENTOUT	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
45	A6	61	B3	95	A3	PB8	I/O	FT_f	-	I2C1_SCL, CAN1_RX, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
46	C6	62	A3	96	B3	PB9	I/O	FT_f	-	IR_OUT, I2C1_SDA, SPI2_NSS, CAN1_TX, SDMMC1_D5, SAI1_FS_A, EVENTOUT	-
-	-	-	-	97	C3	PE0	I/O	FT	-	TIM16_CH1, EVENTOUT	-
-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
47	A7	63	D4	99	D3	VSS	S	-	-	-	-
48	A8	64	E4	100	C4	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0394 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 17. Alternate function AF0 to AF7[1] (continued)

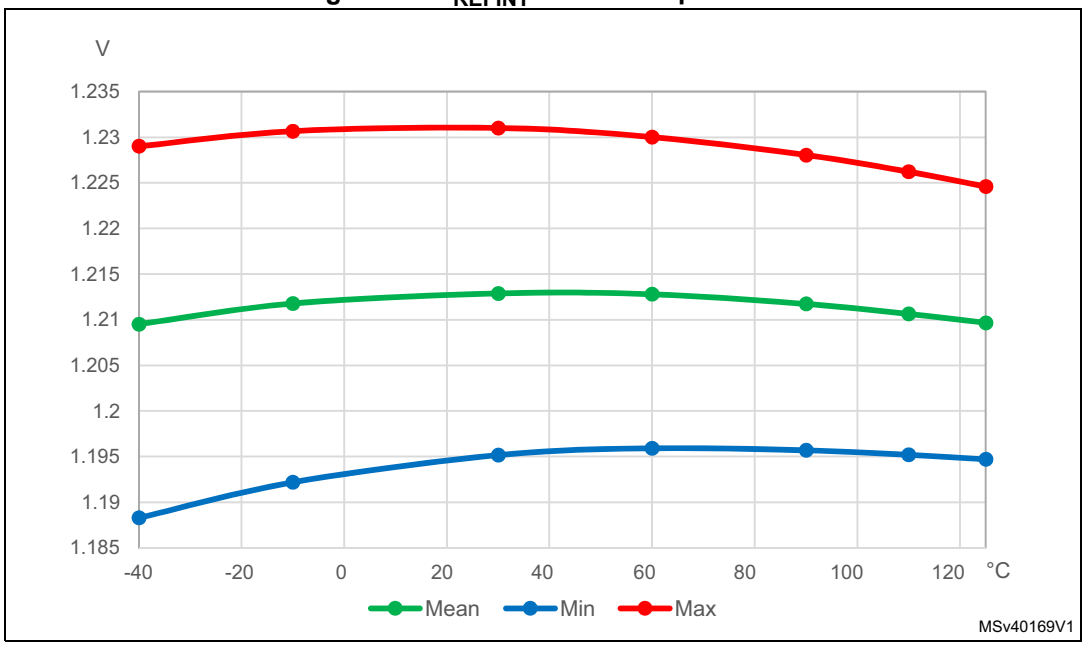
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

1. Please refer to *Table 18* for AF8 to AF15.

Table 18. Alternate function AF8 to AF15(1)

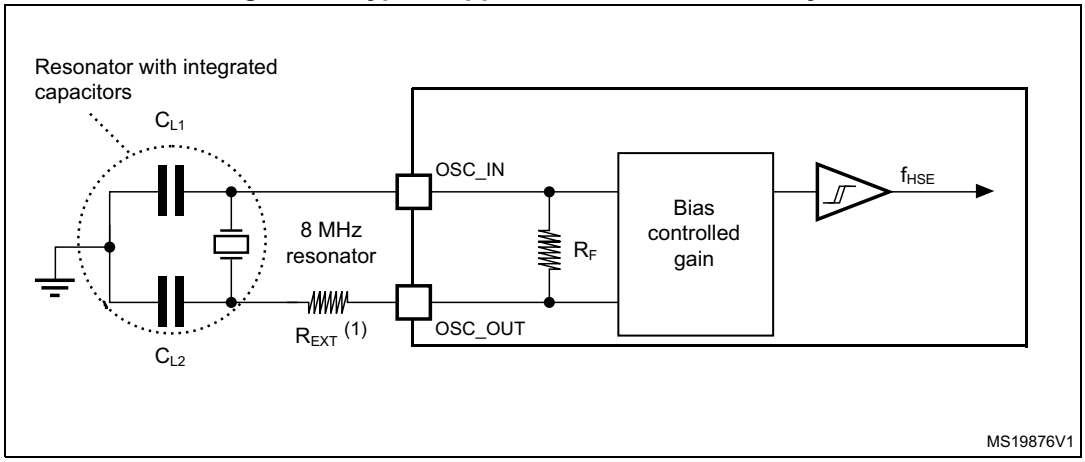
Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_ BK1_NCS	-	COMP2_OUT	-	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_ BK1_IO3	-	TIM1_BKIN_ COMP2	-	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_ BK1_IO2	-	COMP2_OUT	-	-	EVENTOUT
	PA8	-	-	-	-	-	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PA11	-	CAN1_RX	-	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PA13	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_ DE	TSC_G3_IO1	-	-	-	-	-	EVENTOUT

Figure 17. V_{REFINT} versus temperature



Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 48*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 48. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Table 53. PLL, PLLSAI1 characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.0968	-	80	MHz
		Voltage scaling Range 2	3.0968	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 2 PLLs.

Table 87. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1	1	-	-	
		Voltage Range 2	3.5			
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1	1	-	-	
		Voltage Range 2	1.5			
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1	6	-	-	
		Voltage Range 2	6.5			
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1	5.5	-	-	
		Voltage Range 2	5.5			
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	-	5	5.5	
		Voltage Range 2		9.5	14	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	-	5	8.5	
		Voltage Range 2		15	19	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	8	-		
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	13	-		

1. Guaranteed by characterization results.

Table 89. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 50 MHz	-	2	3	ns
t_{OHD}	Output hold default time SD	f_{PP} = 50 MHz	0	-	-	ns

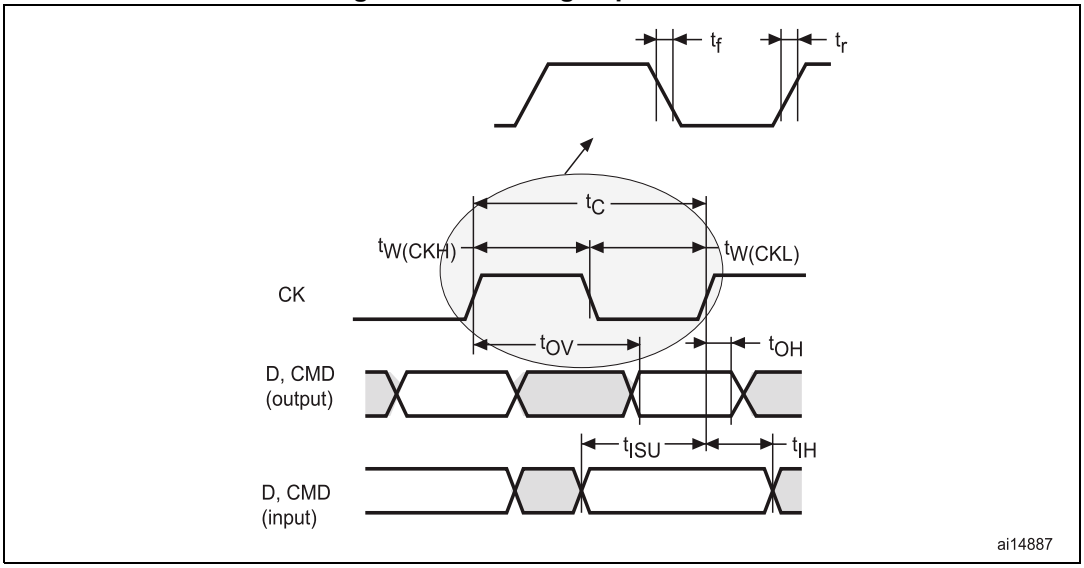
1. Guaranteed by characterization results.

Table 90. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	0	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	1.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 38. SDIO high-speed mode

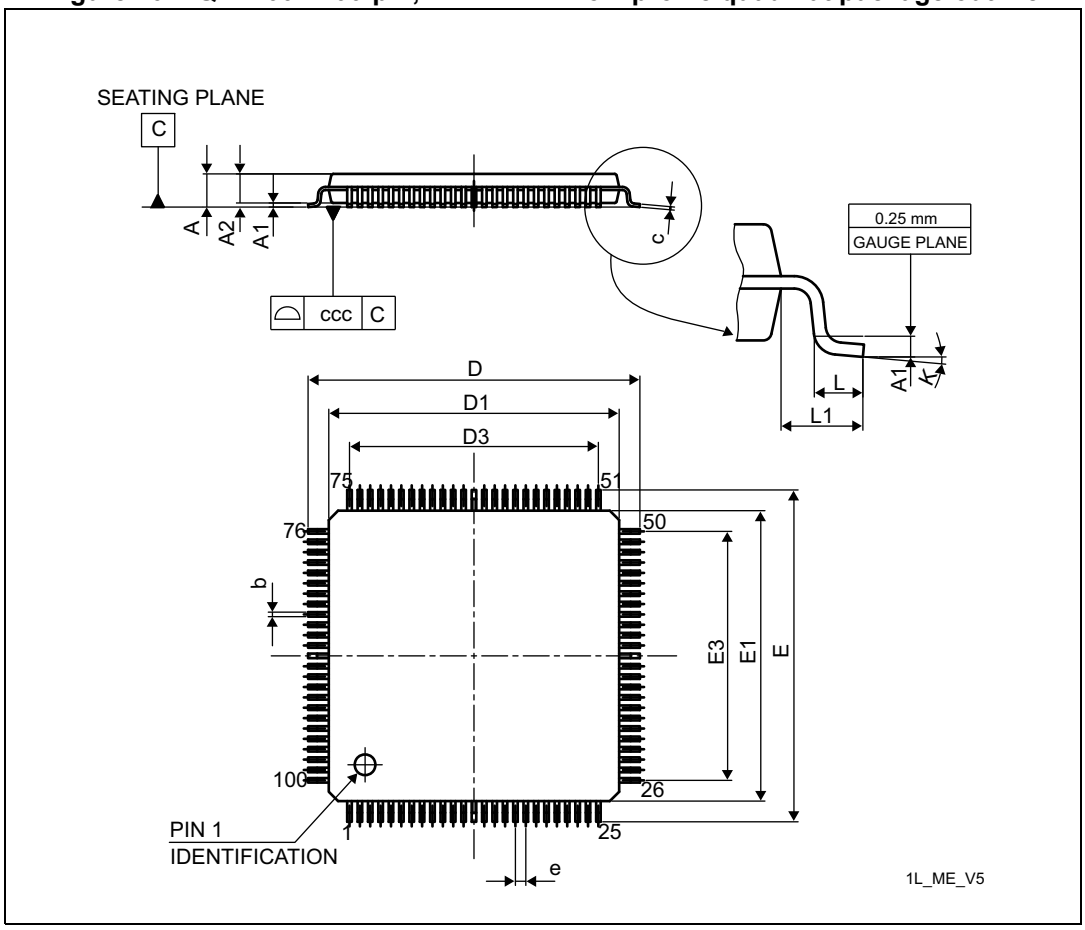


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 40. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 91. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059

Table 92. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

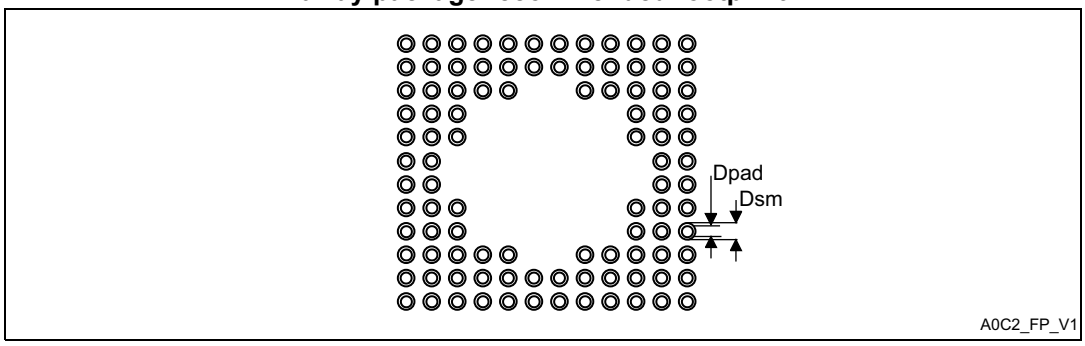


Table 93. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 75 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

T_{Jmax} = 75 °C + (58 °C/W × 447 mW) = 75 °C + 25.926 °C = 100.926 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 3).

Suffix 6: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 105-25.926 = 79.074 °C

Suffix 3: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 130-25.926 = 104.074 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

T_{Jmax} = 100 °C + (58 °C/W × 134 mW) = 100 °C + 7.772 °C = 107.772 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).