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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex® -M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451rei6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451rei6</a>

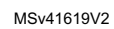
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Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
USARTx (x=1,2,3) UART4	O	O	O	O	O <sup>(6)</sup>	O <sup>(6)</sup>	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O <sup>(6)</sup>	O <sup>(6)</sup>	O <sup>(6)</sup>	O <sup>(6)</sup>	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O <sup>(7)</sup>	O <sup>(7)</sup>	-	-	-	-	-	-	-
I2C3	O	O	O	O	O <sup>(7)</sup>	O <sup>(7)</sup>	O <sup>(7)</sup>	O <sup>(7)</sup>	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O <sup>(8)</sup>	O <sup>(8)</sup>	-	-	-	-	-	-	-	-	-	-	-

### Figure 4. Clock tree



### 3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### 3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to [Table 7: DMA implementation](#) for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

**Table 7. DMA implementation**

DMA features	DMA1	DMA2
Number of regular channels	7	7

### 3.28 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

### 3.29 Serial audio interfaces (SAI)

The device embeds 1 SAI. Refer to [Table 14: SAI implementation](#) for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

**Figure 9. STM32L451Rx UFBGA64 ballout<sup>(1)</sup>**

	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN (PC14)	PC13	PB9	PB4 (NJTRST)	PB3 (JTDO/TRACESWO)	PA15 (JTDI)	PA14 (JTCK/SWCLK)	PA13 (JTMS/SWDIO)
B	PC15-OSC32_OUT (PC15)	VBAT	PB8	PH3-BOOT0 (BOOT0)	PD2	PC11	PC10	PA12
C	PH0-OSC_IN (PH0)	VSS	PB7	PB5	PC12	PA10	PA9	PA11
D	PH1-OSC_OUT (PH1)	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	NRST	PC1	PC0	VDD	VDD	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

MSv40960V1

1. The above figure shows the package top view.

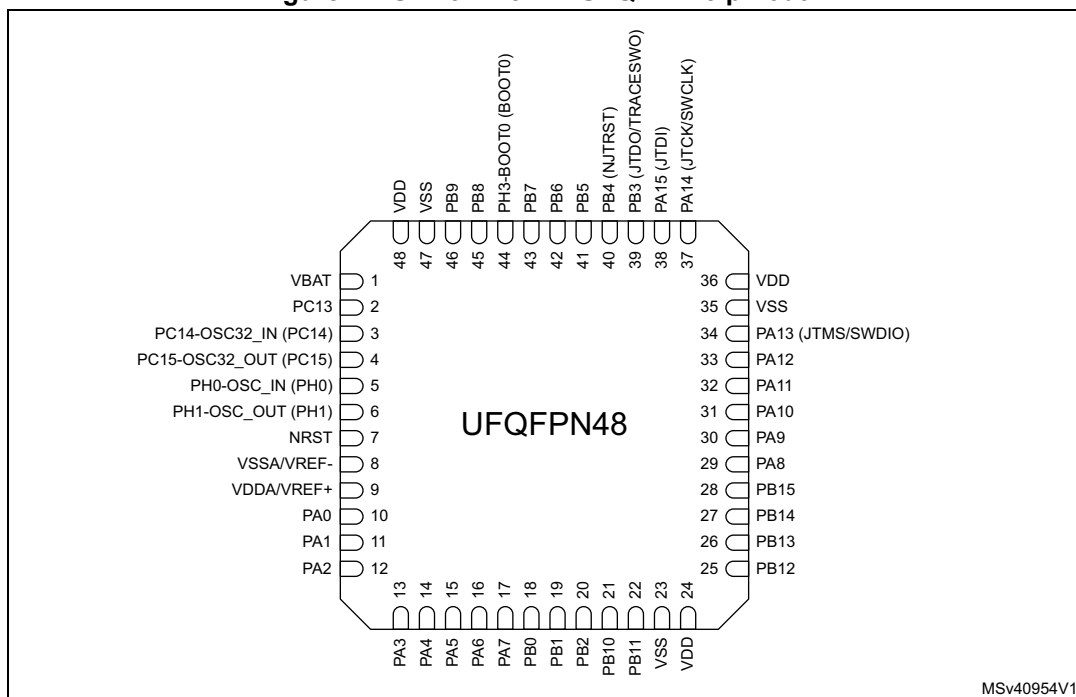
**Figure 10. STM32L451Rx WLCSP64 pinout<sup>(1)</sup>**

	1	2	3	4	5	6	7	8
A	VDD	PA15 (JTDI)	PC12	PB4 (NJTRST)	PB7	PB8	VSS	VDD
B	VSS	VDD	PC11	PB3 (JTDO/TRACESWO)	PB6	PH3-BOOT0 (BOOT0)	VBAT	PC13
C	PA10	PA13 (JTMS/SWDIO)	PA14 (JTCK/SWCLK)	PD2	PB5	PB9	PC15-OSC32_OUT (PC15)	PC14-OSC32_IN (PC14)
D	PA9	PA11	PA12	PC10	PC1	PC2	PC0	PH0-OSC_IN (PH0)
E	PC7	PC9	PA8	PC4	PA7	PA1	PC3	PH1-OSC_OUT (PH1)
F	PB15	PC6	PC8	PB1	PA5	PA3	VDDA/VREF+	NRST
G	PB14	PB13	PB12	PB2	PC5	PA4	PA2	VSSA/VREF-
H	VDD	VSS	PB11	PB10	PB0	PA6	VDD	PA0

MSv40956V1

1. The above figure shows the package top view.



Figure 11. STM32L451Cx UFQFPN48 pinout<sup>(1)</sup>

MSv40954V1

1. The above figure shows the package top view.

Table 15. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_f <sup>(1)</sup>	I/O, Fm+ capable
	_a <sup>(2)</sup>	I/O, with Analog switch function supplied by V <sub>DDA</sub>
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in Table 16 are: FT\_f, FT\_fa.

2. The related I/O structures in Table 16 are: FT\_a, FT\_fa, TT\_a.

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
14	G6	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
15	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, DFSDM1_CKOUT, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
16	H6	22	G4	31	L4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
17	E5	23	H4	32	M4	PA7	I/O	FT_fa	-	TIM1_CH1N, TIM3_CH2, I2C3_SCL, SPI1_MOSI, DFSDM1_DATIN0, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
-	E4	24	H5	33	K5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC1_IN13
-	G5	25	H6	34	L5	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
18	H5	26	F5	35	M5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, SPI1_NSS, DFSDM1_CKIN0, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
19	F4	27	G5	36	M6	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
20	G4	28	G6	37	L6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, EVENTOUT	COMP1_INP
-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, SAI1_SD_B, EVENTOUT	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, EVENTOUT	-
-	-	-	-	87	B6	PD6	I/O	FT	-	DFSDM1_DATIN1, USART2_RX, QUADSPI_BK2_IO2, SAI1_SD_A, EVENTOUT	-
-	-	-	-	88	A5	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, QUADSPI_BK2_IO3, EVENTOUT	-
39	B4	55	A5	89	A8	PB3 (JTDO/ TRACE SWO)	I/O	FT_a	(3)	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT	COMP2_INM
40	A4	56	A4	90	A7	PB4 (NJTRST)	I/O	FT_fa	(3)	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, TSC_G2_IO1, SAI1_MCLK_B, EVENTOUT	COMP2_INP
41	C5	57	C4	91	C5	PB5	I/O	FT	-	LPTIM1_IN1, TIM3_CH2, CAN1_RX, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
42	B5	58	D3	92	B5	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, I2C4_SCL, USART1_TX, CAN1_TX, TSC_G2_IO3, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP
43	A5	59	C3	93	B4	PB7	I/O	FT_fa	-	LPTIM1_IN2, I2C1_SDA, I2C4_SDA, USART1_RX, UART4_CTS, TSC_G2_IO4, EVENTOUT	COMP2_INM, PVD_IN
44	B6	60	B4	94	A4	PH3- BOOT0 (BOOT0)	I/O	-	-	EVENTOUT	BOOT0

Table 17. Alternate function AF0 to AF7<sup>(1)</sup> (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_ DE
	PD3	-	-	-	-	-	SPI2_MISO	DFSDM1_ DATIN0	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_ CKIN0	USART2_RTS_ DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	-	-	DFSDM1_ DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_ CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS
	PD12	-	-	-	-	I2C4_SCL	-	-	USART3_RTS_ DE
	PD13	-	-	-	-	I2C4_SDA	-	-	-
	PD14	-	-	-	-	-	-	-	-
	PD15	-	-	-	-	-	-	-	-

**Table 17. Alternate function AF0 to AF7<sup>(1)</sup> (continued)**

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

1. Please refer to [Table 18](#) for AF8 to AF15.

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^{\circ}\text{C}$  and  $T_A = T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean  $\pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = V_{DDA} = 3\text{ V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean  $\pm 2\sigma$ ).

#### 6.1.3 Typical curves

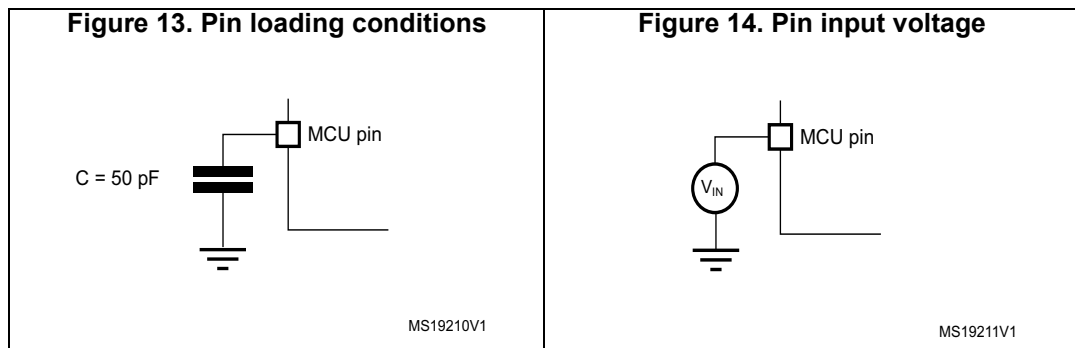
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 13](#).

#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 14](#).





**Table 29. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1**

Symbol	Parameter	Conditions			TYP					MAX <sup>(1)</sup>					Unit
		-	Voltage scaling	f <sub>HCLK</sub>	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I <sub>DD_ALL</sub> (Run)	Supply current in Run mode	f <sub>HCLK</sub> = f <sub>HSE</sub> up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.40	2.40	2.55	2.70	3.05	2.70	2.75	2.90	3.20	3.80	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.80	1.95	2.25	2.80	
				8 MHz	0.820	0.850	0.950	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.470	0.500	0.600	0.765	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.325	0.420	0.585	0.915	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.210	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.750	0.15	0.25	0.35	0.65	1.25	
			Range 1	80 MHz	8.55	8.60	8.75	8.95	9.35	9.55	9.65	9.85	10.5	11.0	
				72 MHz	7.70	7.80	7.90	8.15	8.50	8.60	8.70	8.90	9.25	9.95	
				64 MHz	6.90	6.95	7.10	7.30	7.70	7.70	7.75	7.95	8.35	9.00	
				48 MHz	5.15	5.20	5.30	5.55	5.90	5.75	5.85	6.05	6.40	7.05	
				32 MHz	3.45	3.50	3.65	3.85	4.25	3.90	4.00	4.20	4.50	5.15	
				24 MHz	2.65	2.70	2.80	3.00	3.40	3.00	3.05	3.25	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.55	2.05	2.10	2.30	2.60	3.25	
I <sub>DD_ALL</sub> (LPRun)	Supply current in low-power run mode	f <sub>HCLK</sub> = f <sub>MSI</sub> all peripherals disable FLASH in power-down	2 MHz	220	255	360	540	895	270	330	460	760	1400	μA	
			1 MHz	120	155	260	440	795	165	215	370	660	1300		
			400 kHz	60.0	92.0	195	375	730	100	160	330	585	1250		
			100 kHz	36.0	62.5	165	345	695	63.0	130	305	555	1200		

1. Guaranteed by characterization results, unless otherwise specified.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 41](#). The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 20: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 41](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

**Table 41. Peripheral current consumption**

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix <sup>(1)</sup>	3.2	2.9	3.1	μA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA <sup>(2)</sup>	1.7	1.4	1.6	
	GPIOB <sup>(2)</sup>	1.6	1.3	1.6	
	GPIOC <sup>(2)</sup>	1.7	1.5	1.6	
	GPIOD <sup>(2)</sup>	1.8	1.6	1.7	
	GPIOE <sup>(2)</sup>	1.7	1.6	1.6	
	GPIOH <sup>(2)</sup>	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	N/A	N/A	
	RNG clock domain	0.5	N/A	N/A	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge <sup>(3)</sup>	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	
	DAC1	2.4	1.8	2.2	



### 6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 56](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 56. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 80\text{ MHz}$ , conforming to IEC 61000-4-2	3B
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 80\text{ MHz}$ , conforming to IEC 61000-4-4	5A

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 67. ADC characteristics<sup>(1) (2)</sup> (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATR}$	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
$t_s$	Sampling time	$f_{ADC} = 80$ MHz	0.03125	-	8.00625	$\mu s$
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	$\mu s$
$t_{CONV}$	Total conversion time (including sampling time)	$f_{ADC} = 80$ MHz Resolution = 12 bits	0.1875	-	8.1625	$\mu s$
		Resolution = 12 bits	$t_s + 12.5$ cycles for successive approximation = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the $V_{DDA}$ supply	$f_s = 5$ Msps	-	730	830	$\mu A$
		$f_s = 1$ Msps	-	160	220	
		$f_s = 10$ ksps	-	16	50	
$I_{DDV\_S}(ADC)$	ADC consumption from the $V_{REF+}$ single ended mode	$f_s = 5$ Msps	-	130	160	$\mu A$
		$f_s = 1$ Msps	-	30	40	
		$f_s = 10$ ksps	-	0.6	2	
$I_{DDV\_D}(ADC)$	ADC consumption from the $V_{REF+}$ differential mode	$f_s = 5$ Msps	-	260	310	$\mu A$
		$f_s = 1$ Msps	-	60	70	
		$f_s = 10$ ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when  $V_{DDA} < 2.4$  V (BOOSTEN = 1 in the SYSCFG\_CFGR1 when  $V_{DDA} < 2.4$  V). It is disable when  $V_{DDA} \geq 2.4$  V.
3.  $V_{REF+}$  can be internally connected to  $V_{DDA}$  and  $V_{REF-}$  can be internally connected to  $V_{SSA}$ , depending on the package. Refer to [Section 4: Pinouts and pin description](#) for further details.

The maximum value of  $R_{AIN}$  can be found in [Table 68: Maximum ADC RAIN](#).

Table 84. I2C analog filter characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Max	Unit
$t_{AF}$	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	260 <sup>(3)</sup>	ns

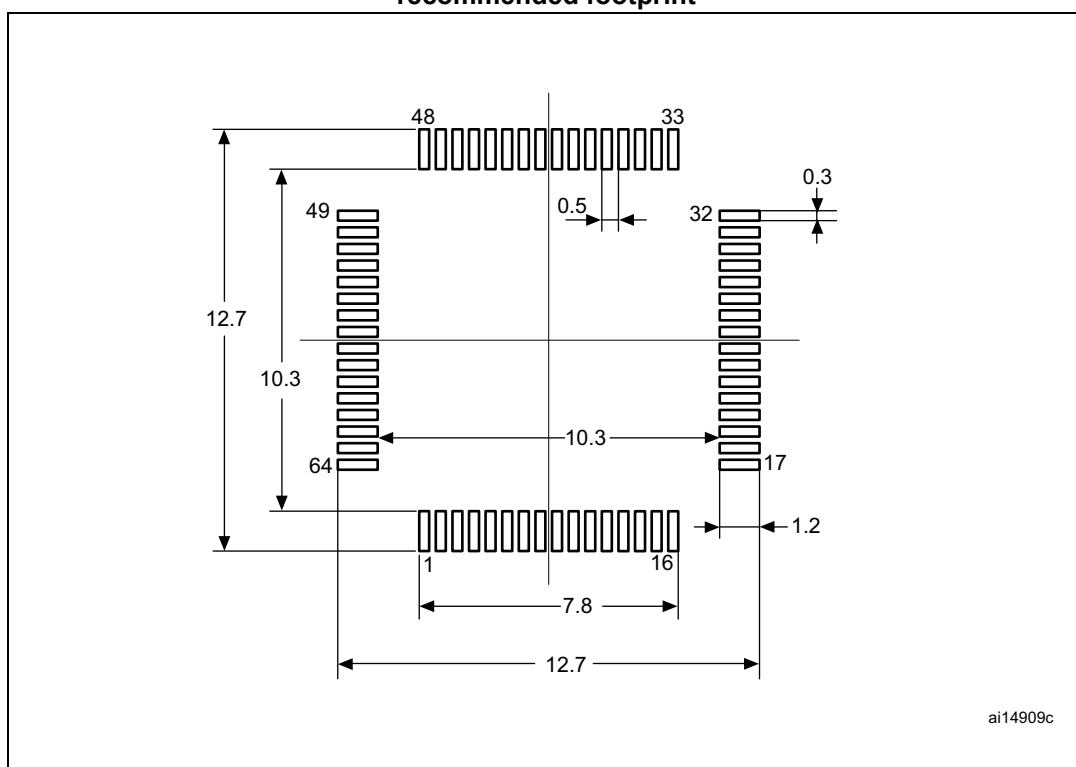
1. Guaranteed by design.
2. Spikes with widths below  $t_{AF(min)}$  are filtered.
3. Spikes with widths above  $t_{AF(max)}$  are not filtered

**Table 94. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**



1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 75\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$ :

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 100](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $58\text{ °C/W}$

$$T_{Jmax} = 75\text{ °C} + (58\text{ °C/W} \times 447\text{ mW}) = 75\text{ °C} + 25.926\text{ °C} = 100.926\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ) see [Section 8: Ordering information](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

**Note:** With this given  $P_{Dmax}$  we can find the  $T_{Amax}$  allowed for a given device temperature range (order code suffix 6 or 3).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (58\text{ °C/W} \times 447\text{ mW}) = 105 - 25.926 = 79.074\text{ °C}$$

$$\text{Suffix 3: } T_{Amax} = T_{Jmax} - (58\text{ °C/W} \times 447\text{ mW}) = 130 - 25.926 = 104.074\text{ °C}$$

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 100\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus:  $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 100](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $58\text{ °C/W}$

$$T_{Jmax} = 100\text{ °C} + (58\text{ °C/W} \times 134\text{ mW}) = 100\text{ °C} + 7.772\text{ °C} = 107.772\text{ °C}$$

This is above the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).