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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451ret6

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L451xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DAC and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 5. Voltage reference buffer

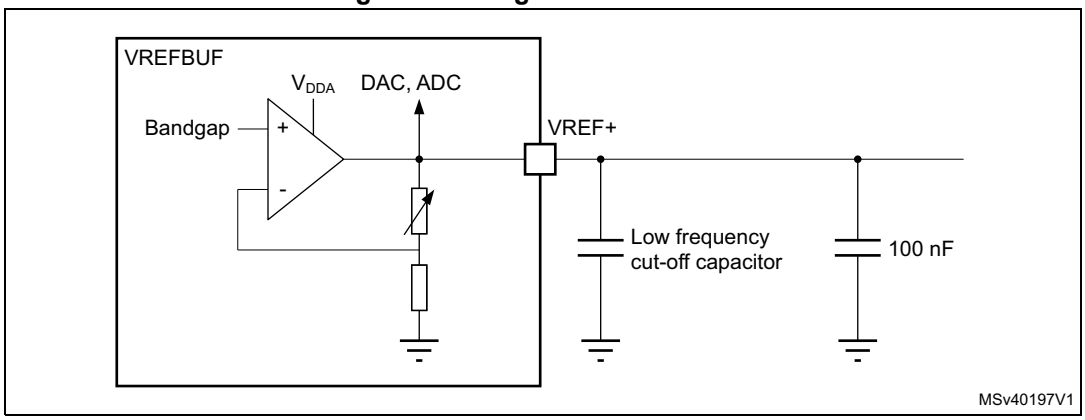


Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	D5	9	E2	16	J2	PC1	I/O	FT_fa	-	TRACED0, LPTIM1_OUT, I2C4_SDA, I2C3_SDA, LPUART1_TX, EVENTOUT	ADC1_IN2
-	D6	10	F2	17	J3	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, EVENTOUT	ADC1_IN3
-	E7	11	G1	18	K2	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	-	19	J1	VSSA	S	-	-	-	-
-	-	-	-	20	K1	VREF-	S	-	-	-	-
8	G8	12	F1	-	-	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	22	M1	VDDA	S	-	-	-	-
9	F7	13	H1	-	-	VDDA/ VREF+	S	-	-	-	-
10	H8	14	G2	23	L2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, UART4_TX, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM, ADC1_IN5, RTC_TAMP2, WKUP1
11	E6	15	H2	24	M2	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP, ADC1_IN6
12	G7	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4,LSCO
13	F6	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	18	C2	27	E3	VSS	S	-	-	-	-
-	H7	19	D2	28	H3	VDD	S	-	-	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 13*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 14*.

Figure 13. Pin loading conditions

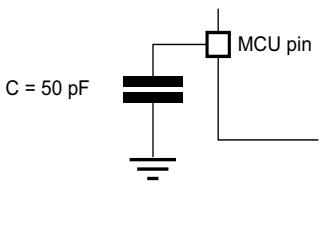
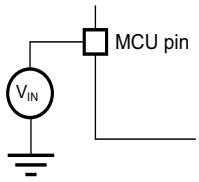


Figure 14. Pin input voltage



4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 21. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	140	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(4)	
	Injected current on PA4, PA5	-5/0	
$\Sigma\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 42. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	3.34	4.3	µs
			Wakeup clock HSI16 = 16 MHz	3.7	6.5	
		Range 2	Wakeup clock MSI = 24 MHz	3.8	7.1	
			Wakeup clock HSI16 = 16 MHz	3.7	6.5	
			Wakeup clock MSI = 4 MHz	9.3	7.1	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.85	2.7	
			Wakeup clock HSI16 = 16 MHz	2.68	3	
		Range 2	Wakeup clock MSI = 24 MHz	2.47	3.4	
			Wakeup clock HSI16 = 16 MHz	2.68	3	
			Wakeup clock MSI = 4 MHz	9.67	12.5	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.75	7.6	µs
			Wakeup clock HSI16 = 16 MHz	7.14	8	
		Range 2	Wakeup clock MSI = 24 MHz	7	7.82	
			Wakeup clock HSI16 = 16 MHz	7.14	7.9	
			Wakeup clock MSI = 4 MHz	10.44	11.9	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.21	5.9	
			Wakeup clock HSI16 = 16 MHz	6.23	6.9	
		Range 2	Wakeup clock MSI = 24 MHz	5.73	6.4	
			Wakeup clock HSI16 = 16 MHz	6.23	6.9	
			Wakeup clock MSI = 4 MHz	10.9	12.3	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	16.05	19.2	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			17.06	20.3	

Table 42. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	7.93	9.1	µs
			Wakeup clock HSI16 = 16 MHz	7.32	8.5	
		Range 2	Wakeup clock MSI = 24 MHz	8.25	9.4	
			Wakeup clock HSI16 = 16 MHz	7.32	8.4	
			Wakeup clock MSI = 4 MHz	11.43	13.3	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.23	6	
			Wakeup clock HSI16 = 16 MHz	6.33	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.78	6.5	
			Wakeup clock HSI16 = 16 MHz	6.33	7.1	
			Wakeup clock MSI = 4 MHz	11.37	12.9	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	16.13	18.2	µs
			Wakeup clock MSI = 4 MHz	24.06	26.6	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	16.09	18.2	µs
			Wakeup clock MSI = 4 MHz	24	26.6	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	255.38	316.41	µs

1. Guaranteed by characterization results.

Table 43. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 44. Wakeup time using USART/LPUART(1)

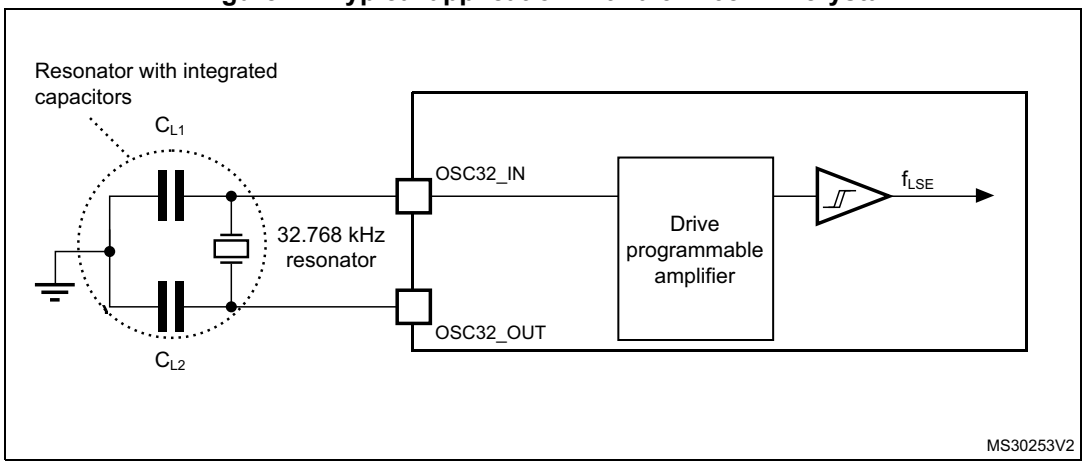
Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI16	Stop 0 mode	-	1.7	µs
		Stop 1 mode and Stop 2 mode	-	8.5	

1. Guaranteed by design.

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

High-speed internal 48 MHz (HSI48) RC oscillator

Table 51. HSI48 oscillator characteristics(1)

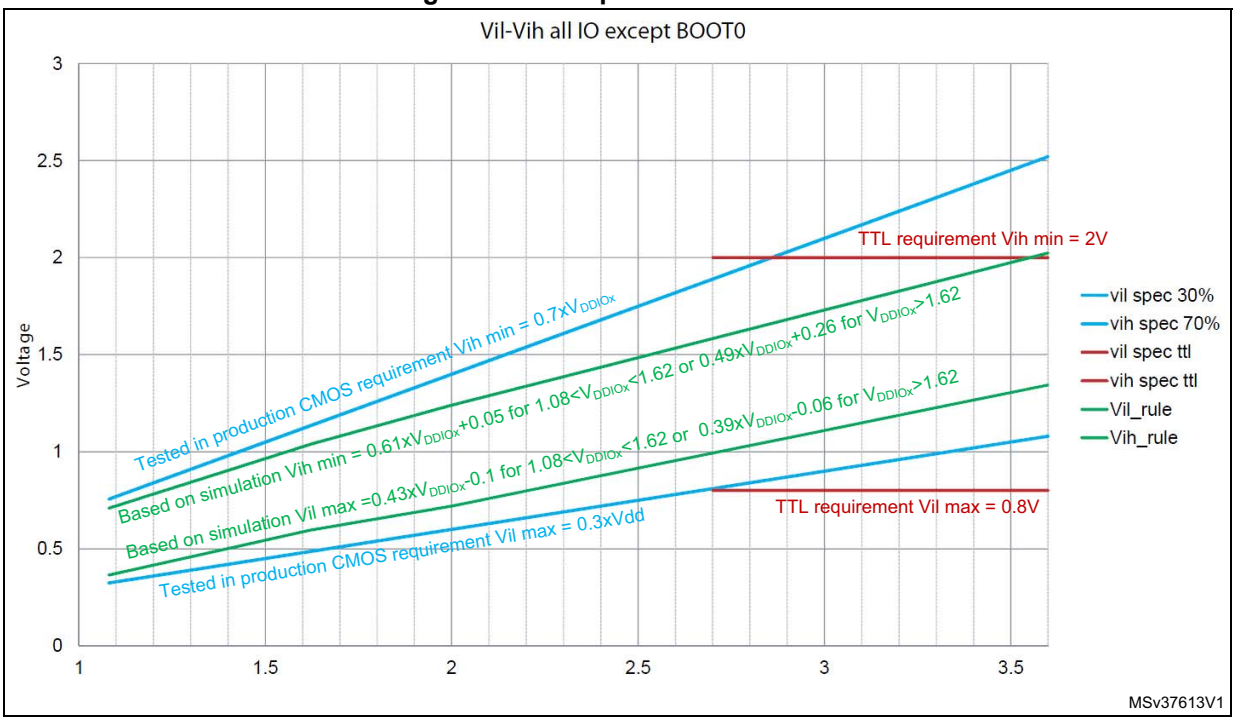
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

1. Refer to *Figure 25: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. All FT_xx IO except PA11, PA12 and PC3 I/O.
5. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.
6. To sustain a voltage higher than Min(V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
7. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 25* for standard I/Os, and in *Figure 25* for 5 V tolerant I/Os.

Figure 25. I/O input characteristics



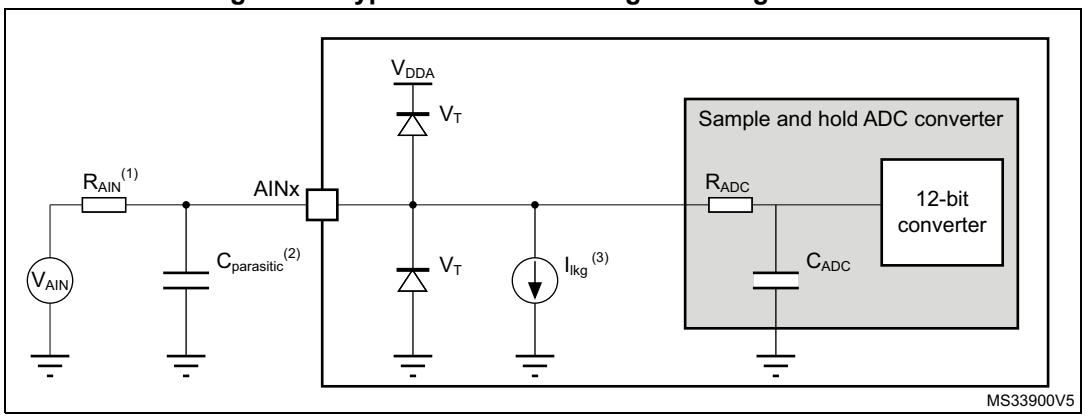
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

Table 72. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 67: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 61: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 61: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 15: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 Voltage reference buffer characteristics

Table 75. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046(3)	2.048	2.049(3)	
			V_{RS} = 1	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA

6.3.21 Comparator characteristics

Table 76. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 77. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

SPI characteristics

Unless otherwise specified, the parameters given in *Table 85* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 23: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 85. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	-	40	MHz
		Master mode receiver/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1			16	
		Master mode transmitter 1.71 < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode receiver 1.71 < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode transmitter/full duplex 2.7 < V_{DD} < 3.6 V Voltage Range 1			37(2)	
		Slave mode transmitter/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1			20(2)	
		Voltage Range 2			13	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4 \times T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2 \times T_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{PCLK}-2$	T_{PCLK}	$T_{PCLK}+2$	ns
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	ns
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	36	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns

Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 86* and *Table 87* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 86. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.71 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	5	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Figure 34. Quad SPI timing diagram - SDR mode

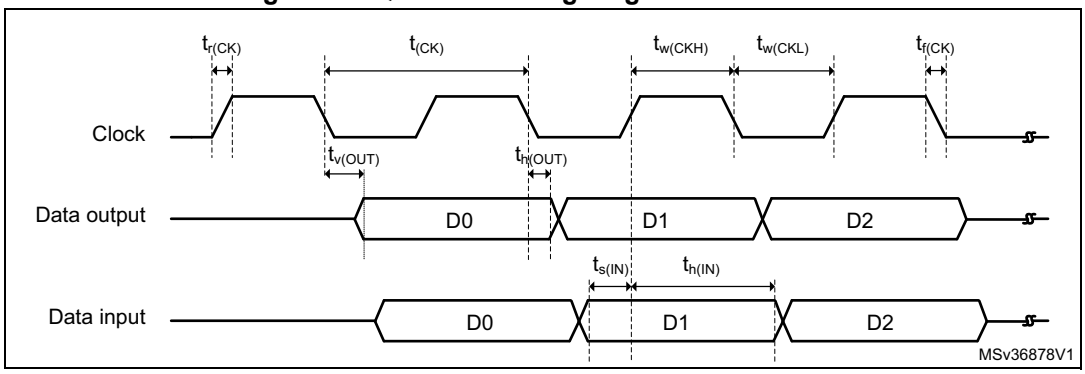


Figure 35. Quad SPI timing diagram - DDR mode

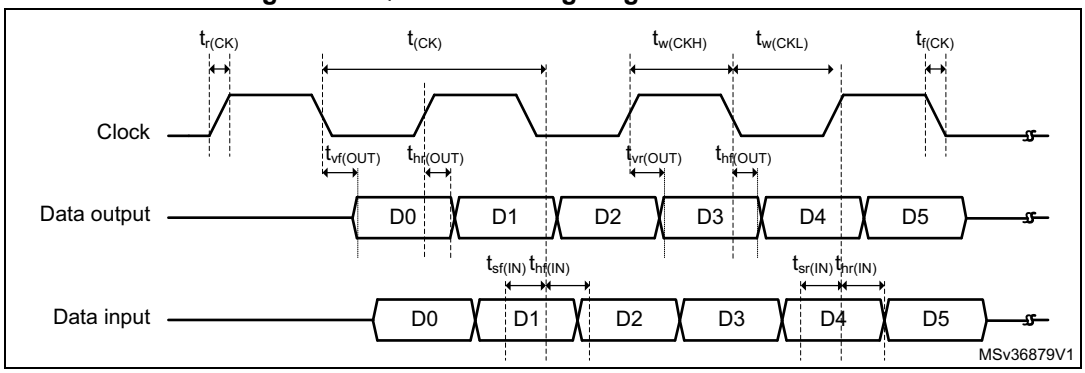
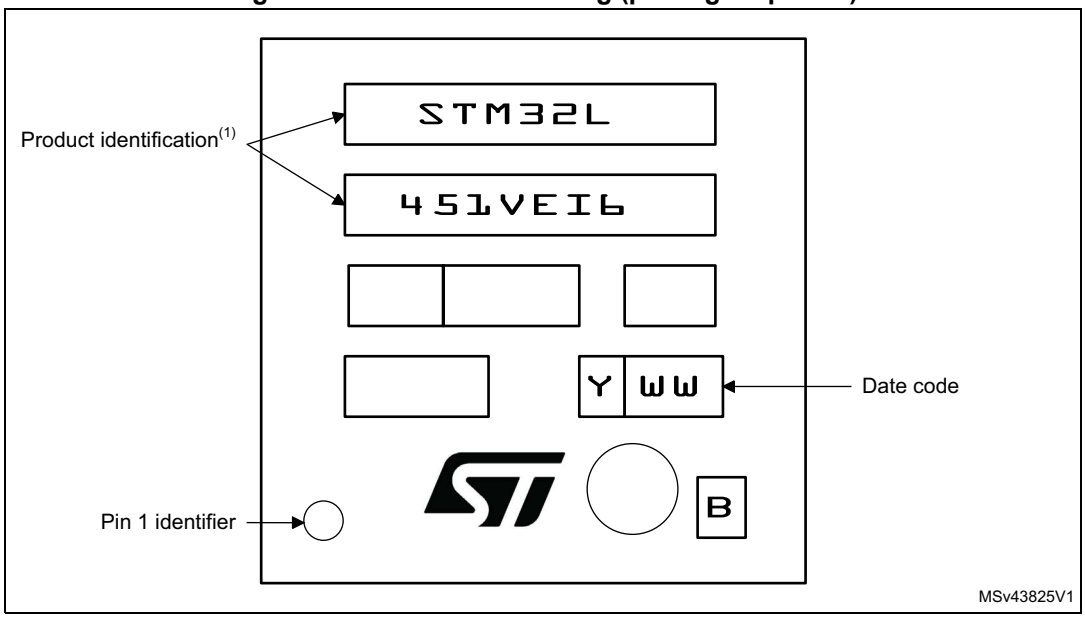


Figure 45. UFBGA100 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 75 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

T_{Jmax} = 75 °C + (58 °C/W × 447 mW) = 75 °C + 25.926 °C = 100.926 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 3).

Suffix 6: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 105-25.926 = 79.074 °C

Suffix 3: T_{Amax} = T_{Jmax} - (58°C/W × 447 mW) = 130-25.926 = 104.074 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 100* T_{Jmax} is calculated as follows:

– For LQFP64, 58 °C/W

T_{Jmax} = 100 °C + (58 °C/W × 134 mW) = 100 °C + 7.772 °C = 107.772 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).