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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.36x3.66)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451rey6tr

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Table 2. STM32L451xx family device features and peripheral counts (continued)

Peripheral	STM32L451Vx	STM32L451Rx	STM32L451Cx
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	UFQFPN48

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L451xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L451xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.



Table 4. STM32L451xx modes overview

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source	Consumption ⁽³⁾	Wakeup time
Run	MR range 1	Yes	ON ⁽⁴⁾	ON	Any	All	N/A	94 µA/MHz	N/A
	MR range2					All except RNG		85 µA/MHz	
LPRun	LPR	Yes	ON ⁽⁴⁾	ON	Any except PLL	All except RNG	N/A	95 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any	All	Any interrupt or event	27 µA/MHz	6 cycles
	MR range2					All except RNG		27 µA/MHz	
LPSleep	LPR	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any except PLL	All except RNG	Any interrupt or event	38 µA/MHz	6 cycles
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2)	125 µA	2.47 µs in SRAM 4.1 µs in Flash
	MR Range 2							125 µA	

3.11 Clocks and startup

The clock controller (see [Figure 4](#)) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
 - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
 - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than $\pm 0.25\%$ accuracy. The MSI can supply a PLL.
 - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **RC48 with clock recovery system (HSI48):** internal RC48 MHz clock source can be used to drive the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
 - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is $\pm 5\%$ accuracy.
- **Peripheral clock sources:** Several peripherals (SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Two PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the SDMMC/RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 67 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 37 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	D5	9	E2	16	J2	PC1	I/O	FT_fa	-	TRACED0, LPTIM1_OUT, I2C4_SDA, I2C3_SDA, LPUART1_TX, EVENTOUT	ADC1_IN2
-	D6	10	F2	17	J3	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, EVENTOUT	ADC1_IN3
-	E7	11	G1	18	K2	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	-	19	J1	VSSA	S	-	-	-	-
-	-	-	-	20	K1	VREF-	S	-	-	-	-
8	G8	12	F1	-	-	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	22	M1	VDDA	S	-	-	-	-
9	F7	13	H1	-	-	VDDA/ VREF+	S	-	-	-	-
10	H8	14	G2	23	L2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, UART4_TX, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM, ADC1_IN5, RTC_TAMP2, WKUP1
11	E6	15	H2	24	M2	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP, ADC1_IN6
12	G7	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4, LSCO
13	F6	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	18	C2	27	E3	VSS	S	-	-	-	-
-	H7	19	D2	28	H3	VDD	S	-	-	-	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	60	H12	PD13	I/O	FT	-	I2C4_SDA, TSC_G6_IO4, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	61	H11	PD14	I/O	FT	-	EVENTOUT	-
-	-	-	-	62	H10	PD15	I/O	FT	-	EVENTOUT	-
-	F2	37	F6	63	E12	PC6	I/O	FT	-	TIM3_CH1, DFSDM1_CKIN3, TSC_G4_IO1, SDMMC1_D6, EVENTOUT	-
-	E1	38	E7	64	E11	PC7	I/O	FT	-	TIM3_CH2, DFSDM1_DATIN3, TSC_G4_IO2, SDMMC1_D7, EVENTOUT	-
-	F3	39	E8	65	E10	PC8	I/O	FT	-	TIM3_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
-	E2	40	D8	66	D12	PC9	I/O	FT	-	TIM3_CH4, TSC_G4_IO4, SDMMC1_D1, EVENTOUT	-
29	E3	41	D7	67	D11	PA8	I/O	FT	-	MCO, TIM1_CH1, DFSDM1_CKIN1, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	D1	42	C7	68	D10	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, DFSDM1_DATIN1, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
31	C1	43	C6	69	C12	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, SAI1_SD_A, EVENTOUT	-
32	D2	44	C8	70	B12	PA11	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, TIM1_BKIN2_COMP1, EVENTOUT	-
33	D3	45	B8	71	A12	PA12	I/O	FT_f	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, EVENTOUT	-
34	C2	46	A8	72	A11	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JTMS/SWDAT, IR_OUT, SAI1_SD_B, EVENTOUT	-
35	B1	47	D5	-	-	VSS	S	-	-	-	-
36	A1	48	E5	73	C11	VDD	S	-	-	-	-

Table 18. Alternate function AF8 to AF15⁽¹⁾

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_ BK1_NCS	-	COMP2_OUT	-	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_ BK1_IO3	-	TIM1_BKIN_ COMP2	-	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_ BK1_IO2	-	COMP2_OUT	-	-	EVENTOUT
	PA8	-	-	-	-	-	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PA11	-	CAN1_RX	-	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PA13	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_ DE	TSC_G3_IO1	-	-	-	-	-	EVENTOUT

1. Please refer to [Table 17](#) for AF0 to AF7.



Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR ⁽³⁾ (except BOR0) and PVD consumption from V_{DD}) ⁽²⁾		-	-	1.1	1.6	μA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1) ⁽²⁾	PVM1 consumption from V_{DD}	-	-	0.2	-	μA
I_{DD} (PVM3/PVM4) ⁽²⁾	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	μA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

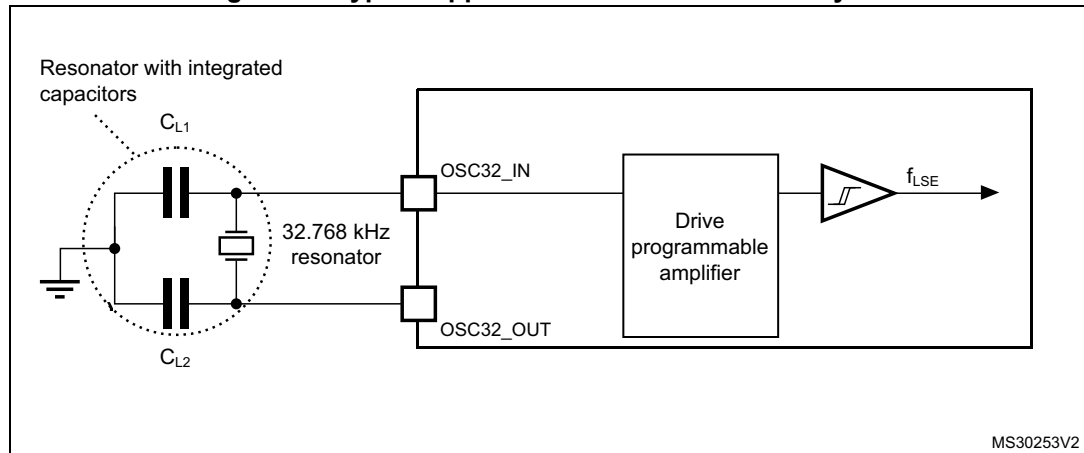
2. Guaranteed by design.

3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{V}$). It is disable when $V_{DDA} \geq 2.4\text{ V}$.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 69. ADC accuracy - limited test conditions 1⁽¹⁾(2)(3)

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	5	LSB
			Slow channel (max speed)	-	4	5	
		Differential	Fast channel (max speed)	-	3.5	4.5	
			Slow channel (max speed)	-	3.5	4.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	2.5	
			Slow channel (max speed)	-	1	2.5	
		Differential	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	4.5	
			Slow channel (max speed)	-	2.5	4.5	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
		Differential	Fast channel (max speed)	-	1	2	
			Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.4	10.5	-	bits
			Slow channel (max speed)	10.4	10.5	-	
		Differential	Fast channel (max speed)	10.8	10.9	-	
			Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	64.4	65	-	dB
			Slow channel (max speed)	64.4	65	-	
		Differential	Fast channel (max speed)	66.8	67.4	-	
			Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
		Differential	Fast channel (max speed)	67	68	-	
			Slow channel (max speed)	67	68	-	

Table 72. ADC accuracy - limited test conditions 4⁽¹⁾⁽²⁾⁽³⁾ (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V _{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
		Differential	Fast channel (max speed)	-	-73	-72		
			Slow channel (max speed)	-	-73	-72		

- Guaranteed by design.
- ADC DC accuracy values are measured after internal calibration.
- ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
- The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4 \text{ V}$). It is disable when $V_{DDA} \geq 2.4 \text{ V}$. No oversampling.

Figure 28. ADC accuracy characteristics

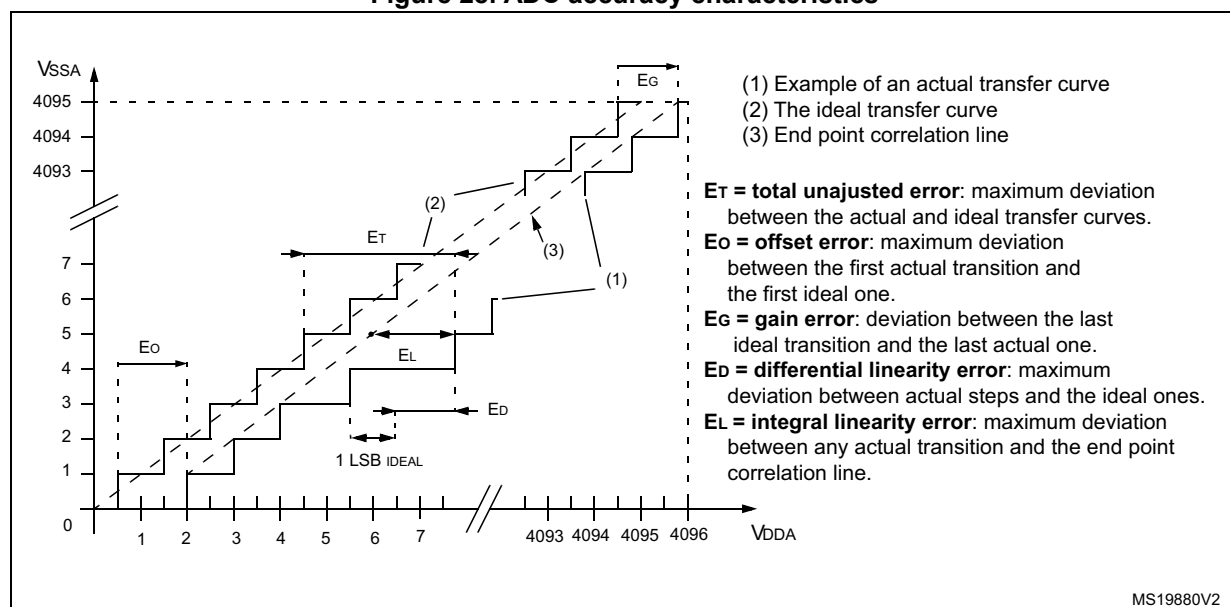


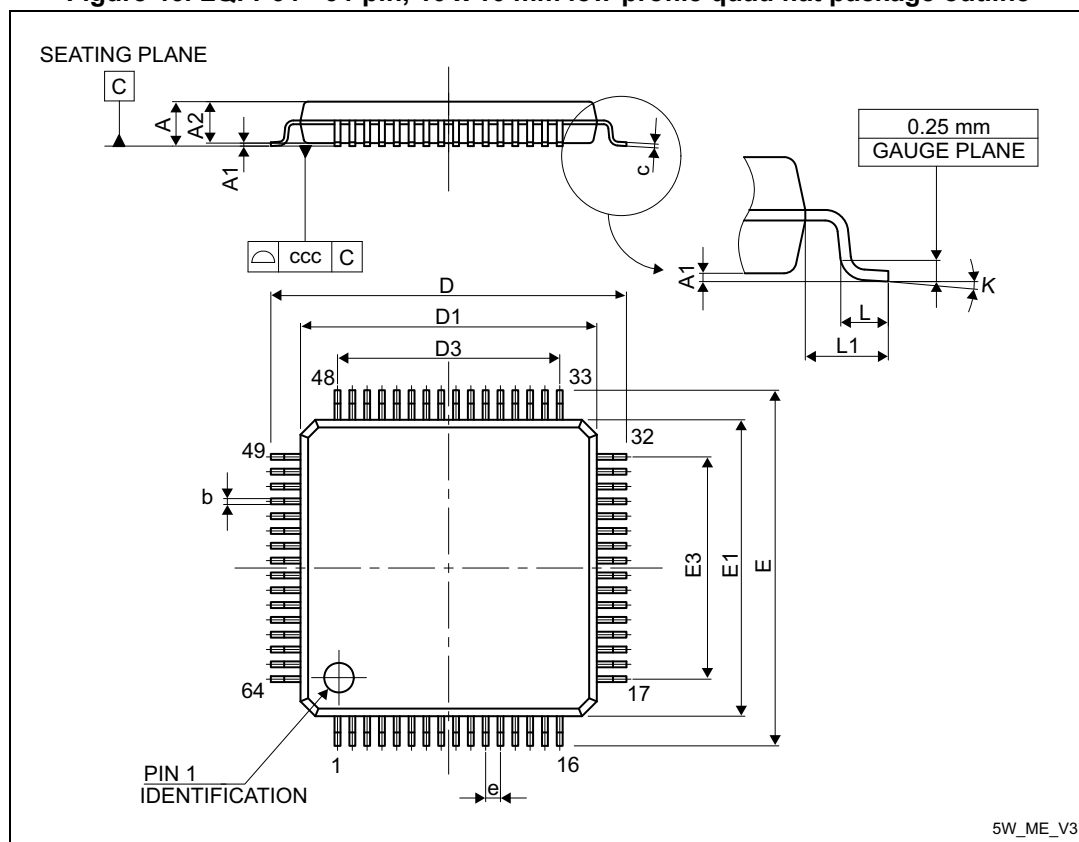
Table 74. DAC accuracy⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFFF when buffer is OFF, and from code giving 0.2 V and ($V_{REF+} - 0.2$) V when buffer is ON.

7.3 LQFP64 package information

Figure 46. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

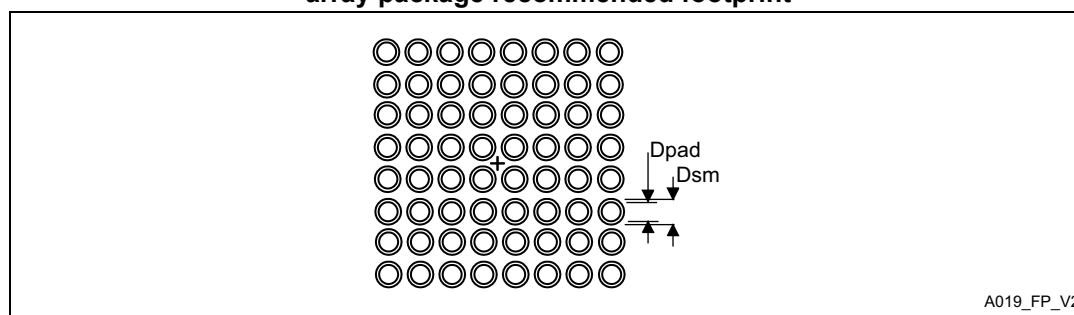
Table 94. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 95. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

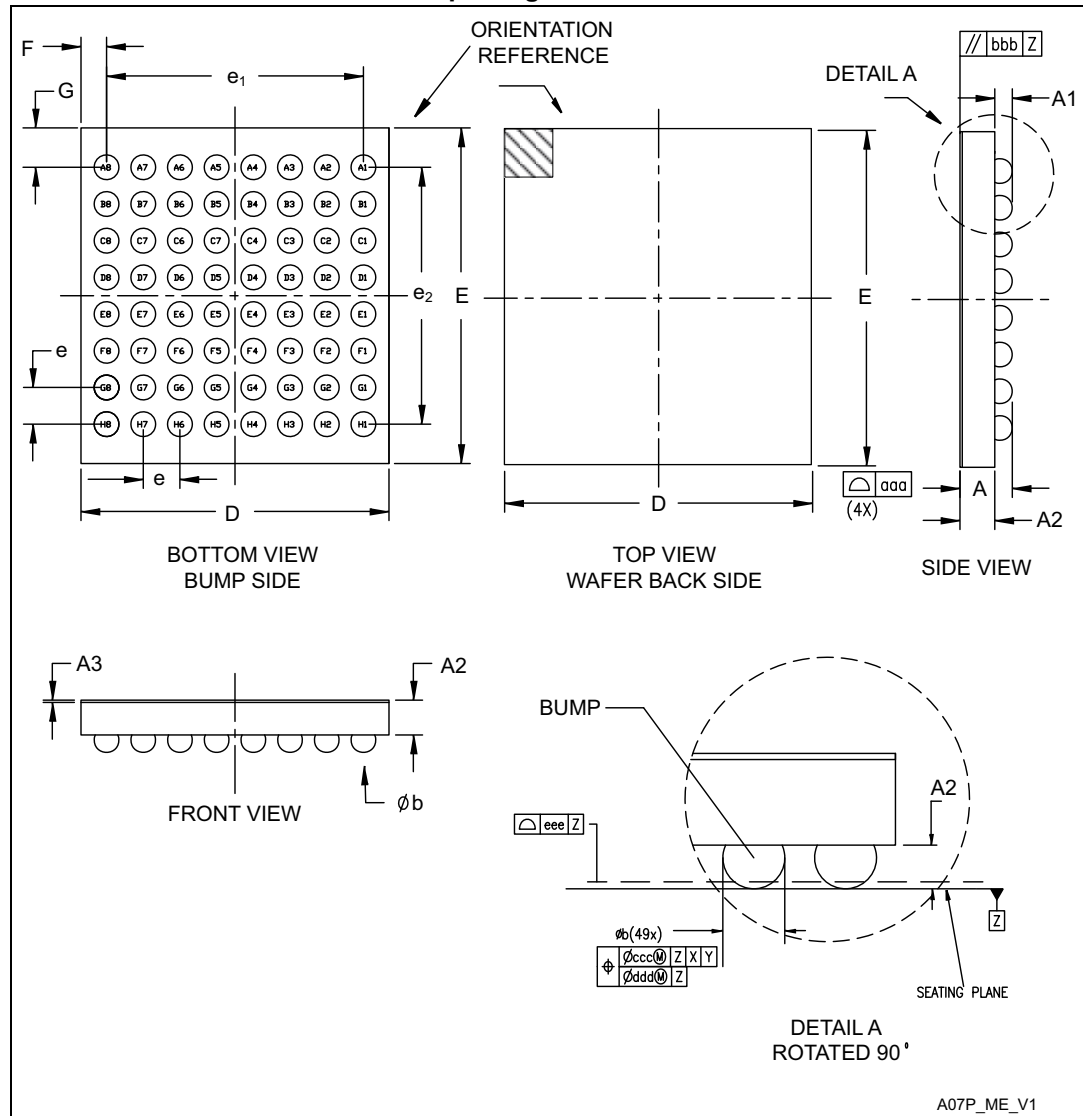
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint**Table 96. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm

7.5 WLCSP64 package information

Figure 52. WLCSP64 - 64-ball, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale package outline



1. Dimensions are expressed in millimeters.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of all I_{DDXXX} and V_{DDXXX} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 100. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	56	°C/W
	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm / 0.5 mm pitch	75	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	58	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient WLCSP64 3.141 × 3.127 / 0.35 mm pitch	53	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm / 0.5 mm pitch	29	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L451xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.