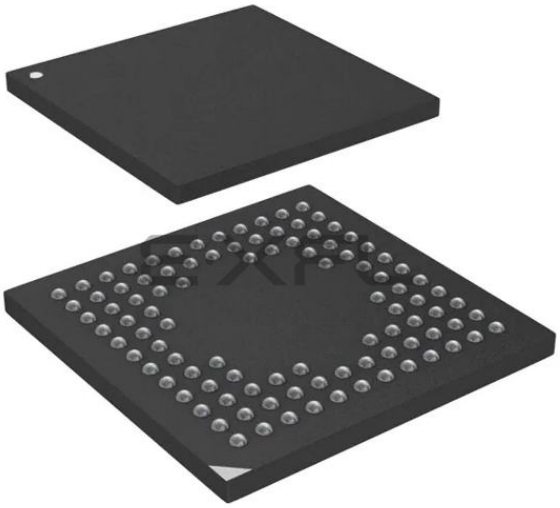

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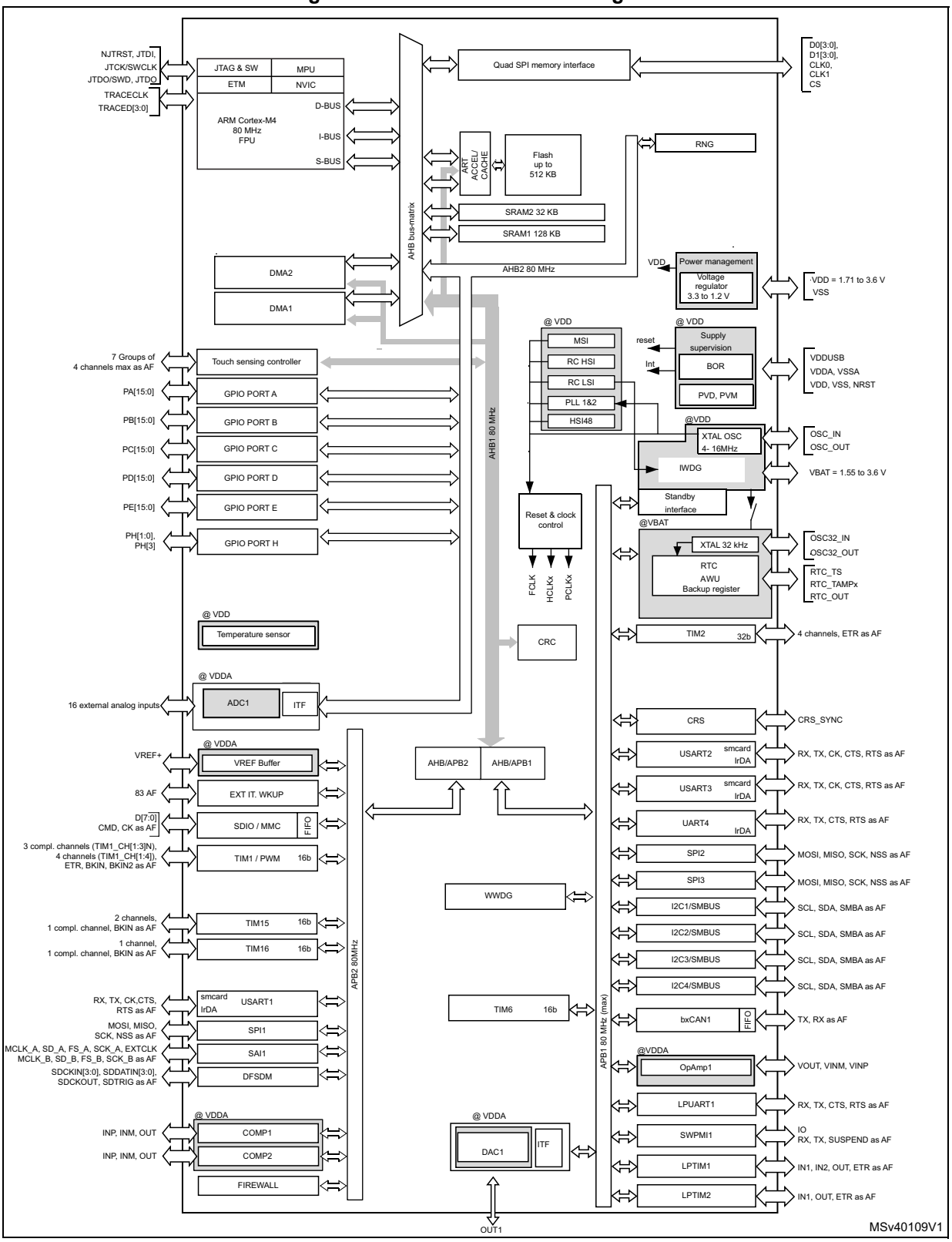
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451vci6

Table 2. STM32L451xx family device features and peripheral counts

Peripheral		STM32L451Vx		STM32L451Rx		STM32L451Cx	
Flash memory		256KB	512KB	256KB	512KB	256KB	512KB
SRAM		160KB					
Quad SPI		Yes					
Timers	Advanced control	1 (16-bit)					
	General purpose	2 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
	Low -power	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI	3					
	I^2C	4					
	USART UART LPUART	3 1 1					
	SAI	1					
	CAN	1					
	SDMMC	Yes				No	
RTC		Yes					
Tamper pins		3		2		2	
Random generator		Yes					
GPIOs Wakeup pins		83 5		52 4		38 3	
Capacitive sensing Number of channels		21		12		6	
12-bit ADC Number of channels		1 16		1 16		1 10	
12-bit DAC channels		1					
Internal voltage reference buffer		Yes		No			
Analog comparator		2					
Operational amplifiers		1					
Max. CPU frequency		80 MHz					
Operating voltage		1.71 to 3.6 V					

Figure 1. STM32L451xx block diagram



Note: AF: alternate function on I/O pins.

3.11 Clocks and startup

The clock controller (see *Figure 4*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **RC48 with clock recovery system (HSI48)**: internal RC48 MHz clock source can be used to drive the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Two PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the SDMMC/RNG and the SAI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
14	G6	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
15	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, DFSDM1_CKOUT, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
16	H6	22	G4	31	L4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
17	E5	23	H4	32	M4	PA7	I/O	FT_fa	-	TIM1_CH1N, TIM3_CH2, I2C3_SCL, SPI1_MOSI, DFSDM1_DATIN0, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
-	E4	24	H5	33	K5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC1_IN13
-	G5	25	H6	34	L5	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
18	H5	26	F5	35	M5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, SPI1_NSS, DFSDM1_CKIN0, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
19	F4	27	G5	36	M6	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
20	G4	28	G6	37	L6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, EVENTOUT	COMP1_INP
-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, SAI1_SD_B, EVENTOUT	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, SAI1_FS_B, EVENTOUT	-
-	-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, EVENTOUT	-
21	H4	29	G7	47	L10	PB10	I/O	FT_f	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
22	H3	30	H7	48	L11	PB11	I/O	FT_f	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, EVENTOUT	-

Table 17. Alternate function AF0 to AF7(1)

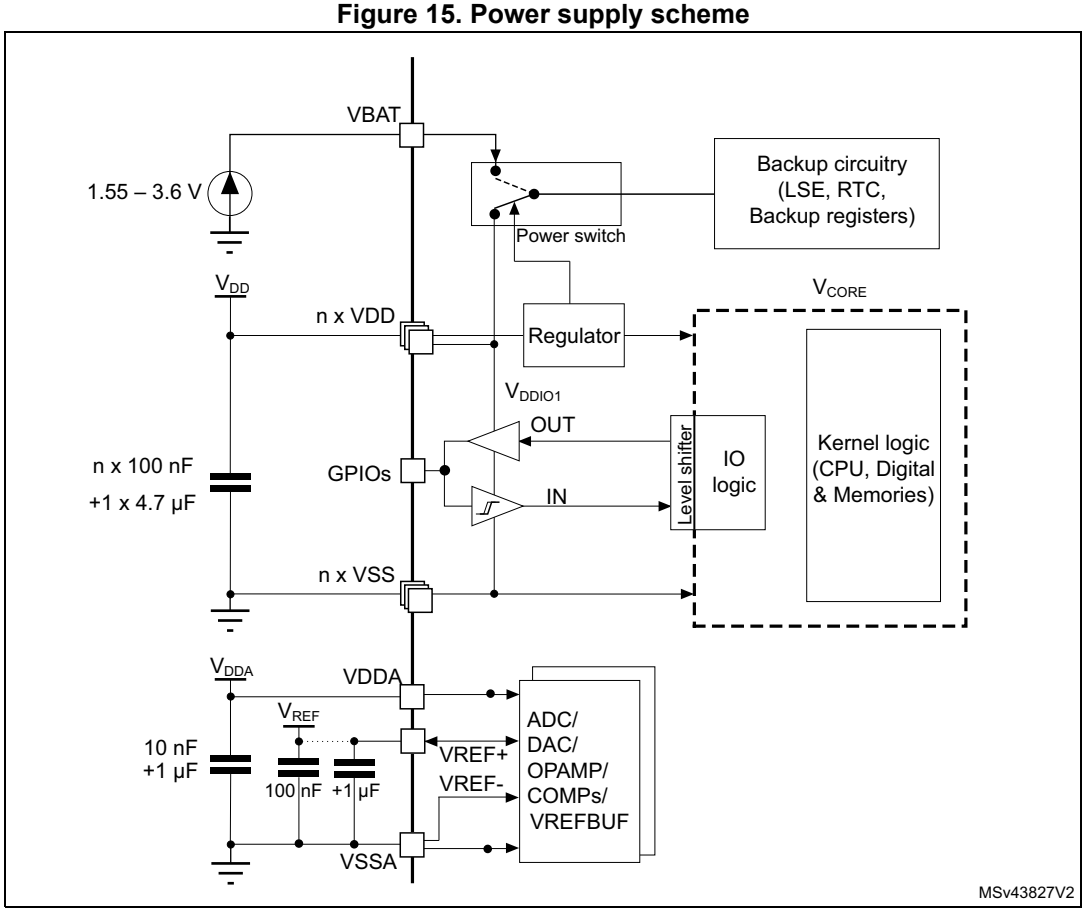
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	DFSDM1_ CKOUT	-
	PA6	-	TIM1_BKIN	TIM3_CH1	-	-	SPI1_MISO	COMP1_OUT	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	-	I2C3_SCL	SPI1_MOSI	DFSDM1_ DATIN0	-
	PA8	MCO	TIM1_CH1	-	-	-	-	DFSDM1_ CKIN1	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	DFSDM1_ DATIN1	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	COMP1_OUT	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS/SWDAT	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

Table 18. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port D	PD0	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PD2	-	TSC_SYNC	-	-	SDMMC1_ CMD	-	-	EVENTOUT
	PD3	-	-	QUADSPI_ BK2_NCS	-	-	-	-	EVENTOUT
	PD4	-	-	QUADSPI_ BK2_IO0	-	-	-	-	EVENTOUT
	PD5	-	-	QUADSPI_ BK2_IO1	-	-	-	-	EVENTOUT
	PD6	-	-	QUADSPI_ BK2_IO2	-	-	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	QUADSPI_ BK2_IO3	-	-	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	-	-	-	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	-	-	-	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	-	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	-	-	-	-	EVENTOUT
	PD15	-	-	-	-	-	-	-	EVENTOUT

6.1.6 Power supply scheme

Figure 15. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.35	2.40	2.50	2.65	3.00	2.65	2.75	2.90	3.20	3.75	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.75	1.95	2.20	2.80	
				8 MHz	0.815	0.845	0.940	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.465	0.495	0.595	0.760	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.320	0.420	0.580	0.910	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.205	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.745	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.45	8.50	8.65	8.90	9.25	9.45	9.50	9.75	10.10	10.75	
				72 MHz	7.65	7.70	7.85	8.05	8.45	8.50	8.60	8.80	9.15	9.85	
				64 MHz	6.80	6.85	7.00	7.20	7.60	7.60	7.70	7.90	8.25	8.90	
				48 MHz	5.10	5.15	5.25	5.45	5.85	5.70	5.80	6.00	6.35	7.00	
				32 MHz	3.45	3.50	3.60	3.80	4.20	3.85	3.95	4.15	4.50	5.15	
				24 MHz	2.60	2.65	2.80	2.95	3.35	2.95	3.05	3.20	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.50	2.00	2.10	2.30	2.60	3.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	225	260	365	550	900	275	335	470	770	1400	µA
				1 MHz	130	160	270	450	800	170	225	375	670	1300	
				400 kHz	73.0	99.5	205	385	735	105	165	325	600	1250	
				100 kHz	38.0	71.0	175	355	705	70	140	315	565	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 38. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (SRAM2)(3)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	250	730	2700	6350	13850	575	1800	6350	14500	32000	nA
			2.4 V	250	740	2700	6150	14000	620	1800	6450	14500	32000	
			3 V	255	740	2700	6450	13500	645	1850	6500	15000	32500	
			3.6 V	255	755	2800	6500	13500	790	1950	6500	15000	33000	
I_{DD_ALL} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (4).	3 V	2.00	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: I_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 42: Low-power mode wakeup timings*.

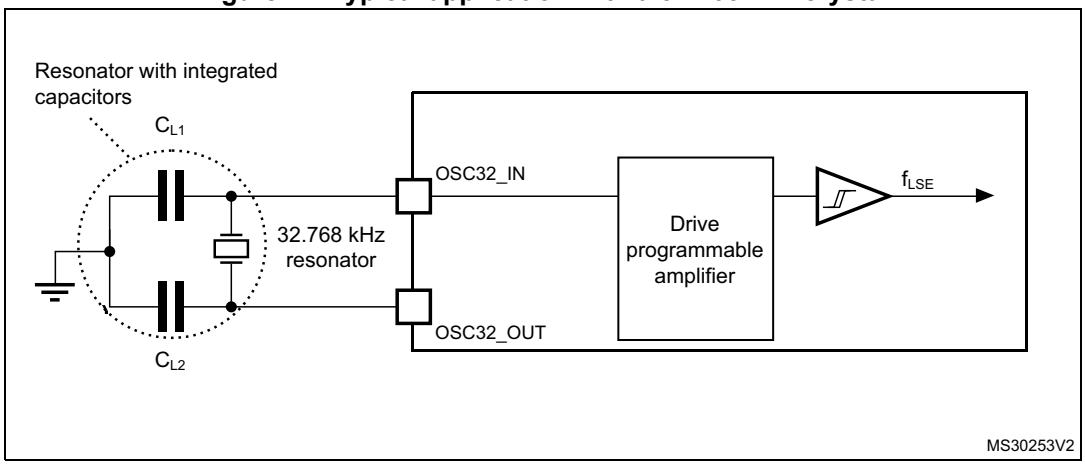
Table 39. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	19.0	120	720	2200	6400	38.0	350	2050	6350	19500	nA
			2.4 V	26.0	145	855	2600	7450	62.0	400	2400	7450	22500	
			3 V	37.0	185	1050	3100	8700	105	500	2850	8750	26000	
			3.6 V	67.0	260	1350	3950	11000	160	650	3500	10500	30000	

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 62. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 63*, respectively.

6.3.18 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 67* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 23: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 67. ADC characteristics(1) (2)

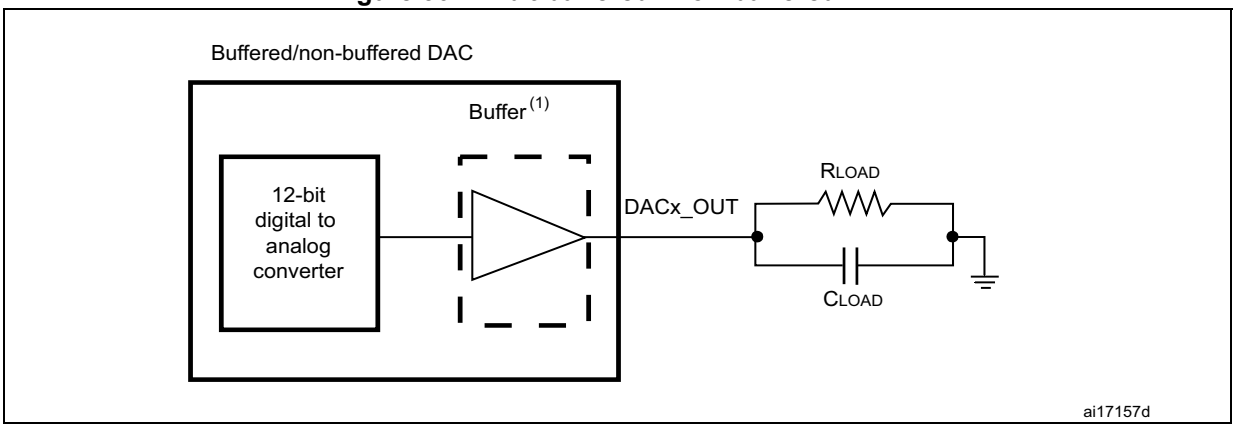
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	80	MHz
		Range 2	0.14	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	$(V_{REF+}+V_{REF-})/2$ - 0.18	$(V_{REF+}+V_{REF-})/2$	$(V_{REF+}+V_{REF-})/2$ + 0.18	V
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

Table 73. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 61: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0394 reference manual for more details.

Figure 30. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 75. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Table 77. OPAMP characteristics(1) (continued)

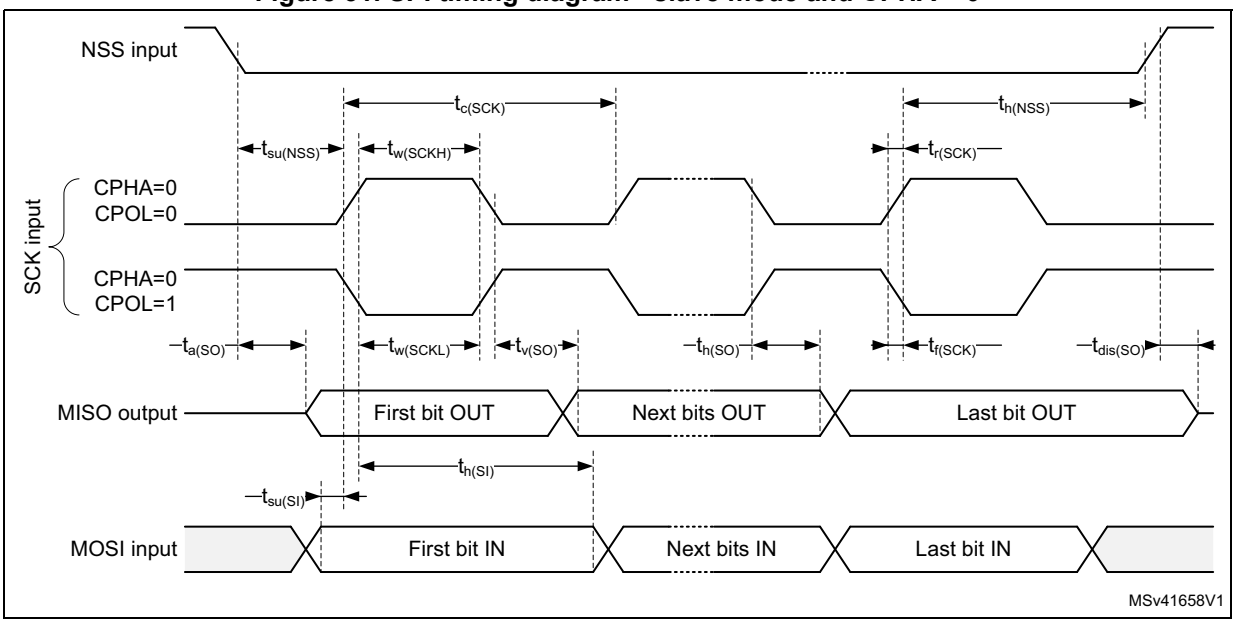
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Table 85. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	13.5	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	24	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

Figure 31. SPI timing diagram - slave mode and CPHA = 0



8 Ordering information

Table 101. STM32L451xx ordering information scheme

Example: STM32 L 451 C C T 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

451: STM32L451xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

C = 256 KB of Flash memory

E = 512 KB of Flash memory

Package

T = LQFP ECOPACK®2

U = QFN ECOPACK®2

I = UFBGA ECOPACK®2

Y = CSP ECOPACK®2

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.