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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l451vct6

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI or CAN.

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDA} = 1.62 V (ADC/COMPs) / 1.8 (DAC/OPAMP) / 2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, DAC, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with V_{DDIO1} = V_{DD}.

Table 4. STM32L451xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Run	MR range 1	Yes	ON[4]	ON	Any	All	N/A	94 µA/MHz	N/A
	MR range2					All except RNG		85 µA/MHz	
LPRun	LPR	Yes	ON[4]	ON	Any except PLL	All except RNG	N/A	95 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON[4]	ON[5]	Any	All	Any interrupt or event	27 µA/MHz	6 cycles
	MR range2					All except RNG		27 µA/MHz	
LPSleep	LPR	No	ON[4]	ON[5]	Any except PLL	All except RNG	Any interrupt or event	38 µA/MHz	6 cycles
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3)[6] UART4[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3)[6] UART4[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2)	125 µA	2.47 µs in SRAM 4.1 µs in Flash
	MR Range 2							125 µA	

Table 6. STM32L451xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DAC1 DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L451xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DAC and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 5. Voltage reference buffer

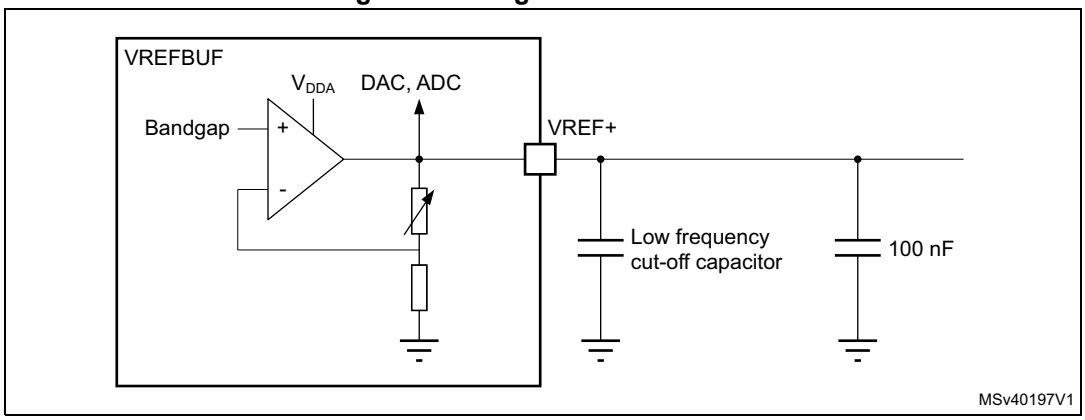


Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
14	G6	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
15	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, DFSDM1_CKOUT, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
16	H6	22	G4	31	L4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
17	E5	23	H4	32	M4	PA7	I/O	FT_fa	-	TIM1_CH1N, TIM3_CH2, I2C3_SCL, SPI1_MOSI, DFSDM1_DATIN0, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
-	E4	24	H5	33	K5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC1_IN13
-	G5	25	H6	34	L5	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
18	H5	26	F5	35	M5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, SPI1_NSS, DFSDM1_CKIN0, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
19	F4	27	G5	36	M6	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
20	G4	28	G6	37	L6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, EVENTOUT	COMP1_INP
-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, SAI1_SD_B, EVENTOUT	-

Table 16. STM32L451xx pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, SAI1_FS_B, EVENTOUT	-
-	-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, EVENTOUT	-
21	H4	29	G7	47	L10	PB10	I/O	FT_f	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
22	H3	30	H7	48	L11	PB11	I/O	FT_f	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, EVENTOUT	-

Table 18. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port E	PE0	-	-	-	-	-	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	-	-	-	-	EVENTOUT
	PE2	-	TSC_G7_IO1	-	-	-	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	-	-	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	-	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	-	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	-	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_ BK1_NCS	-	-	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_ BK1_IO0	-	-	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_ BK1_IO1	-	-	-	-	EVENTOUT
	PE14	-	-	QUADSPI_ BK1_IO2	-	-	-	-	EVENTOUT
	PE15	-	-	QUADSPI_ BK1_IO3	-	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 13*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 14*.

Figure 13. Pin loading conditions

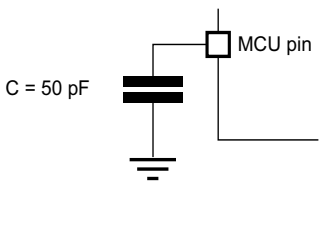


Figure 14. Pin input voltage

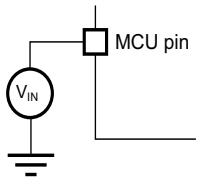


Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1) (2)	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.35	2.40	2.50	2.65	3.00	2.65	2.75	2.90	3.20	3.75	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.75	1.95	2.20	2.80	
				8 MHz	0.815	0.845	0.940	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.465	0.495	0.595	0.760	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.320	0.420	0.580	0.910	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.205	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.745	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.45	8.50	8.65	8.90	9.25	9.45	9.50	9.75	10.10	10.75	
				72 MHz	7.65	7.70	7.85	8.05	8.45	8.50	8.60	8.80	9.15	9.85	
				64 MHz	6.80	6.85	7.00	7.20	7.60	7.60	7.70	7.90	8.25	8.90	
				48 MHz	5.10	5.15	5.25	5.45	5.85	5.70	5.80	6.00	6.35	7.00	
				32 MHz	3.45	3.50	3.60	3.80	4.20	3.85	3.95	4.15	4.50	5.15	
				24 MHz	2.60	2.65	2.80	2.95	3.35	2.95	3.05	3.20	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.50	2.00	2.10	2.30	2.60	3.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	225	260	365	550	900	275	335	470	770	1400	µA
				1 MHz	130	160	270	450	800	170	225	375	670	1300	
				400 kHz	73.0	99.5	205	385	735	105	165	325	600	1250	
				100 kHz	38.0	71.0	175	355	705	70	140	315	565	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.75	2.80	2.90	3.10	3.40	3.15	3.25	3.40	3.70	4.30	mA
				16 MHz	1.95	2.00	2.10	2.25	2.60	2.25	2.30	2.50	2.75	3.35	
				8 MHz	1.10	1.15	1.25	1.40	1.75	1.25	1.35	1.50	1.75	2.35	
				4 MHz	0.640	0.670	0.765	0.935	1.25	0.75	0.80	0.95	1.25	1.80	
				2 MHz	0.380	0.405	0.505	0.670	1.00	0.45	0.50	0.65	0.95	1.50	
				1 MHz	0.250	0.275	0.375	0.540	0.865	0.30	0.35	0.50	0.80	1.35	
				100 kHz	0.135	0.160	0.255	0.420	0.750	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.85	8.90	9.05	9.30	9.70	10.0	10.5	10.5	11.0	11.5	
				72 MHz	8.00	8.05	8.20	8.40	8.85	9.05	9.15	9.35	9.70	10.5	
				64 MHz	7.90	7.95	8.10	8.35	8.75	8.95	9.10	9.35	9.70	10.5	
				48 MHz	6.60	6.65	6.80	7.05	7.45	7.55	7.65	7.90	8.30	9.00	
				32 MHz	4.75	4.80	4.95	5.15	5.55	5.40	5.50	5.75	6.10	6.80	
				24 MHz	3.60	3.65	3.80	4.00	4.35	4.10	4.20	4.40	4.75	5.40	
				16 MHz	2.60	2.65	2.75	2.95	3.35	3.00	3.05	3.25	3.60	4.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	340	360	470	650	1000	400	455	575	880	1550	µA
				1 MHz	175	215	320	500	855	225	285	420	720	1350	
				400 kHz	89.5	120	225	405	760	130	185	340	620	1250	
				100 kHz	42.5	75.5	180	360	715	75	145	320	575	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	76.5	105	220	410	740	110	175	350	600	1250	µA
				1 MHz	54.0	81.0	195	385	715	81.5	155	325	570	1200	
				400 kHz	28.0	64.5	175	370	695	60.5	130	305	555	1200	
				100 kHz	21.5	55.0	170	360	690	58.5	120	300	550	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 35. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	2.05	5.40	19.0	44.0	97.0	4.00	11.5	41.5	100	220	µA
			2.4 V	2.10	5.45	19.0	44.5	98.5	4.05	11.5	42.0	100	225	
			3 V	2.05	5.55	19.5	45.0	100	4.10	12.0	43.0	105	230	
			3.6 V	2.05	5.65	20.0	46.5	105	4.20	12.0	44.0	105	235	
I_{DD_ALL} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	2.30	5.65	19.0	44.0	97.0	4.50	12.0	42.0	100	220	µA
			2.4 V	2.35	5.80	19.5	44.5	99.0	4.65	12.0	42.5	100	225	
			3 V	2.50	5.90	20.0	45.5	100	4.90	12.5	43.5	105	230	
			3.6 V	2.60	6.15	20.5	47.0	105	5.20	13.0	44.5	105	235	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	2.60	6.05	21.0	48.0	97.0	-	-	-	-	-	
			2.4 V	2.55	6.20	21.0	49.0	98.5	-	-	-	-	-	
			3 V	2.80	6.35	21.5	49.5	100	-	-	-	-	-	
			3.6 V	2.85	6.60	22.5	51.5	105	-	-	-	-	-	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	2.40	5.70	19.0	44.5	98.0	-	-	-	-	-	
			2.4 V	2.50	5.85	19.5	45.0	99.5	-	-	-	-	-	
			3 V	2.60	6.00	20.0	46.0	100	-	-	-	-	-	
			3.6 V	2.65	6.25	20.5	47.0	105	-	-	-	-	-	

Table 42. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	3.34	4.3	µs
			Wakeup clock HSI16 = 16 MHz	3.7	6.5	
		Range 2	Wakeup clock MSI = 24 MHz	3.8	7.1	
			Wakeup clock HSI16 = 16 MHz	3.7	6.5	
			Wakeup clock MSI = 4 MHz	9.3	7.1	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.85	2.7	
			Wakeup clock HSI16 = 16 MHz	2.68	3	
		Range 2	Wakeup clock MSI = 24 MHz	2.47	3.4	
			Wakeup clock HSI16 = 16 MHz	2.68	3	
			Wakeup clock MSI = 4 MHz	9.67	12.5	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.75	7.6	µs
			Wakeup clock HSI16 = 16 MHz	7.14	8	
		Range 2	Wakeup clock MSI = 24 MHz	7	7.82	
			Wakeup clock HSI16 = 16 MHz	7.14	7.9	
			Wakeup clock MSI = 4 MHz	10.44	11.9	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.21	5.9	
			Wakeup clock HSI16 = 16 MHz	6.23	6.9	
		Range 2	Wakeup clock MSI = 24 MHz	5.73	6.4	
			Wakeup clock HSI16 = 16 MHz	6.23	6.9	
			Wakeup clock MSI = 4 MHz	10.9	12.3	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	16.05	19.2	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			17.06	20.3	

6.3.10 Flash memory characteristics

Table 54. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 55. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 69. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 74. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 77. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

6.3.24 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 80. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 Timer characteristics

The parameters given in the following tables are guaranteed by design.

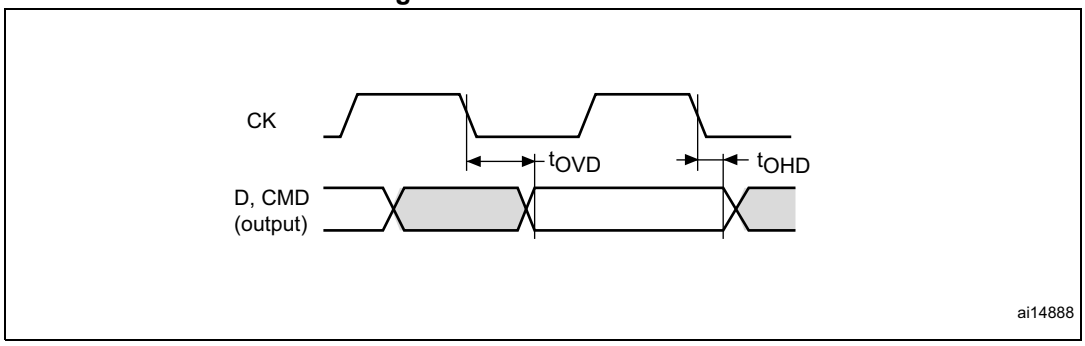
Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 81. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Figure 39. SD default mode



CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).