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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx508cvk1b

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The system includes four PLLs.
CSPI eCSPI-1 eCSPI-2	Configurable SPI, Enhanced CSPI	Slave Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
DAP TPIU CTI	Debug System	System Control Peripherals	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. Debug access port (DAP)—The DAP provides real-time access for the debugger without halting the core to System memory and peripheral registers. All debug configuration registers and Debugger access to JTAG scan chains.
DRAM MC	DRAM Memory Controller	External Memory Interface	The DRAM MC consists of a DRAM memory controller and PHY, supporting LPDDR2, DDR2, and LPDDR1 memories with clock frequencies up to 266 MHz with 32-bit interface. It is tightly linked with the system bus fabric and employs advanced arbitration mechanism to maximize DRAM bandwidth efficiency.
EIM	Static Memory Controller	External Memory Interface	The EIM is an external static memory and generic host interface. It supports up to a 32-bit interface (through pin-muxing) or a dedicated 16-bit muxed interface. It can be used to interface to PSRAMs (sync and async), NOR-flash or any external memory mapped peripheral.
BCH32/GPMI2	Raw NAND System with ECC	RawNAND and SSP Peripherals	The i.MX50 contains a fully hardware accelerated raw NAND flash solution supporting SLC and MLC devices. The system consists of the GPMI2 module, which is driven by the APBH DMA engine to perform the NAND flash interface function (supporting up to ONFI2.1). Coupled with the GPMI2 is the BCH32 hardware error-correction engine which is an AXI bus-master and supports up to 32-bits of correction over block sizes up to 1 Kbyte (that is, supports up to 2 Kbyte code-size).
System Fabric and QoS	System Fabric and QoS	System Peripherals	In order to aggregate the multitude of masters and memory mapped devices, the i.MX50 contains a next-generation AMBA3 AXI bus fabric. In addition, the i.MX50 contains a Quality of Service Controller IP (QoSC) which allows both soft priority control and dynamic priority elevation. Software priority control works for all masters but dynamic hardware control only works for EPDC and eLCDIF.
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit *set and forget* timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.

- All other supply voltages at nominal levels
- External (MHz) crystal and on-chip oscillator disabled
- CKIL input ON with 32 kHz signal present
- All PLLs OFF, all CCM-generated clocks OFF
- All modules disabled
- No external resistive loads that cause current

4.1.6 USB-OH-1 (OTG + 1 Host Port) Current Consumption

Table 16 shows the USB interface current consumption.

Table 16. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full speed	RX	5.5	6	mA
		TX	7	8	
	High speed	RX	5	6	
		TX	5	6	
Analog supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full speed	RX	6.5	7	mA
		TX	6.5	7	
	High speed	RX	12	13	
		TX	21	22	
Digital supply VCC (1.2 V)	Full speed	RX	6	7	mA
		TX	6	7	
	High speed	RX	6	7	
		TX	6	7	

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX50 processor (worst-case scenario)

[1] Vin(dc) specifies the allowable dc excursion of each differential input.

[2] Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “pure” input level and Vcp is the “complementary” input level. the minimum value is equal to Vih(dc) - Vil(dc).

[3] Typ condition: typ model, 1.8 V, and 25 °C. Max condition: BCS model, 1.9 V, and 105 °C. Min condition: WCS model, 1.7 V, and -20 °C.

4.3.5 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 21 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 21. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec’ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.35	0.62 1.27	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	µA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	µA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	µA

4.5.3 LVIO I/O Slow AC Parameters

Table 26 shows the AC parameters for LVIO slow I/O.

Table 28. LVIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.97/1.57 3.12/2.70	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.29/1.87 3.79/3.44	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.93/2.48 5.42/4.98	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.92/4.57 10.64/9.85	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.50/0.63 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.53 0.26/0.29			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.40 0.18/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.10			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns
Output Pad di/dt (High Drive)	tdit				24	mA/ns
Output Pad di/dt (Medium drive)	tdit				16	mA/ns
Output Pad di/dt (Low drive)	tdit				8	mA/ns
Input Transition Times[2]	trm				25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

Table 36. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 37 shows the electrical parameters of CAMP.

Table 37. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 38 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 38. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

4.6.5.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

The following diagrams show the write and read timing of Source Synchronous Mode.

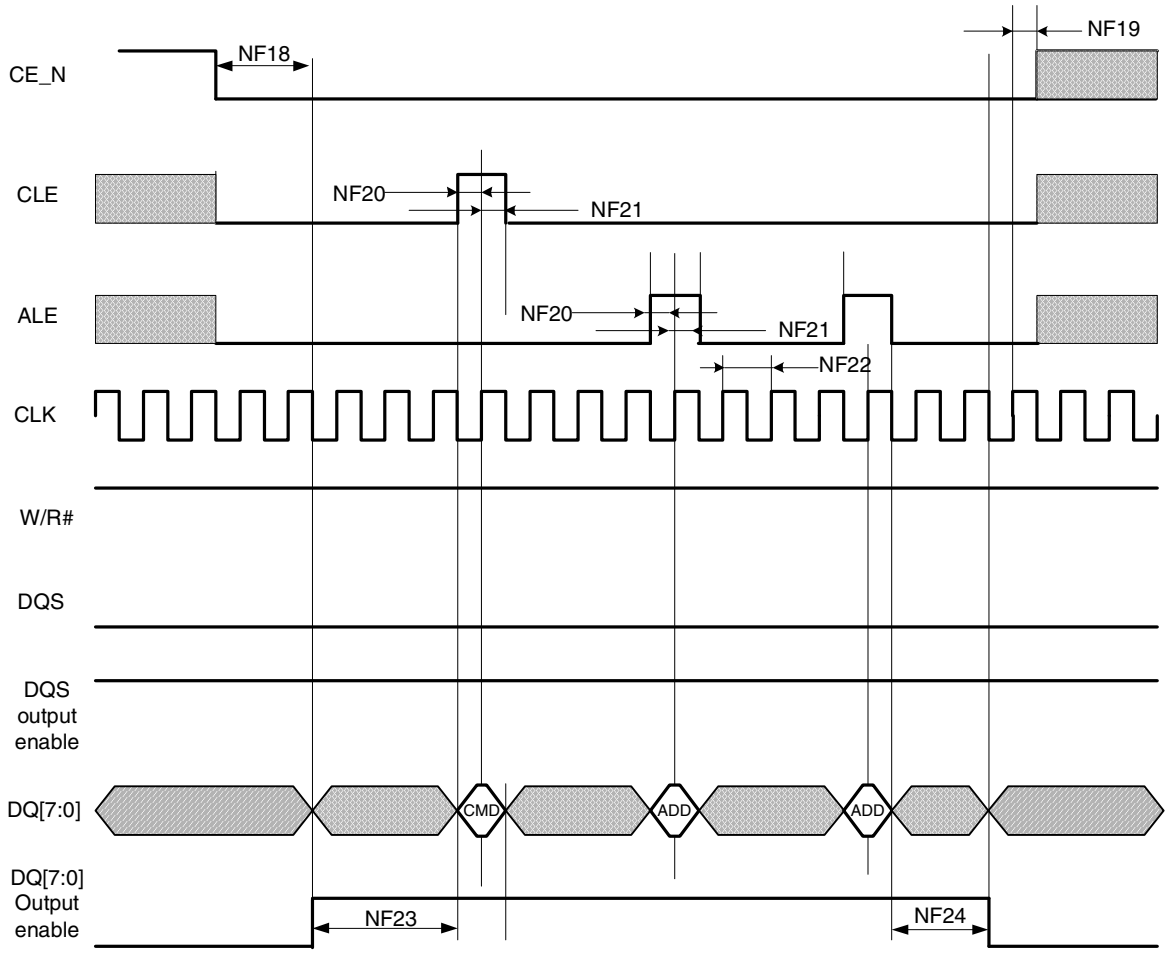

Figure 12. Source Synchronous Mode Command and Address Timing Diagram

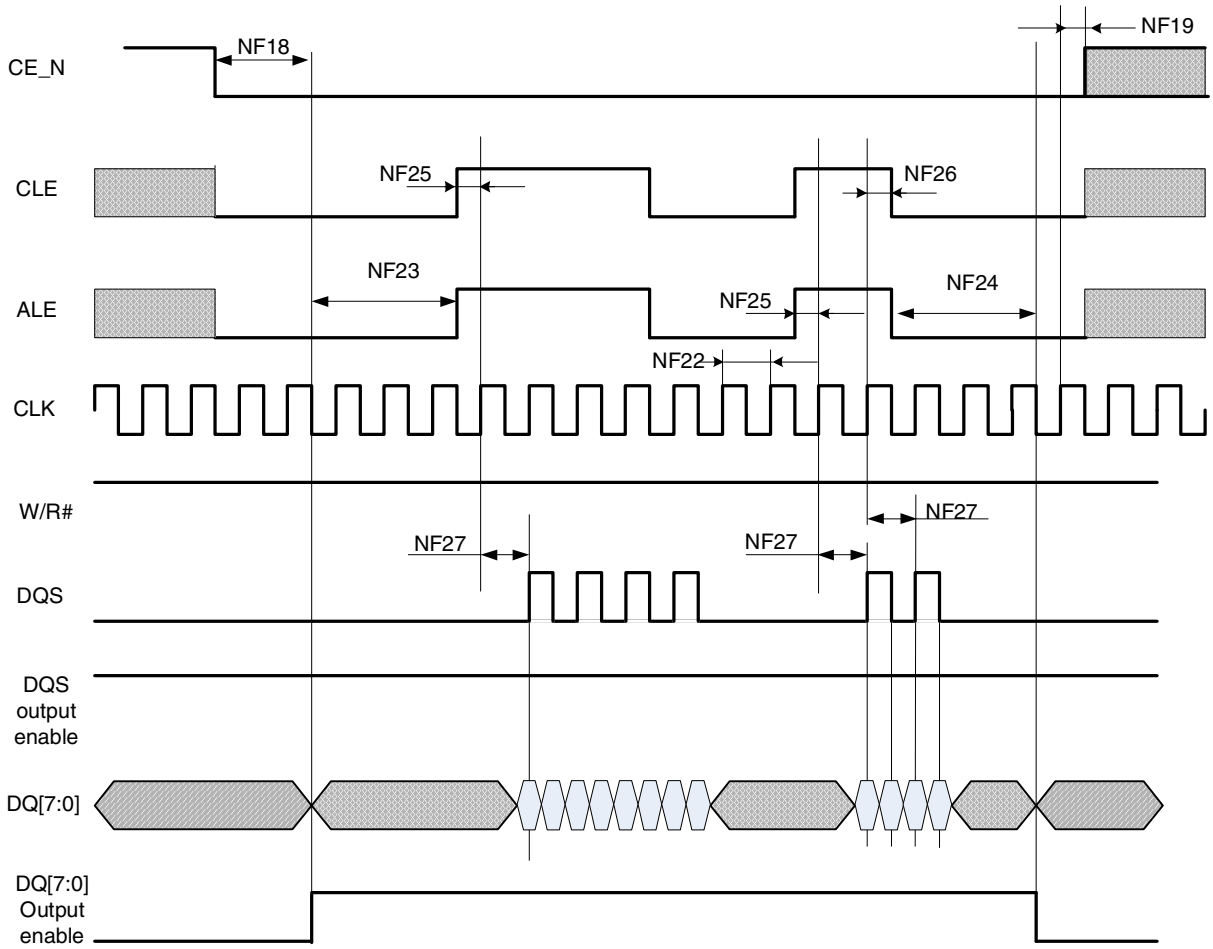

Figure 13. Source Synchronous Mode Data Write Timing Diagram

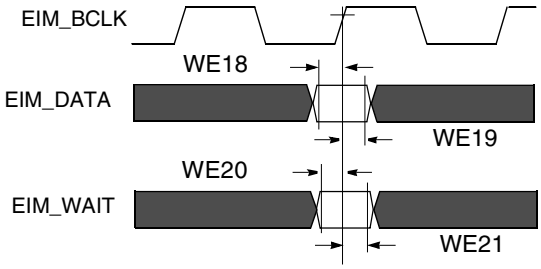

Figure 18. EIM Inputs Timing Diagram

Table 42. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

[1] *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

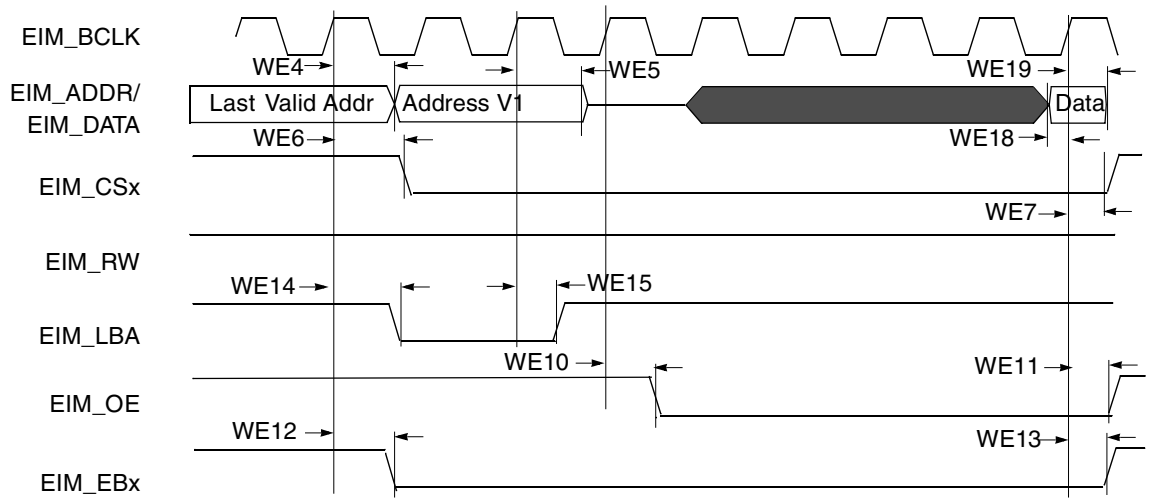

Figure 24. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=2

Figure 25, Figure 26, Figure 27, and Table 43 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

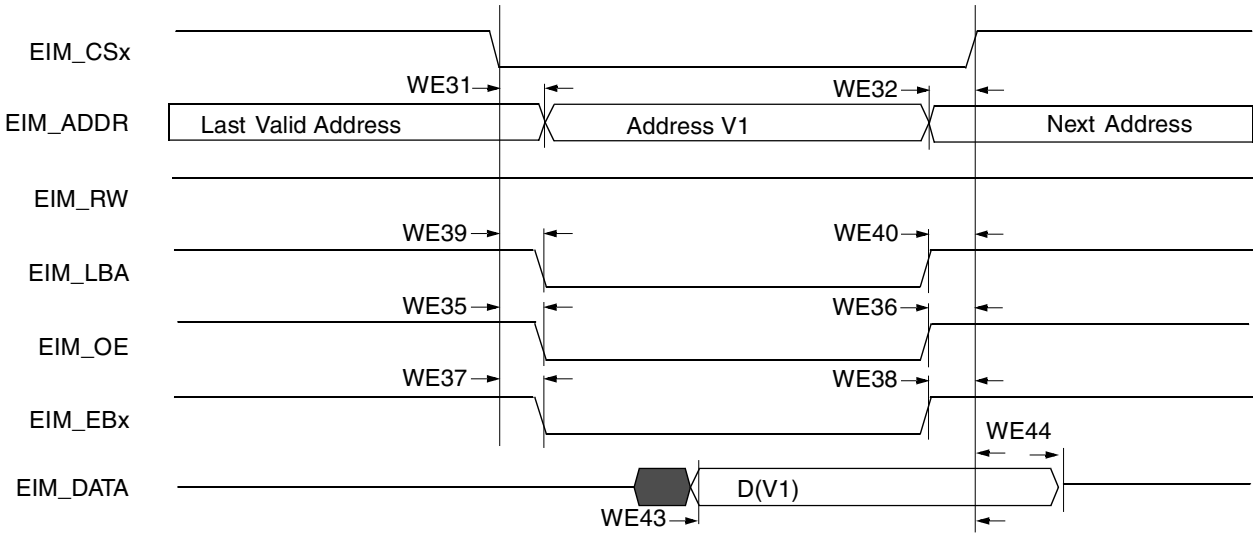

Figure 25. Asynchronous Memory Read Access

4.8.2 DRAM Command and Address Output Timing—LPDDR2

The following diagrams and tables specify the timings related to the address and command pins, which interface LPDDR2 memory devices.

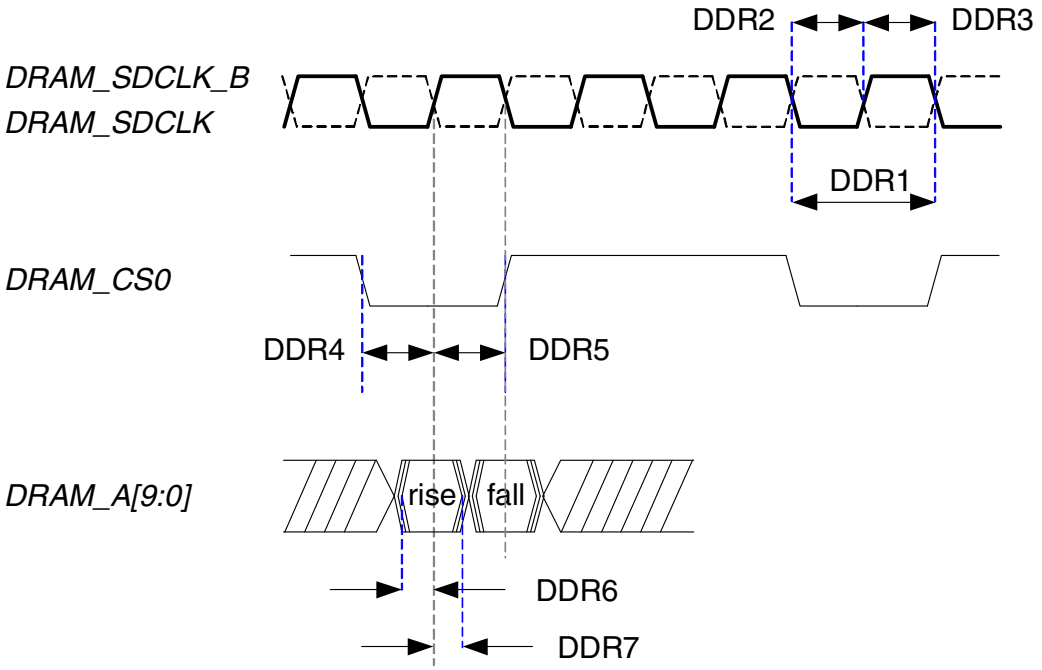

Figure 29. DRAM Command/Address Output Timing—LPDDR2

Table 45. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Control output hold time	tIH	0.5 tCK - 0.3	—	ns
DDR6 CK >= 200 MHz	Address output setup time	tIS	0.5 tCK - 1.3	—	ns
DDR7 CK >= 200 MHz	Address output hold time	tIH	0.5 tCK - 1.3	—	ns
DDR6 CK < 200 MHz	Address output setup time	tIS	1	—	ns
DDR7 CK < 200 MHz	Address output hold time	tIH	1	—	ns

4.9.2.4 eCSPI Slave Mode Timing

Figure 35 depicts the timing of eCSPI in slave mode and Table 52 lists the eCSPI slave mode timing characteristics.

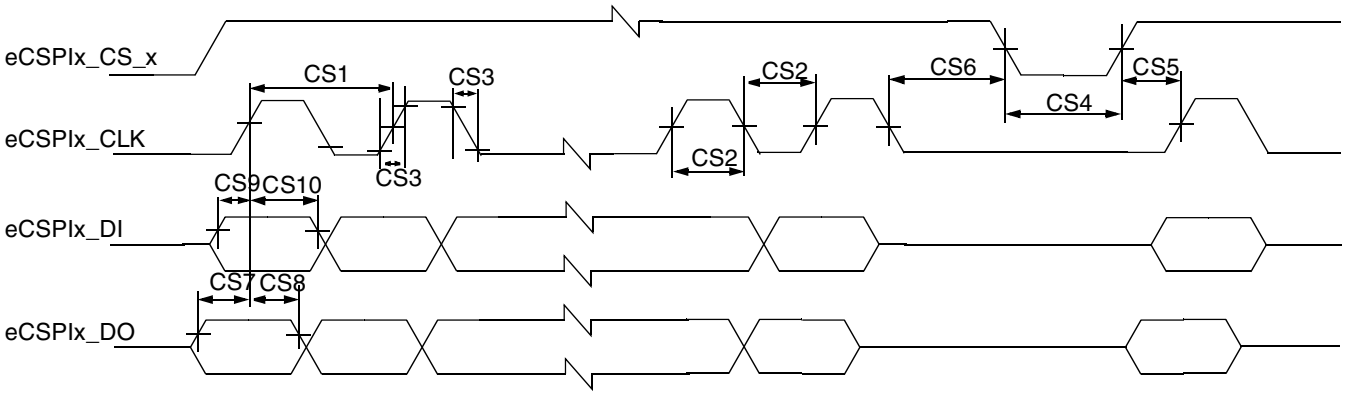

Figure 35. eCSPI Slave Mode Timing Diagram

Table 52. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

Table 59. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—[1]	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High (includes recovery time)	t_{RSTH}	480	512	—	µs

[1] In order not to mask signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

Figure 43 depicts Write 0 Sequence timing, and Table 60 lists the timing parameters.

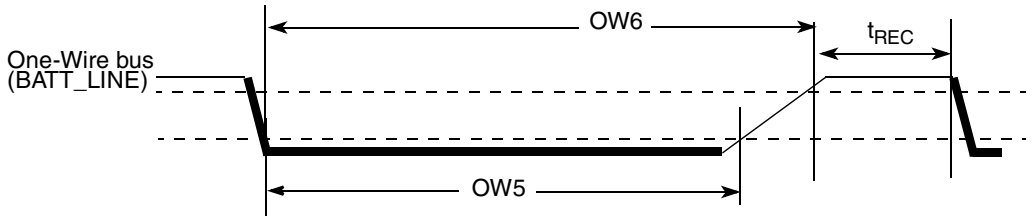

Figure 43. Write 0 Sequence Timing Diagram

Table 60. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
—	Recovery time	t_{REC}	1	—	—	µs

Figure 44 depicts Write 1 Sequence timing, Figure 45 depicts the Read Sequence timing, and Table 61 lists the timing parameters.

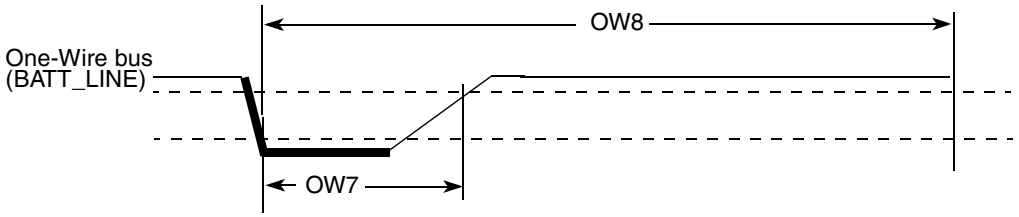

Figure 44. Write 1 Sequence Timing Diagram

4.9.9 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 64.

Table 64. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External— AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O through IOMUX
AUDMUX port 5	AUD5	External—EIM or SD1 I/O through IOMUX
AUDMUX port 6	AUD6	External—EIM or DISP2 through IOMUX

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.9.10.2.1 UART Transmitter

Figure 55 depicts the transmit timing of UART in the RS-232 serial mode with 8 data bit/1 stop bit format. Table 70 lists the UART RS-232 serial mode transmit timing characteristics.

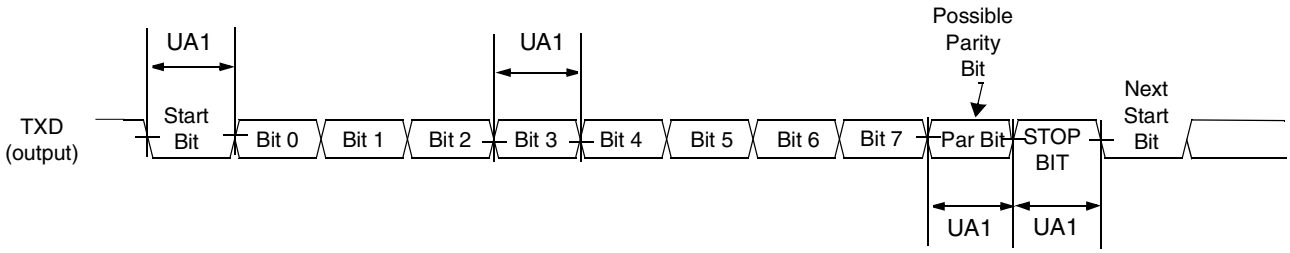

Figure 55. UART RS-232 Serial Mode Transmit Timing Diagram

Table 70. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.10.2.2 UART Receiver

Figure 56 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 71 lists serial mode receive timing characteristics.

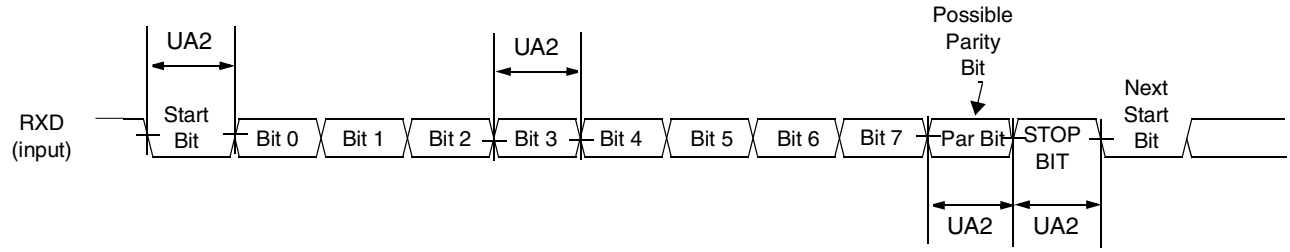

Figure 56. UART RS-232 Serial Mode Receive Timing Diagram

Table 71. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.9.10.3 UART IrDA Mode Timing

The following sections give the UART transmit and receive timings in IrDA mode.

Table 78. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

AA	Y	W	V	U	T	R
NVCC_SRTC	CKIL	PMIC_ON_REQ	SD2_D2	SD2_CLK	SD2_D0	SD1_CMD
NGND_SRTC	ECKIL	PMIC_STBY_REQ	SD2_D3	SD2_D5	SD2_D1	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TDI	JTAG_TMS	JTAG_TCK	SD2_D4	SD2_D6	SD2_CD	SD1_D2
JTAG_TRSTB	VDD_DCDCO	GND_DCDC	SD2_CMD	SD2_D7	SD2_WP	SD1_D3
CKIH	VDD_DCDCI	NC	NC	NC	NC	NC
GND_KEL	USB_OTG_GPANAIO	NC	JTAG_MOD	JTAG_TDO	NVCC_SD1	NVCC_SPI
USB_OTG_RREFEXT	USB_OTG_ID	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI
VSS	USB_OTG_VBUS	NC	NVCC_NANDF	NVCC_JTAG	NC	NC
USB_H1_RREFEXT	USB_H1_VBUS	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC
VSS	USB_H1_GPANAIO	NC	CHGR_DET_B	NVCC_LCD	NC	VSS
DISP_D0	DISP_D1	NC	DISP_D11	VSS	NC	VSS
DISP_D2	DISP_D3	NC	DISP_D12	VSS	NC	VSS
DISP_D4	DISP_D5	NC	DISP_D13	VSS	NC	VSS
DISP_D6	DISP_D7	NC	DISP_D14	VSS	NC	VDDAL1
DISP_D8	DISP_D9	NC	DISP_D15	VSS	NC	NC
SD3_D3	DISP_D10	NC	VSS	VSS	VSS	VDDA
SD3_D4	SD3_D5	NC	VSS	VSS	VSS	DRAM_SDODT1
SD3_D6	SD3_D7	NC	NC	NC	NC	NC
DRAM_A4	DRAM_A2	DRAM_A0	VSS	DRAM_SDCKE	DRAM_SDCLK_1	DRAM_SDCLK_1_B
NVCC_EMI_DRAM	DRAM_A3	DRAM_A1	VSS	DRAM_CS1	DRAM_CS0	NVCC_EMI_DRAM
NC	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	DRAM_D1	DRAM_D2	VSS	DRAM_D5	DRAM_D6	NVCC_EMI_DRAM
NVCC_EMI_DRAM	DRAM_D0	DRAM_D3	DRAM_D4	DRAM_D7	DRAM_DQM0	NVCC_EMI_DRAM
AA	Y	W	V	U	T	R

Table 78. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 79. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

5.3.1 400 MAPBGA 17 x 17 mm Package Views

Figure 65 shows the top view of the 17 x 17 mm package, Figure 66 shows the bottom view of the package, and Figure 67 shows the side view of the package.

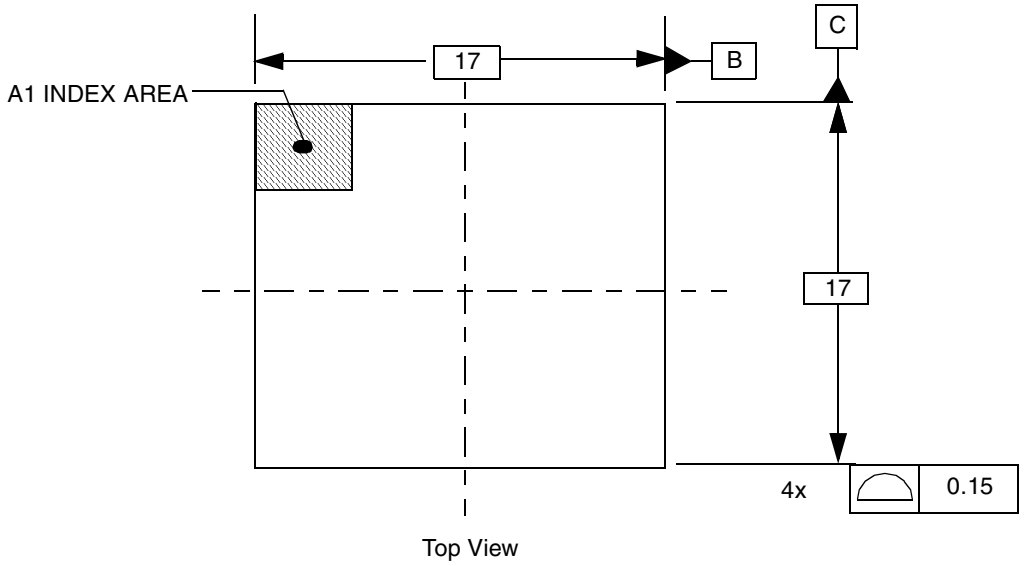

Figure 65. 400 MAPBGA 17x17 mm Package Top view

Table 84. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TDI	AA4	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	V4	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TRSTB	AA5	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	A9	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	A10	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	B9	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	B10	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	A8	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	B8	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	D7	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	A7	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	D12	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	D11	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	D10	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	M1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	N1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	P2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	N2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	M2	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	R4	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	J4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	E1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	G1	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	D1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	D2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper

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