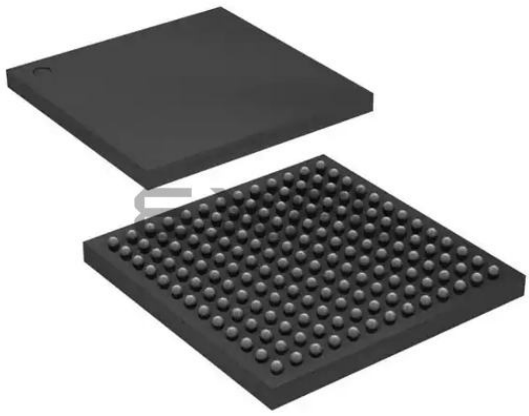


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	116
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA, WLCSP
Supplier Device Package	169-WLCSP (5.5x5.63)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk65fx1m0cac18r

Table of Contents

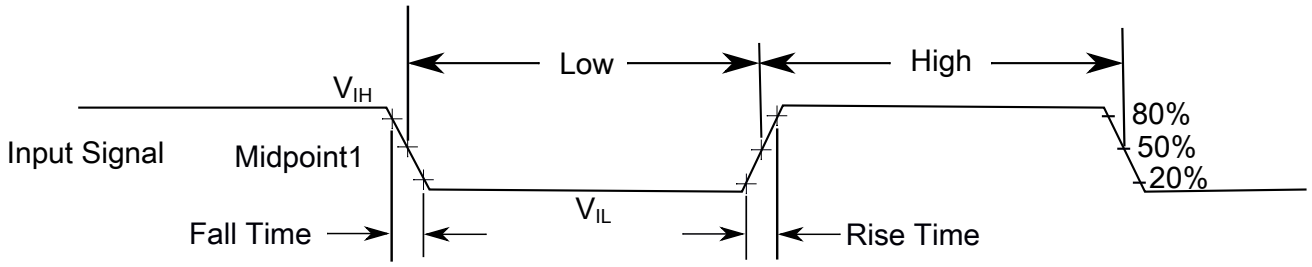
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital[1] input voltage,including RESET_b	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1] input voltage, including EXTAL32 and XTAL32	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	–0.3	3.63	V
V_{USB1_VBUS}	USB1_VBUS detect voltage	–0.3	6.0	V
VREG_IN0, VREG_IN1	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Digital pins have a general purpose I/O port assigned (e.g. PTA0). Analog pins do not have an associated general purpose I/O port.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

1. Measured at VDD=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100MHz
- Bus clock = 50MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 –> RUN	—	172	µs	
	• VLLS1 –> RUN	—	172	µs	
	• VLLS2 –> RUN	—	94	µs	
	• VLLS3 –> RUN	—	94	µs	
	• LLS2 –> RUN	—	5.8	µs	
	• LLS3 –> RUN	—	5.8	µs	
	• VLPS –> RUN	—	5.4	µs	
	• STOP –> RUN	—	5.4	µs	

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	µA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.						nA
	VLLS1	440	490	540	560	570	
	VLLS3	440	490	540	560	570	
	LLS2	490	490	540	560	570	
	LLS3	490	490	540	560	570	
	VLPS	510	560	560	560	610	
	STOP	510	560	560	560	610	
I_{48MIRC}	48MHz IRC	511	520	545	556	563	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.						µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	µA

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	0.847	1.48	µA	
	• @ 70°C	—	6.5	11.31	µA	
	• @ 85°C	—	16.2	28.31	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	0.551	.65	µA	
	• @ 70°C	—	6.3	7.12	µA	
	• @ 85°C	—	17.1	20.02	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.254	0.445	µA	
	• @ 70°C	—	6.3	10.99	µA	
	• @ 85°C	—	15.8	27.58	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	µA	
	• @ 70°C	—	0.49	0.64	µA	
	• @ 85°C	—	1.11	1.4	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					14
	• @ 1.8V					
	• @ –40 to 25°C	—	0.68	0.8	µA	
	• @ 70°C	—	1.2	1.56	µA	
	• @ 3.0V					
	• @ –40 to 25°C	—	0.81	0.96	µA	
	• @ 70°C	—	1.45	1.89	µA	
	• @ 85°C	—	2.5	3.46	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. MCG configured for PEE mode.
6. 168 MHz core and system clock, 56 MHz bus and FlexBus clock, and 28 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
7. 168 MHz core and system clock, 56 MHz bus and FlexBus clock, and 28 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
8. Max values are measured with CPU executing DSP instructions.
9. 120 MHz core and system clock, 60MHz bus clock, and FlexBus. MCG configured for PEE mode.

Table 20. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	1808	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	12.6	ns	
FB3	Address, data, and control output hold	1.0	—	ns	1
FB4	Data and FB_TA input setup	12.5	—	ns	
FB5	Data and FB_TA input hold	0	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

3. D7 and D8 are for write cycles only.

Table 30. SDRAM Timing (Limited voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.1	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	11.3	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	11.1	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 60 MHz
3. D7 and D8 are for write cycles only.

Following figure shows an SDRAM write cycle.

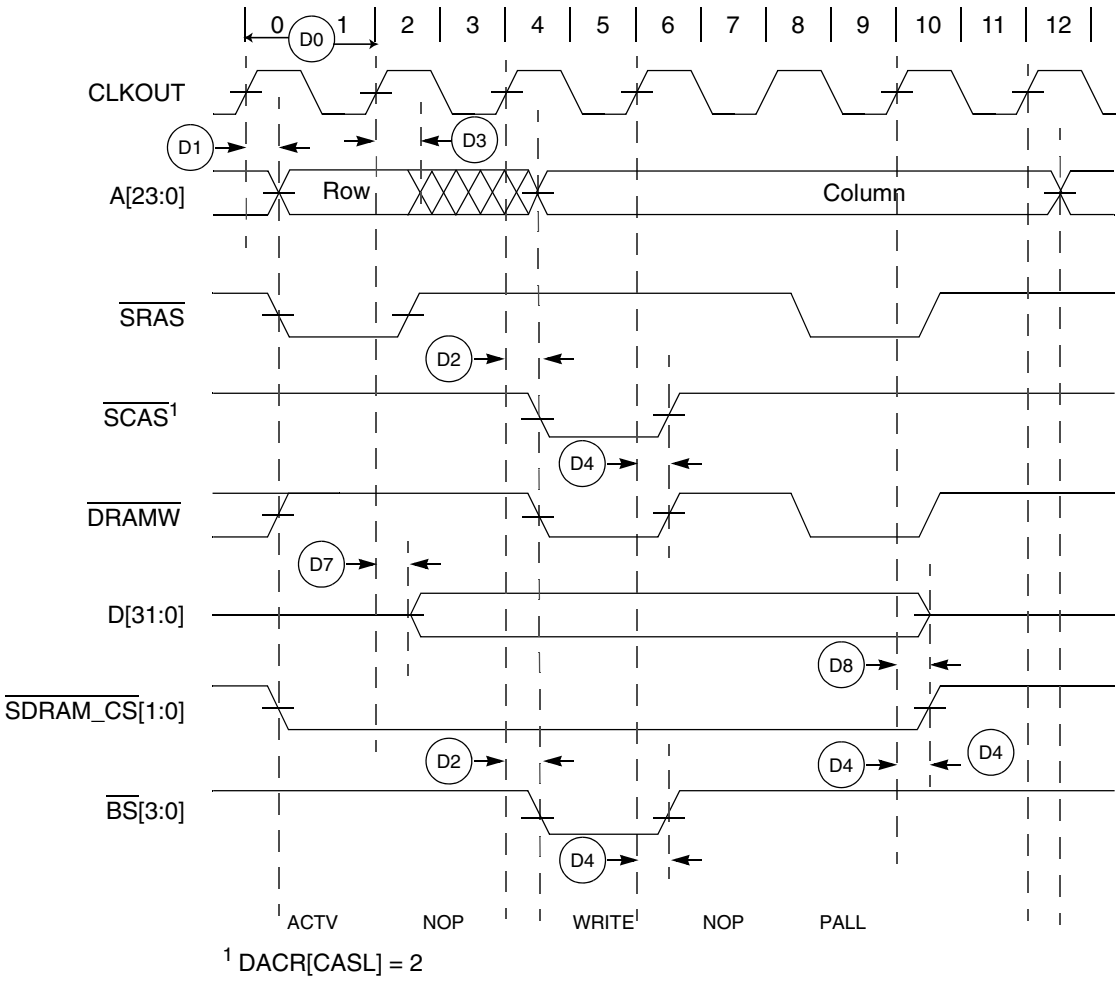


Figure 16. SDRAM read timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 1 and Table 32 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

Table 32. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

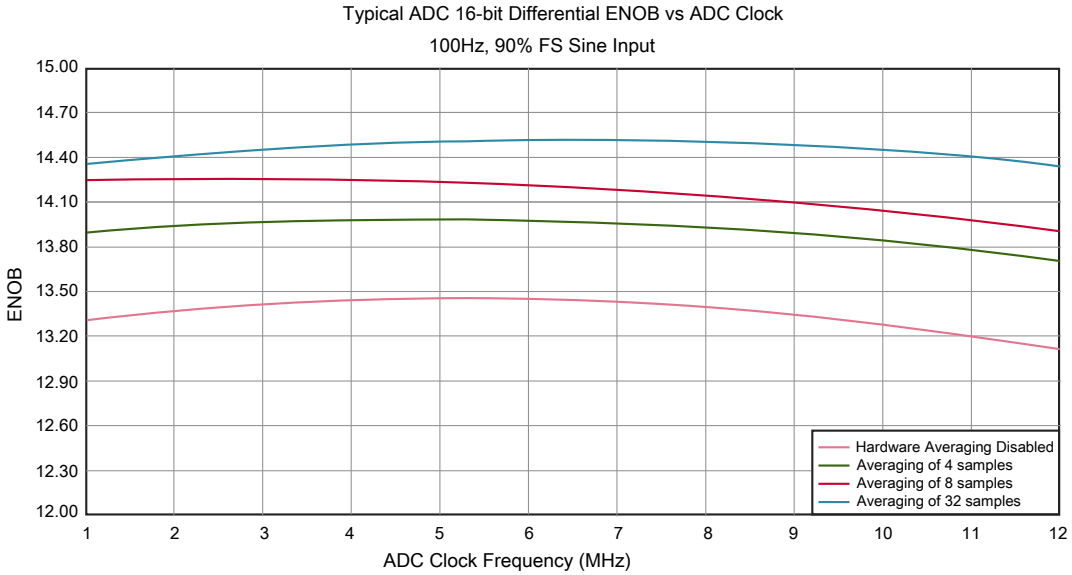


Figure 18. Typical ENOB vs. ADC_CLK for 16-bit differential mode

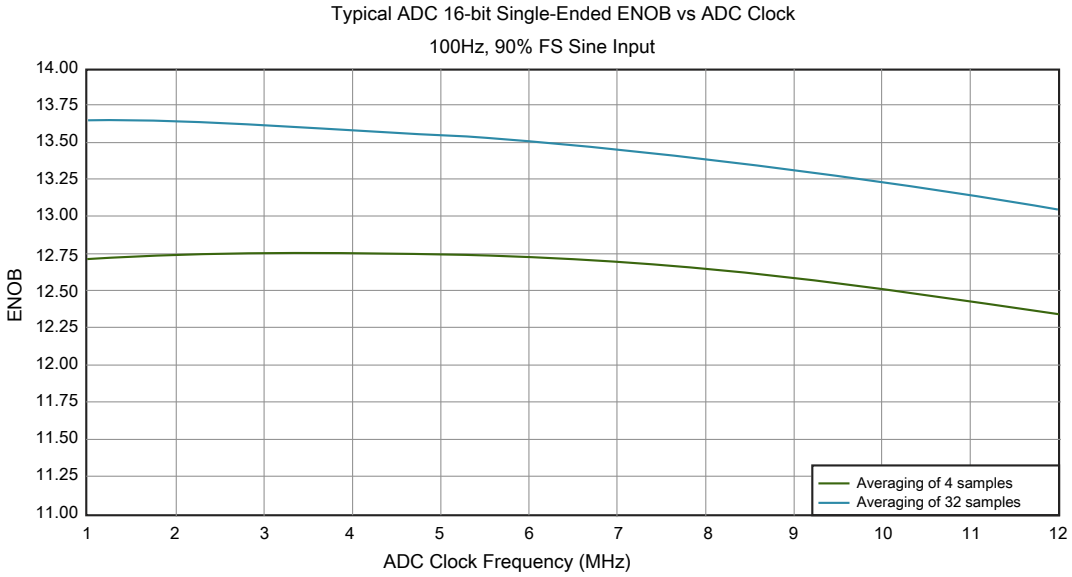


Figure 19. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.8.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 40. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	Operating Voltage	2.7	3.6	V
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

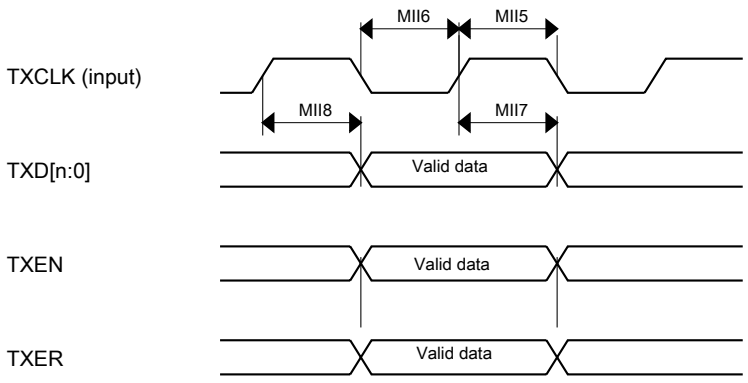


Figure 24. RMII/MII transmit signal timing diagram

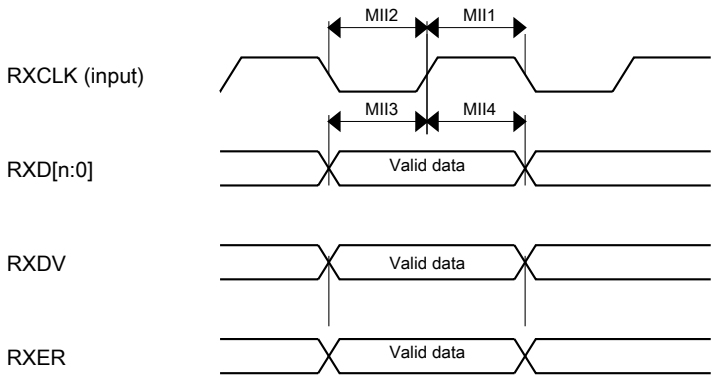


Figure 25. RMII/MII receive signal timing diagram

3.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 41. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	Operating Voltage	2.7	3.6	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 41. RMII signal switching specifications (continued)

Num	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15.4	ns

3.8.2 USB Voltage Regulator Electrical Specifications

Table 42. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREG_IN0 VREG_IN1	Regulator selectable input supply voltages	2.7	—	5.5	V	2
I_{DDon} VREG_IN0 VREG_IN1	Quiescent current — Run mode, load current equal zero, input supply (VREG_IN*) > 3.6 V	— —	157 157	— —	µA	
I_{DDstby} VREG_IN0 VREG_IN1	Quiescent current — Standby mode, load current equal zero	— —	2 2	— —	µA	
I_{DDoff} VREG_IN0 VREG_IN1	Quiescent current — Shutdown mode • VREG_IN*= 5.0 V and temperature=25 °C	— —	680 920	— —	nA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	150	mA	3
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{DROPOUT}$	Regulator drop-out voltage — Run mode at maximum load current with inrush current limit disabled	300	—	—	mV	
VREG_OUT	Regulator programmable output target voltage — Selected input supply > programmed output target voltage + $V_{DROPOUT}$ • Run mode • Standby mode	3 2.1	3.3 2.8	3.6 3.6	V V	4
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	350	—	mA	5
I_{INRUSH}	Inrush current limit	40	—	100	mA	6, 7, 8, 9, 10

1. Typical values assume the selected input supply is 5.0 V, Temp = 25 °C unless otherwise stated.

Table 49. SDHC limited voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	7.6 8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

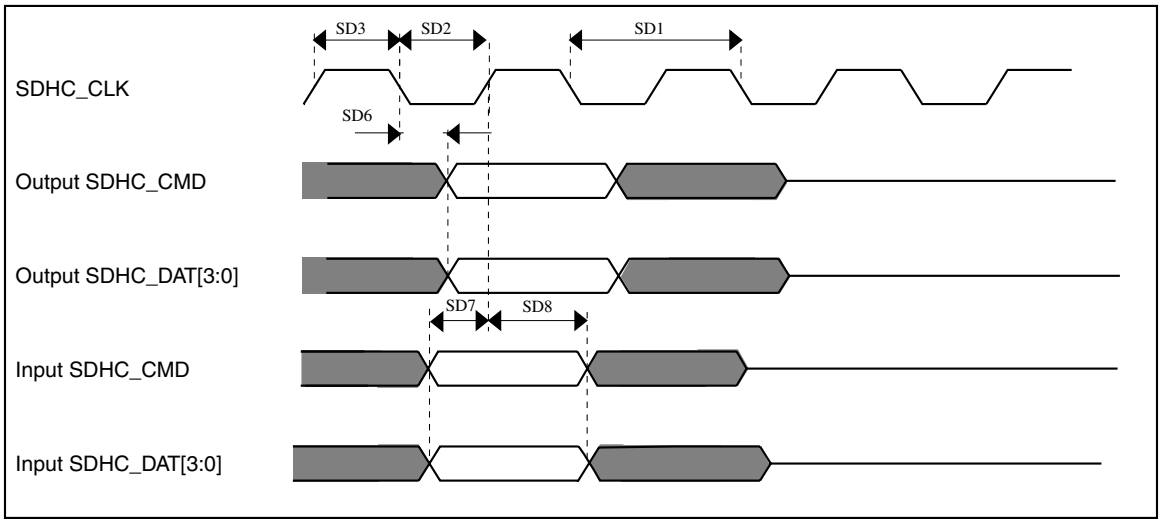


Figure 30. SDHC timing

3.8.12 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] =

Table 52. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

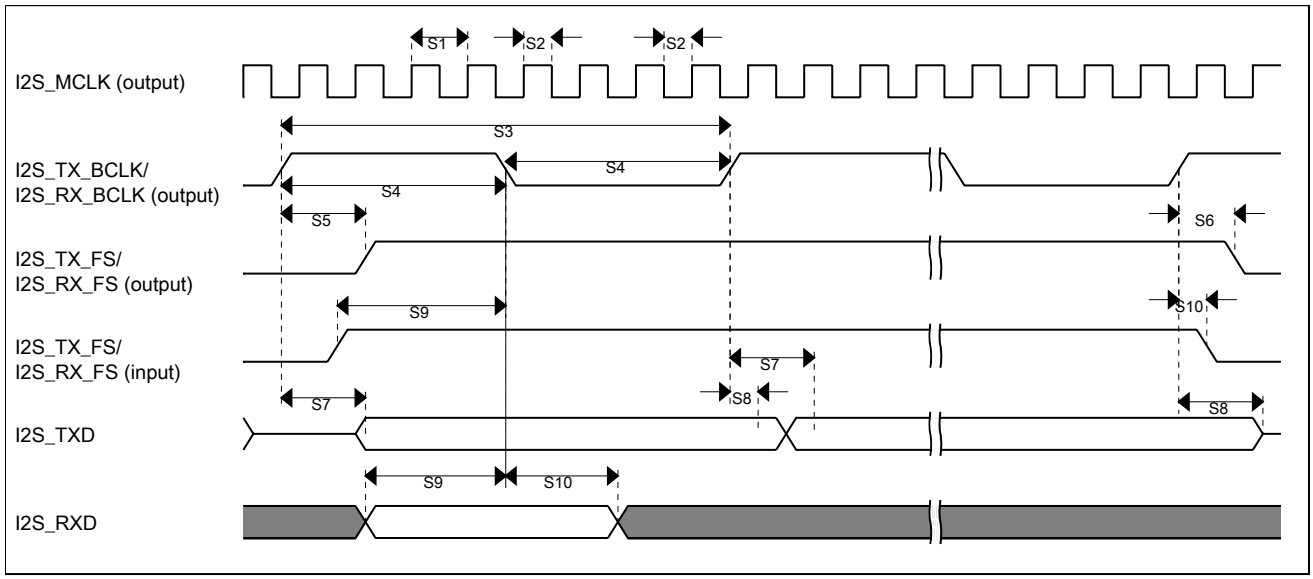


Figure 33. I2S/SAI timing — master modes

Table 53. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.1	ns

Table continues on the next page...

Table 54. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

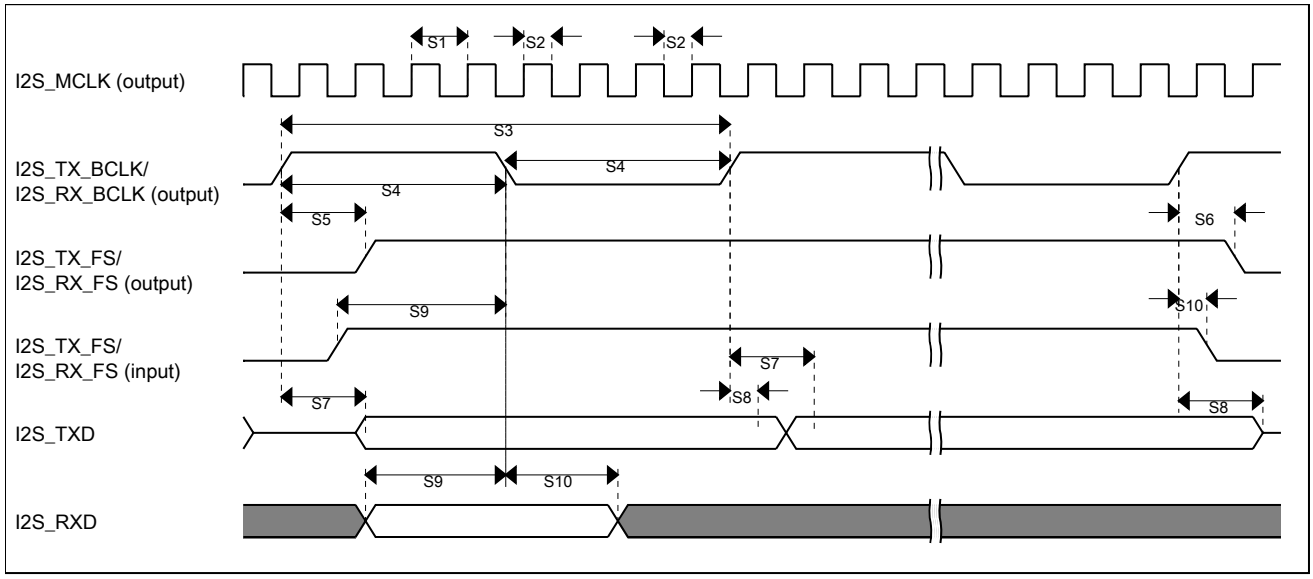


Figure 35. I2S/SAI timing — master modes

Table 55. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	5	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	56.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns

Table continues on the next page...

169 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N13	VSSA	VSSA	VSSA								
H11	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
K10	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
L10	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
M10	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
N11	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								
J10	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B								
H10	TAMPER1	TAMPER1	TAMPER1								
H9	TAMPER2	TAMPER2	TAMPER2								
J9	TAMPER3	TAMPER3	TAMPER3								
N10	TAMPER4	TAMPER4	TAMPER4								
K9	TAMPER5	TAMPER5	TAMPER5								
M9	XTAL32	XTAL32	XTAL32								
N9	EXTAL32	EXTAL32	EXTAL32								
L9	VBAT	VBAT	VBAT								
H8	TAMPER6	TAMPER6	TAMPER6								
J8	TAMPER7	TAMPER7	TAMPER7								
K8	VDD	VDD	VDD								
H7	VSS	VSS	VSS								
N8	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX		I2C0_SCL	EWM_OUT_b		
M8	PTE25/ LLWU_P21	ADC0_SE18	ADC0_SE18	PTE25/ LLWU_P21	CAN1_RX	UART4_RX		I2C0_SDA	EWM_IN		
L8	PTE26	DISABLED		PTE26	ENET_1588_ CLKIN	UART4_CTS_ b			RTC_ CLKOUT	USB0_CLKIN	
J7	PTE27	DISABLED		PTE27		UART4_RTS_ b					
K7	PTE28	DISABLED		PTE28							
N7	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5		LPUART0_ CTS_b		JTAG_TCLK/ SWD_CLK	EZP_CLK

169 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
								BLS31_24_b/ SDRAM_ DQM0			
A6	PTC24	DISABLED		PTC24		LPUART0_TX		FB_A5/ SDRAM_D5			
D7	PTC25	DISABLED		PTC25		LPUART0_RX		FB_A4/ SDRAM_D4			
E8	PTC26	DISABLED		PTC26		LPUART0_ CTS_b	ENET0_ 1588_TMR0	FB_A3/ SDRAM_D3			
A7	PTC27	DISABLED		PTC27		LPUART0_ RTS_b	ENET0_ 1588_TMR1	FB_A2/ SDRAM_D2			
B7	PTC28	DISABLED		PTC28	I2C3_SDA		ENET0_ 1588_TMR2	FB_A1/ SDRAM_D1			
C7	PTC29	DISABLED		PTC29	I2C3_SCL		ENET0_ 1588_TMR3	FB_A0/ SDRAM_D0			
D8	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
A8	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b	FTM3_CH1	FB_CS0_b			
B8	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4/ SDRAM_A12		I2C0_SCL	
C8	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3/ SDRAM_A11		I2C0_SDA	
F8	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4	FB_AD2/ SDRAM_A10	EWM_IN	SPI1_PCS0	
A9	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5	FB_AD1/ SDRAM_A9	EWM_OUT_b	SPI1_SCK	
B9	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
E9	VDD	VDD	VDD								
A10	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7	SDRAM_CKE	FTM0_FLT1	SPI1_SIN	
C9	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C0_SCL			LPUART0_RX	FB_A16		
B10	PTD9	DISABLED		PTD9	I2C0_SDA			LPUART0_TX	FB_A17		
A11	PTD10	DISABLED		PTD10				LPUART0_ RTS_b	FB_A18		
D9	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25	SPI2_PCS0		SDHC0_ CLKIN	LPUART0_ CTS_b	FB_A19		
C10	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
A12	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
B11	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
D10	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

Table 57. Recommended connection for unused analog interfaces (continued)

Pin Type	K65	Short recommendation	Detailed recommendation
USB	USB1_VBUS	Float	Float
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K65 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.