# Renesas Electronics America Inc - R5F212A7SDFA#V2 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 55 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212a7sdfa-v2 |

**Table 1.3 Specifications for R8C/2B Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.6 Product List for R8C/2B Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 2 |
| I/O Ports | Programmable I/O ports | • Input-only: 2 pins<br>• CMOS I/O ports: 55, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function),<br>XCIN clock oscillation circuit (32 kHz)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | • External: 5 sources, Internal: 23 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits × 1<br>Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |
| | Timer RF | 16 bits × 1 (with capture/compare register pin and compare register pin)<br>Input capture mode, output compare mode |

**Table 1.4 Specifications for R8C/2B Group (2)**

| Item | Function | Specification |
|---|---|---|
| Serial Interface | UART0, UART1, UART2 | Clock synchronous serial I/O/UART × 3 |
| Clock Synchronous Serial I/O with Chip Select (SSU) | | 1 (shared with I2C-bus) |
| I2C bus(1) | | 1 (shared with SSU) |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution × 2 circuits |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V)<br>f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) |
| Current consumption | | 12 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>2.1 µA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz))<br>0.65 µA (VCC = 3.0 V, stop mode) |
| Operating Ambient Temperature | | -20 to 85°C (N version)<br>-40 to 85°C (D version)(2)<br>-20 to 105°C (Y version)(3) |
| Package | | 64-pin LQFP<br>• Package code: PLQP0064KB-A (previous code: 64P6Q-A)<br>• Package code: PLQP0064GA-A (previous code: 64P6U-A)<br>64-pin FLGA<br>• Package code: PTLG0064JA-A (previous code: 64F0G) |

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

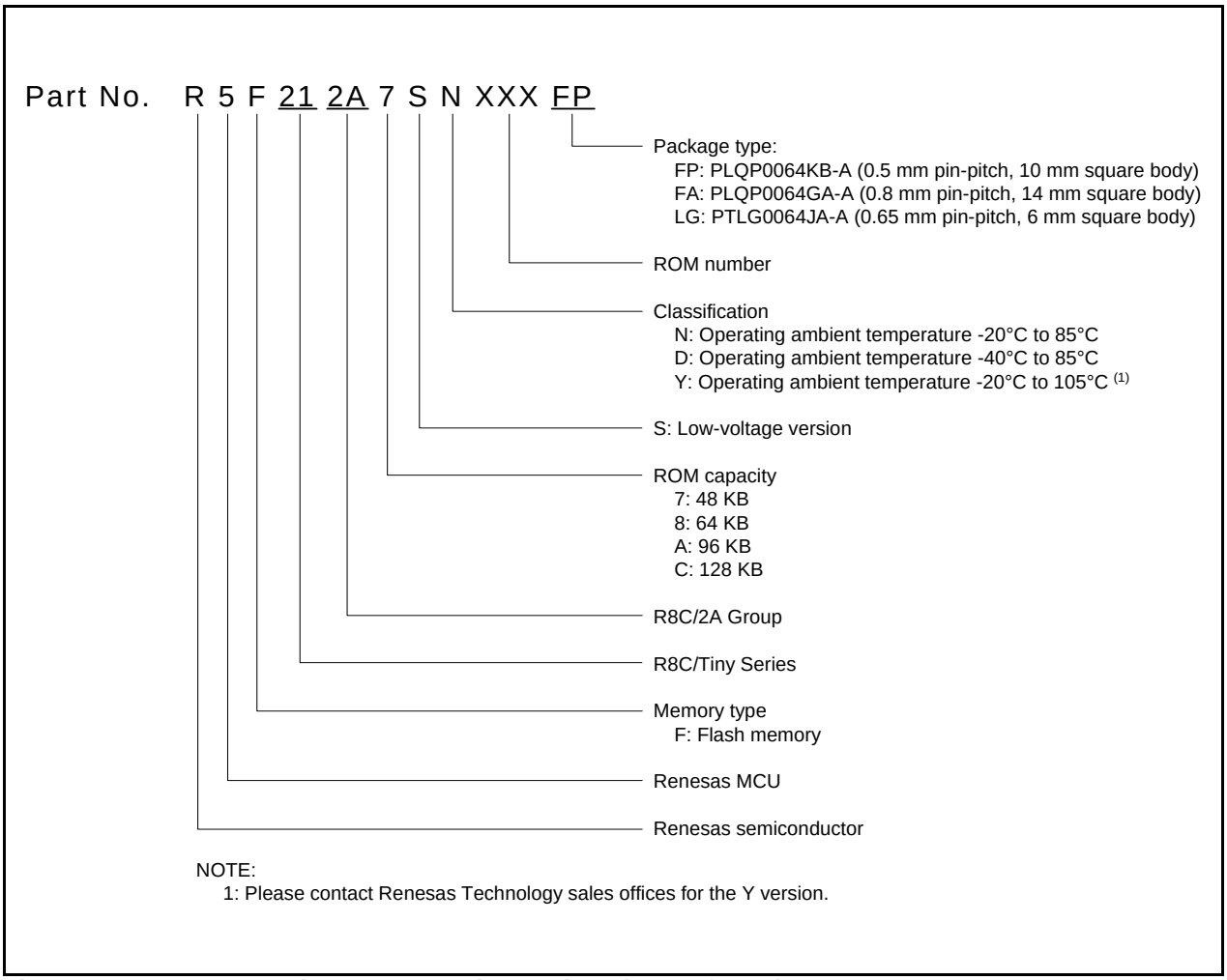



**Figure 1.1 Part Number, Memory Size, and Package of R8C/2A Group**

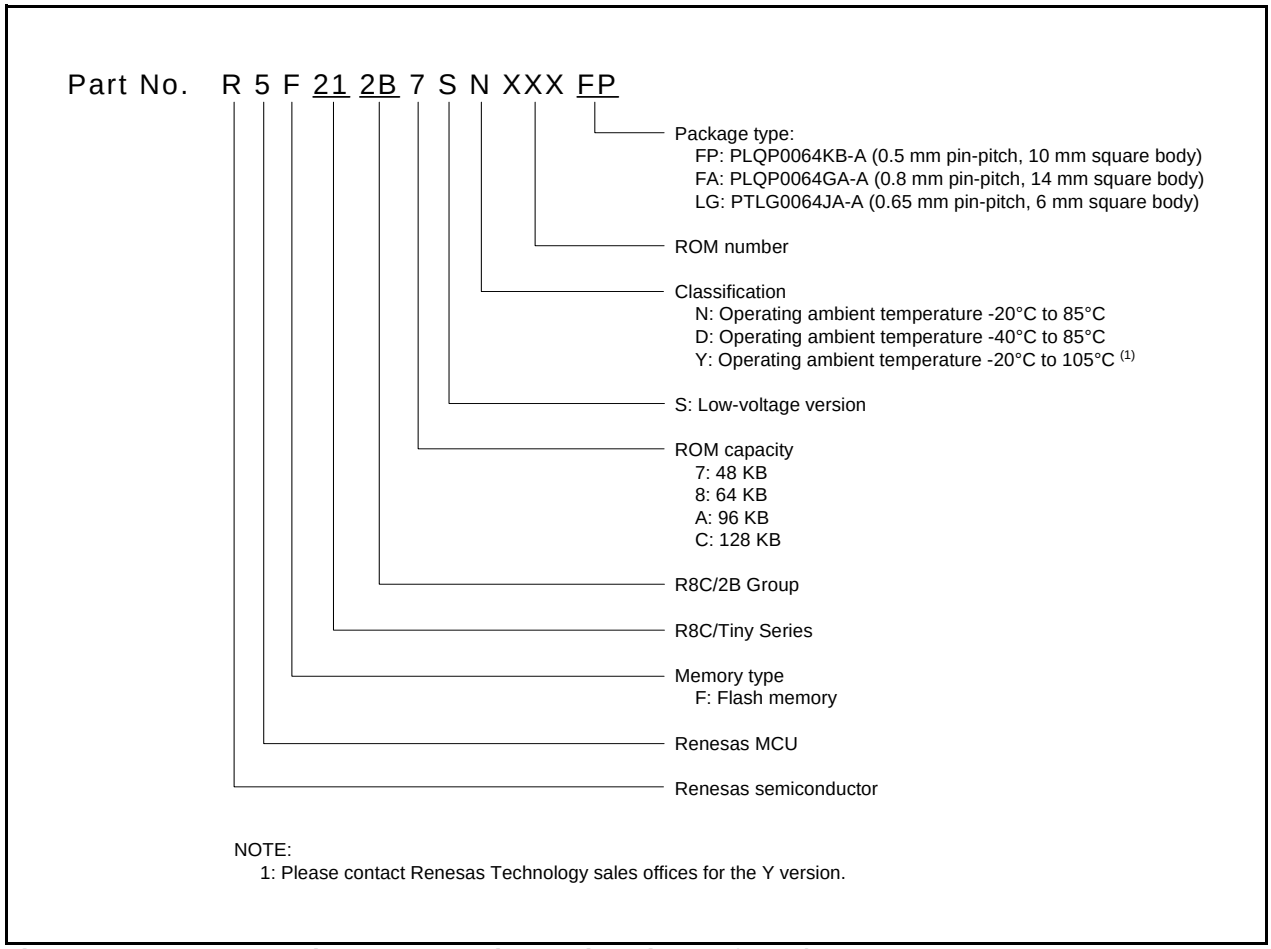
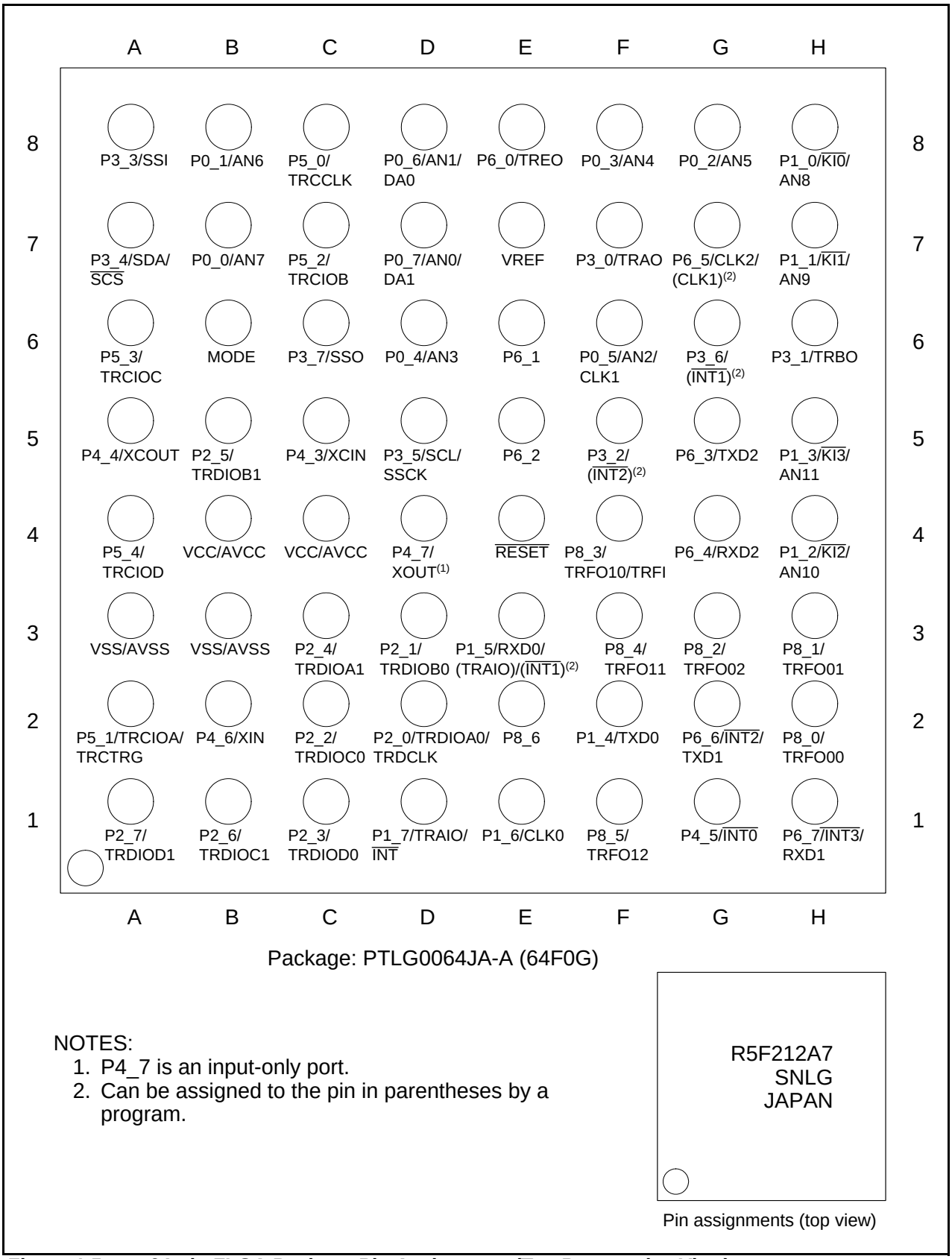



**Figure 1.2 Part Number, Memory Size, and Package of R8C/2B Group**




Package: PTLG0064JA-A (64F0G)

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.




Pin assignments (top view)

**Figure 1.5 64-pin FLGA Package Pin Assignment (Top Perspective View)**

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

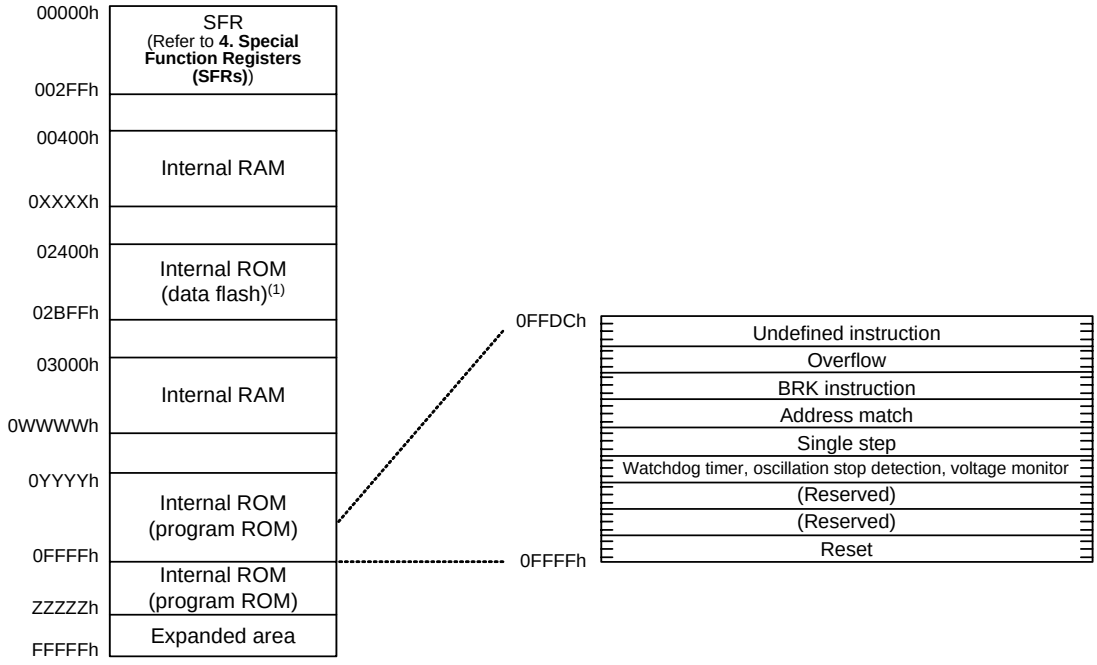
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

## 3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

| Internal ROM | | | Internal RAM | | |
|---|---|---|---|---|---|
| Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh | Address 0WWWWh |
| 48 Kbytes | 04000h | – | 2.5 Kbytes | 00DFFh | – |
| 64 Kbytes | 04000h | 13FFFh | 3 Kbytes | 00FFFh | – |
| 96 Kbytes | 04000h | 1BFFFh | 7 Kbytes | 011FFh | 03DFFh |
| 128 Kbytes | 04000h | 23FFFh | 7.5 Kbytes | 011FFh | 03FFFh |

**Figure 3.2 Memory Map of R8C/2B Group**

**Table 4.6 SFR Information (6)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0140h | Timer RD Control Register 0 | TRDCR0 | 00h |
| 0141h | Timer RD I/O Control Register A0 | TRDIORA0 | 10001000b |
| 0142h | Timer RD I/O Control Register C0 | TRDIORC0 | 10001000b |
| 0143h | Timer RD Status Register 0 | TRDSR0 | 11000000b |
| 0144h | Timer RD Interrupt Enable Register 0 | TRDIER0 | 11100000b |
| 0145h | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b |
| 0146h | Timer RD Counter 0 | TRD0 | 00h |
| 0147h | | | 00h |
| 0148h | Timer RD General Register A0 | TRDGRA0 | FFh |
| 0149h | | | FFh |
| 014Ah | Timer RD General Register B0 | TRDGRB0 | FFh |
| 014Bh | | | FFh |
| 014Ch | Timer RD General Register C0 | TRDGRC0 | FFh |
| 014Dh | | | FFh |
| 014Eh | Timer RD General Register D0 | TRDGRD0 | FFh |
| 014Fh | | | FFh |
| 0150h | Timer RD Control Register 1 | TRDCR1 | 00h |
| 0151h | Timer RD I/O Control Register A1 | TRDIORA1 | 10001000b |
| 0152h | Timer RD I/O Control Register C1 | TRDIORC1 | 10001000b |
| 0153h | Timer RD Status Register 1 | TRDSR1 | 11000000b |
| 0154h | Timer RD Interrupt Enable Register 1 | TRDIER1 | 11100000b |
| 0155h | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b |
| 0156h | Timer RD Counter 1 | TRD1 | 00h |
| 0157h | | | 00h |
| 0158h | Timer RD General Register A1 | TRDGRA1 | FFh |
| 0159h | | | FFh |
| 015Ah | Timer RD General Register B1 | TRDGRB1 | FFh |
| 015Bh | | | FFh |
| 015Ch | Timer RD General Register C1 | TRDGRC1 | FFh |
| 015Dh | | | FFh |
| 015Eh | Timer RD General Register D1 | TRDGRD1 | FFh |
| 015Fh | | | FFh |
| 0160h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0161h | UART2 Bit Rate Register | U2BRG | XXh |
| 0162h | UART2 Transmit Buffer Register | U2TB | XXh |
| 0163h | | | XXh |
| 0164h | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 0165h | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 0166h | UART2 Receive Buffer Register | U2RB | XXh |
| 0167h | | | XXh |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |
| 0170h | | | |
| 0171h | | | |
| 0172h | | | |
| 0173h | | | |
| 0174h | | | |
| 0175h | | | |
| 0176h | | | |
| 0177h | | | |
| 0178h | | | |
| 0179h | | | |
| 017Ah | | | |
| 017Bh | | | |
| 017Ch | | | |
| 017Dh | | | |
| 017Eh | | | |
| 017Fh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 4.12 SFR Information (12)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 02C0h | A/D Register 0 | AD0 | XXh |
| 02C1h | | | XXh |
| 02C2h | | | |
| 02C3h | | | |
| 02C4h | | | |
| 02C5h | | | |
| 02C6h | | | |
| 02C7h | | | |
| 02C8h | | | |
| 02C9h | | | |
| 02CAh | | | |
| 02CBh | | | |
| 02CCh | | | |
| 02CDh | | | |
| 02CEh | | | |
| 02CFh | | | |
| 02D0h | | | |
| 02D1h | | | |
| 02D2h | | | |
| 02D3h | | | |
| 02D4h | A/D Control Register 2 | ADCON2 | 00001000b |
| 02D5h | | | |
| 02D6h | A/D Control Register 0 | ADCON0 | 00000011b |
| 02D7h | A/D Control Register 1 | ADCON1 | 00h |
| 02D8h | | | |
| 02D9h | | | |
| 02DAh | | | |
| 02DBh | | | |
| 02DCh | | | |
| 02DDh | | | |
| 02DEh | | | |
| 02DFh | | | |
| 02E0h | | | |
| 02E1h | | | |
| 02E2h | | | |
| 02E3h | | | |
| 02E4h | Port P8 Direction Register | PD8 | 00h |
| 02E5h | | | |
| 02E6h | Port P8 Register | P8 | XXh |
| 02E7h | | | |
| 02E8h | | | |
| 02E9h | | | |
| 02EAh | | | |
| 02EBh | | | |
| 02ECh | | | |
| 02EDh | | | |
| 02EEh | | | |
| 02EFh | | | |
| 02F0h | | | |
| 02F1h | | | |
| 02F2h | | | |
| 02F3h | | | |
| 02F4h | | | |
| 02F5h | | | |
| 02F6h | | | |
| 02F7h | | | |
| 02F8h | | | |
| 02F9h | | | |
| 02FAh | | | |
| 02FBh | | | |
| 02FCh | Pull-Up Control Register 2 | PUR2 | XXX00000b |
| 02FDh | | | |
| 02FEh | | | |
| 02FFh | Timer RF Output Control Register | TRFOUT | 00h |
| FFFFh | Option Function Select Register | OFS | (Note 2) |

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

# 5. Electrical Characteristics

The electrical characteristics of N version (Topr = –20°C to 85°C) and D version (Topr = –40°C to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = –20°C to 105°C).

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | -0.3 to 6.5 | V |
| $V_I$ | Input voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | $T_{opr}$ = 25°C | 700 | mW |
| $T_{opr}$ | Operating ambient temperature | | -20 to 85 (N version) / -40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |

**Table 5.2 Recommended Operating Conditions**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | 2.2 | – | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | | | 0 | – | 0.2 $V_{CC}$ | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | – | – | –240 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | Sum of all pins $I_{OH(avg)}$ | | – | – | –120 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | Except P2_0 to P2_7 | | – | – | -10 | mA |
| | | P2_0 to P2_7 | | – | – | -40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | Except P2_0 to P2_7 | | – | – | -5 | mA |
| | | P2_0 to P2_7 | | – | – | -20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” current | Sum of all pins $I_{OL(peak)}$ | | – | – | 240 | mA |
| $I_{OL(sum)}$ | Average sum output “L” current | Sum of all pins $I_{OL(avg)}$ | | – | – | 120 | mA |
| $I_{OL(peak)}$ | Peak output “L” current | Except P2_0 to P2_7 | | – | – | 10 | mA |
| | | P2_0 to P2_7 | | – | – | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Except P2_0 to P2_7 | | – | – | 5 | mA |
| | | P2_0 to P2_7 | | – | – | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 5 | MHz |
| $f_{(XCIN)}$ | XCIN clock input oscillation frequency | | 2.2 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 70 | kHz |
| – | System clock | OCD2 = 0<br>XIN clock selected | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 5 | MHz |
| | | OCD2 = 1<br>On-chip oscillator clock selected | FRA01 = 0<br>Low-speed on-chip oscillator clock selected | – | 125 | – | kHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>3.0 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 10 | MHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>2.2 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 5 | MHz |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

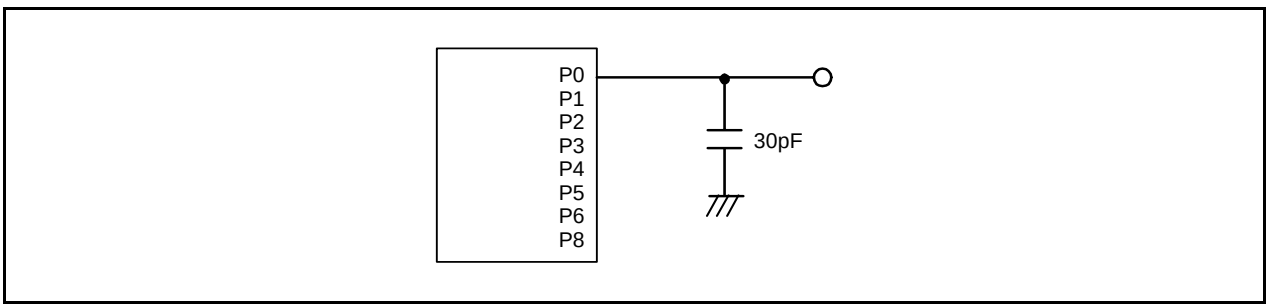



**Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit**

### Table 5.3 A/D Converter Characteristics(1)

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | – | – | 10 | Bit |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 5 MHz, $V_{ref}$ = $AV_{CC}$ = 2.2 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = $AV_{CC}$ | 10 | – | 40 | kΩ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 3.3 | – | – | µs |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 2.8 | – | – | µs |
| $V_{ref}$ | Reference voltage | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage(2) | | | 0 | – | $AV_{CC}$ | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 1 | – | 10 | MHz |
| | | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 0.25 | – | 5 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.2 to 5.5 V | 1 | – | 5 | MHz |

NOTES:
1. $V_{CC}$/$AV_{CC}$ = Vref = 2.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

### Table 5.4 D/A Converter Characteristics(1)

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | – | – | 8 | Bit |
| – | Absolute accuracy | | – | – | 1.0 | % |
| $t_{su}$ | Setup time | | – | – | 3 | µs |
| $R_O$ | Output resistor | | 4 | 10 | 20 | kΩ |
| $I_{Vref}$ | Reference power input current | (NOTE 2) | – | – | 1.5 | mA |

NOTES:
1. $V_{CC}$/$AV_{CC}$ = Vref = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 ($V_{REF}$ not connected), $I_{Vref}$ flows into the D/A converters.

**Table 5.6 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | | 10,000(3) | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | µs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | µs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | -20(8) | – | 85 | °C |
| – | Data hold time(9) | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

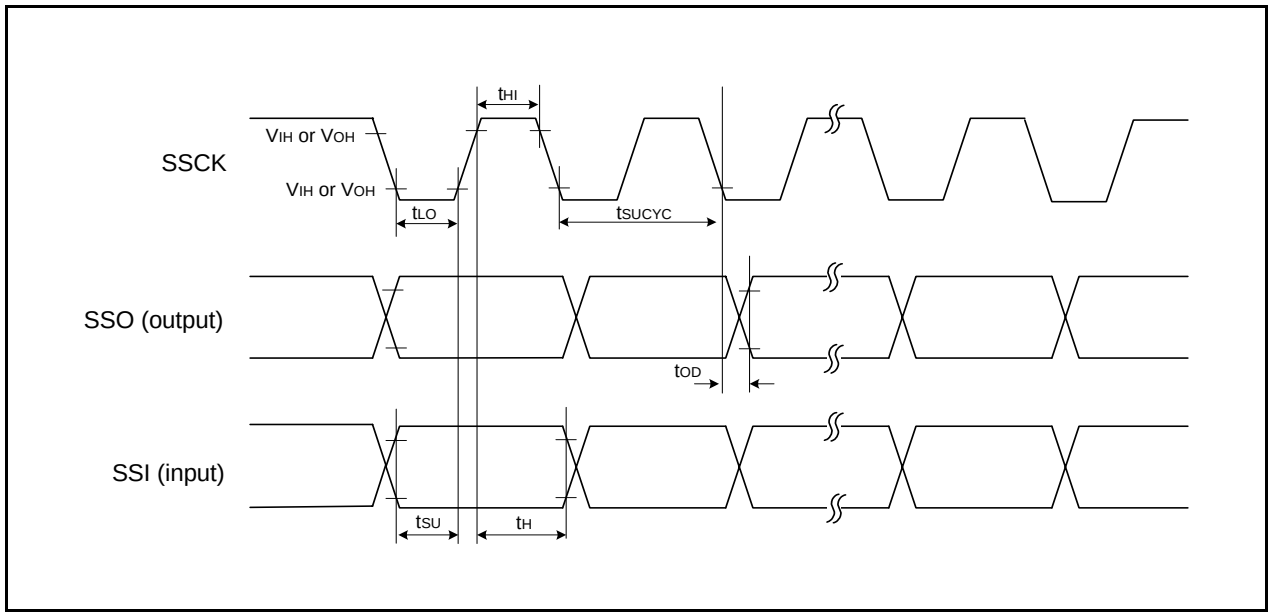
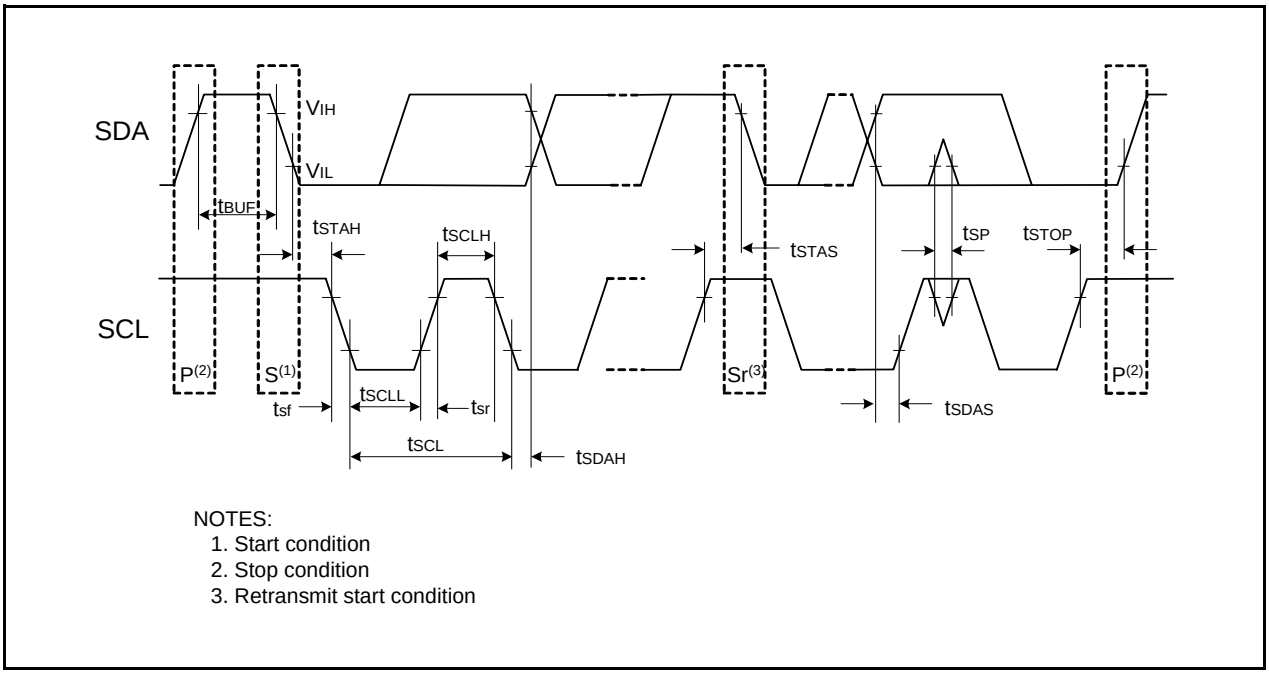



**Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)**

**Table 5.15 Timing Requirements of I²C bus Interface (1)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{SCL}$ | SCL input cycle time | | $12t_{CYC} + 600^{(2)}$ | – | – | ns |
| $t_{SCLH}$ | SCL input “H” width | | $3t_{CYC} + 300^{(2)}$ | – | – | ns |
| $t_{SCLL}$ | SCL input “L” width | | $5t_{CYC} + 500^{(2)}$ | – | – | ns |
| $t_{sf}$ | SCL, SDA input fall time | | – | – | 300 | ns |
| $t_{SP}$ | SCL, SDA input spike pulse rejection time | | – | – | $1t_{CYC}^{(2)}$ | ns |
| $t_{BUF}$ | SDA input bus-free time | | $5t_{CYC}^{(2)}$ | – | – | ns |
| $t_{STAH}$ | Start condition input hold time | | $3t_{CYC}^{(2)}$ | – | – | ns |
| $t_{STAS}$ | Retransmit start condition input setup time | | $3t_{CYC}^{(2)}$ | – | – | ns |
| $t_{STOP}$ | Stop condition input setup time | | $3t_{CYC}^{(2)}$ | – | – | ns |
| $t_{SDAS}$ | Data input setup time | | $1t_{CYC} + 20^{(2)}$ | – | – | ns |
| $t_{SDAH}$ | Data input hold time | | 0 | – | – | ns |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $V_{SS}$ = 0 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$




NOTES:
1. Start condition
2. Stop condition
3. Retransmit start condition

**Figure 5.7 I/O Timing of I²C bus Interface**

**Table 5.16 Electrical Characteristics (1) [$V_{CC}$ = 5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = -5 mA | | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | $I_{OH}$ = -200 µA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = -20 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = -5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -1 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = -500 µA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 5 mA | | – | – | 2.0 | V |
| | | | $I_{OL}$ = 200 µA | | – | – | 0.45 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 500 µA | – | – | 2.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.0 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | -5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 30 | 50 | 167 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 18 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. $V_{CC}$ = 4.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.28 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 to 2

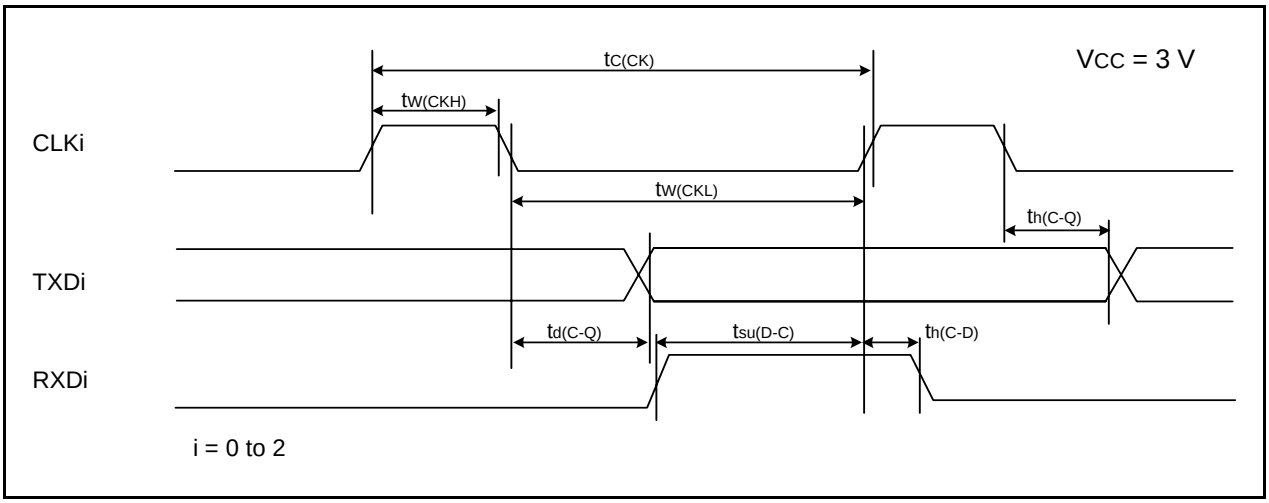



**Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.29 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

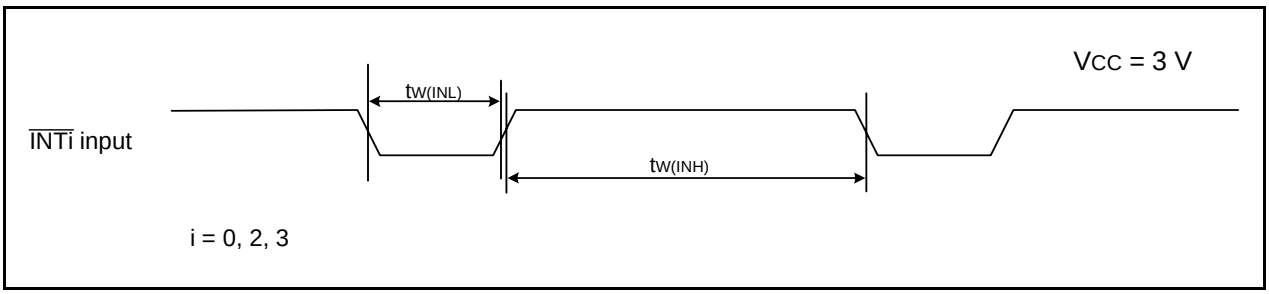



**Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V**

**Timing requirements**
**(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]**

**Table 5.32 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 200 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 90 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

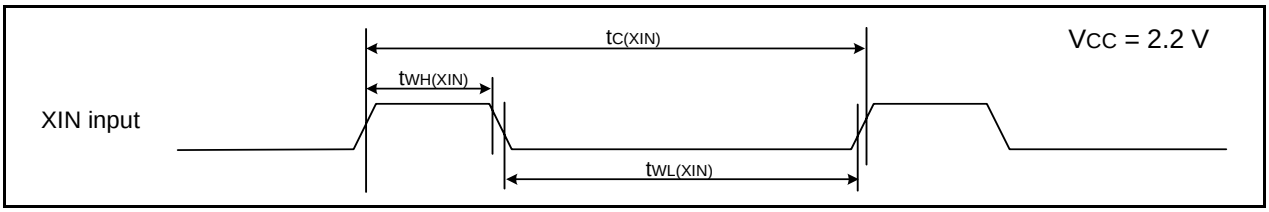



**Figure 5.18 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V**

**Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | TBD | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | TBD | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | TBD | – | ns |

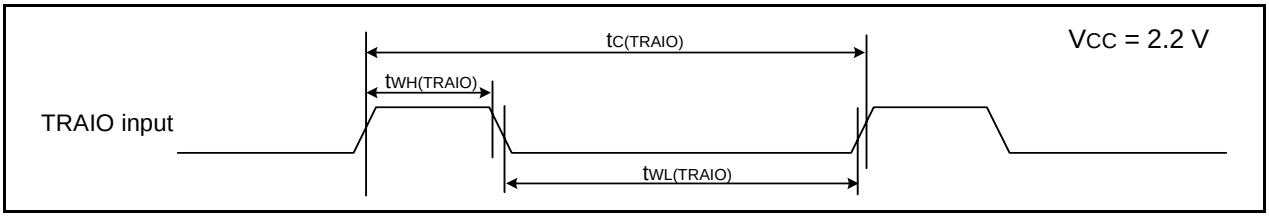



**Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 2.2 V**

**Table 5.34 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 2000(1) | – | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 1000(2) | – | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 1000(2) | – | ns |

NOTES:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

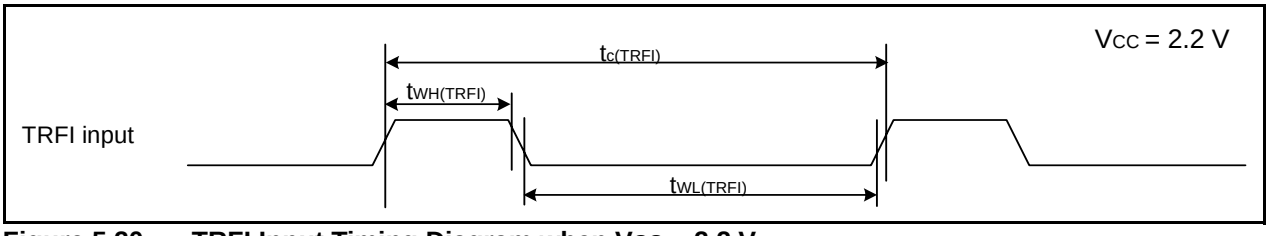
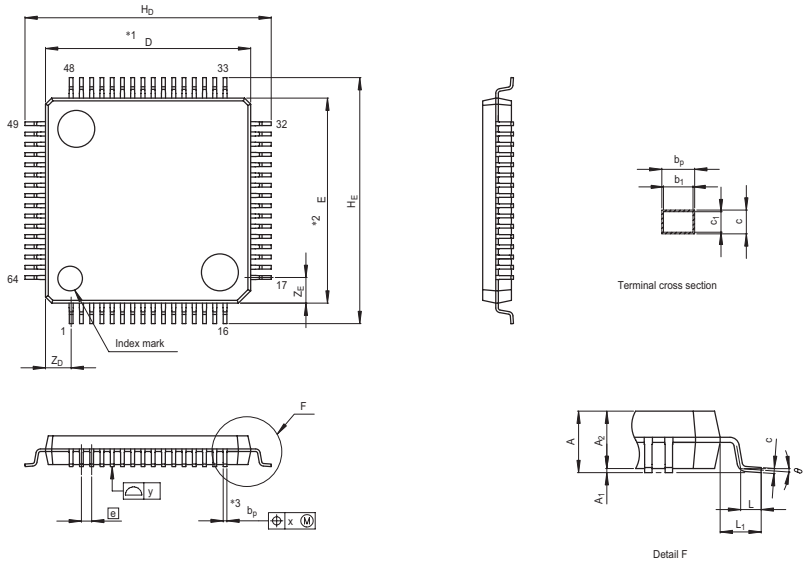



**Figure 5.20 TRFI Input Timing Diagram when Vcc = 2.2 V**

# Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

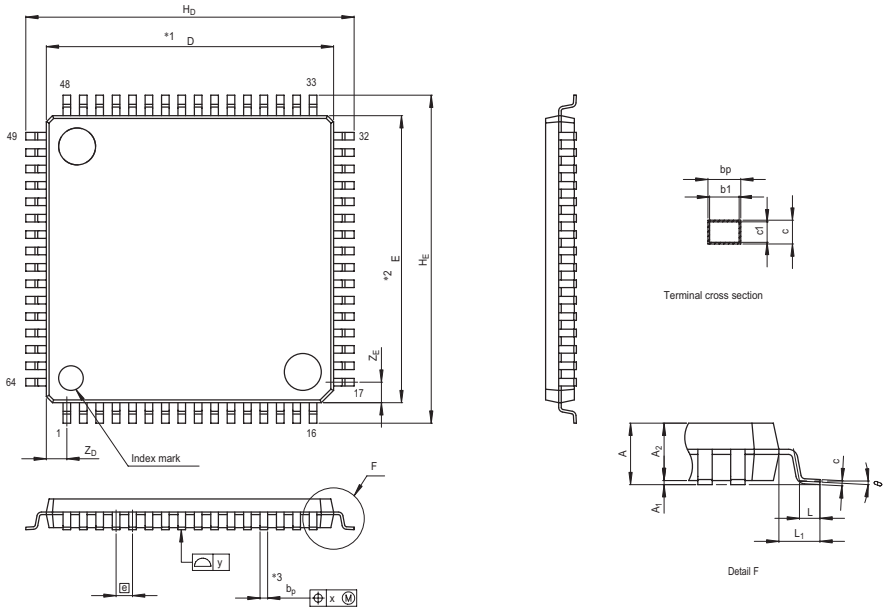
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | 64P6U-A | 0.7g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.32 | 0.37 | 0.42 |
| $b_1$ | — | 0.35 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.8 | — |
| x | — | — | 0.20 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |

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