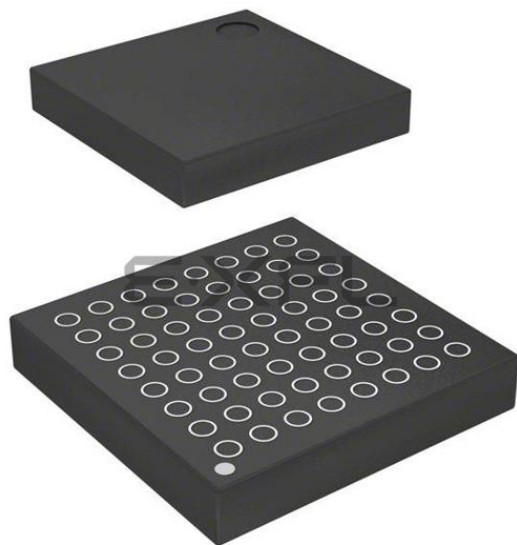




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFLGA
Supplier Device Package	64-TFLGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212a7snlg-u0

1. Overview

1.1 Features

The R8C/2A Group and R8C/2B Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2B Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/2A Group and R8C/2B Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

Table 1.2 Specifications for R8C/2A Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I ² C-bus)
I ² C bus ⁽¹⁾		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

Table 1.5 Product List for R8C/2A Group

Current of Nov. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F212A7SNFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version		
R5F212A7SNFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product ⁽¹⁾	
R5F212A7SNXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNXXXLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNXXXLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNXXXLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			

NOTE:

1. The user ROM is programmed before shipment.

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

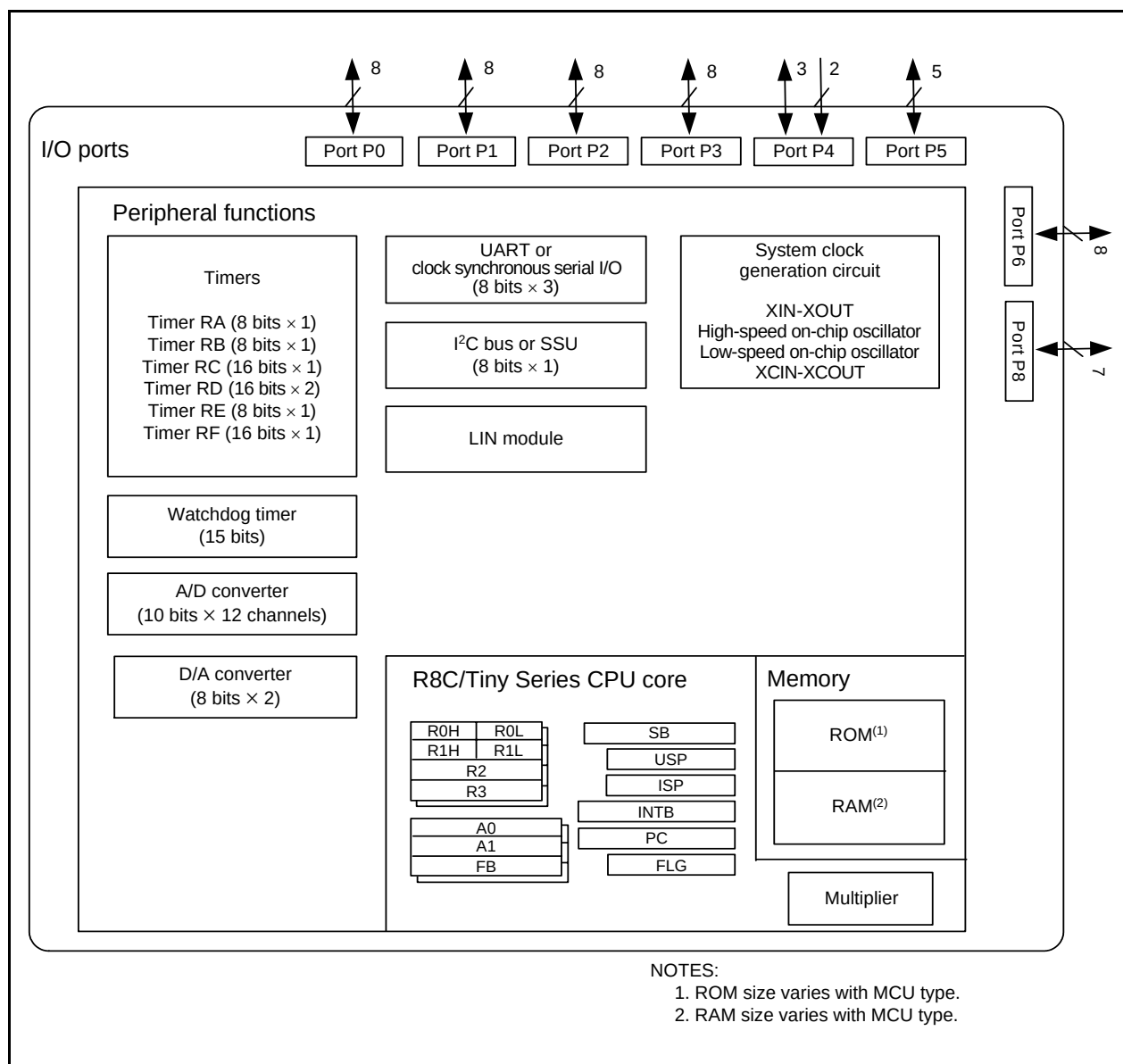


Figure 1.3 Block Diagram

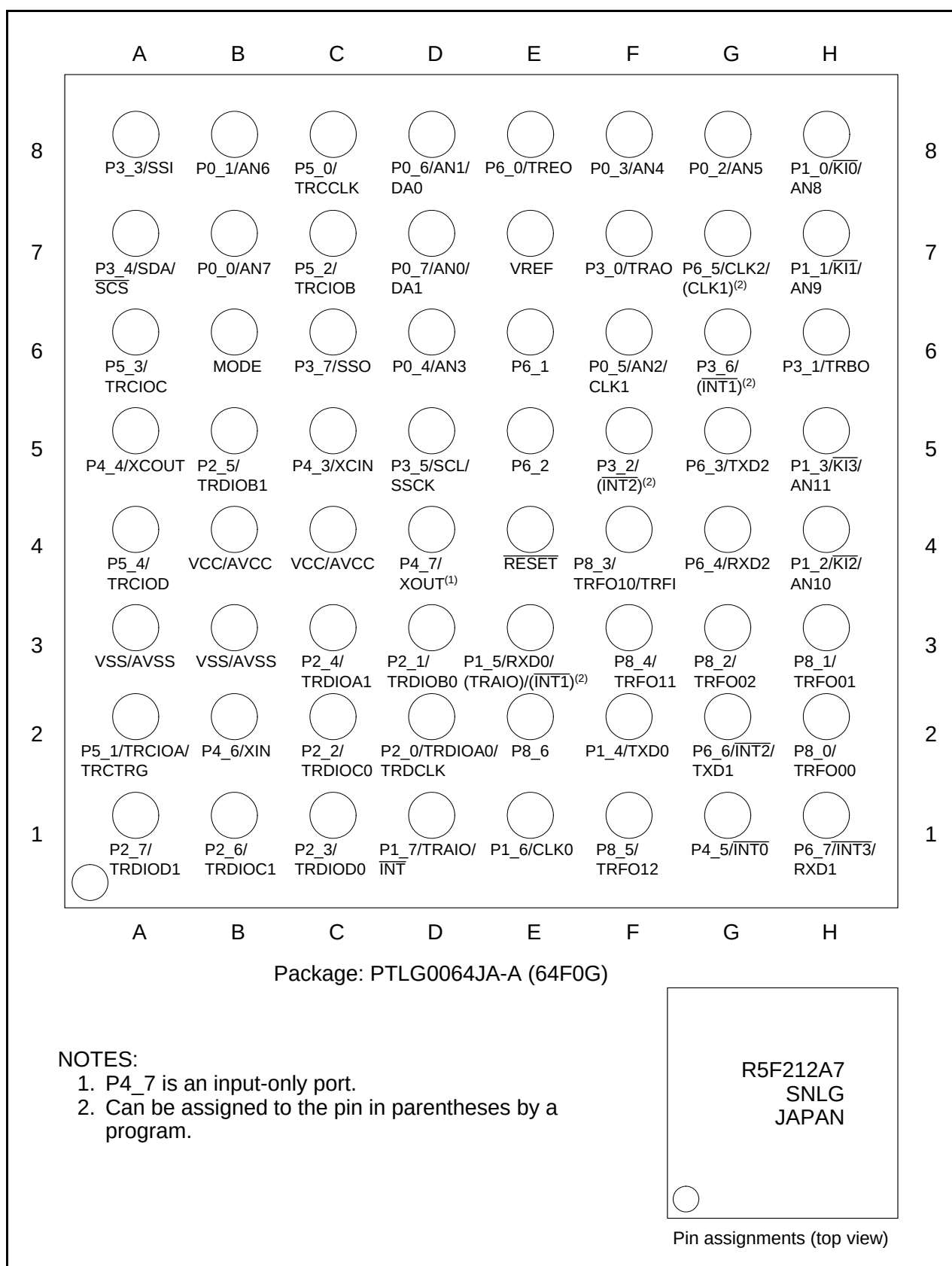


Figure 1.5 64-pin FLGA Package Pin Assignment (Top Perspective View)

Table 1.8 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter
46		P1_3	$\overline{\text{KI3}}$					AN11
47		P1_2	$\overline{\text{KI2}}$					AN10
48		P1_1	$\overline{\text{KI1}}$					AN9
49		P1_0	$\overline{\text{KI0}}$					AN8
50		P0_0						AN7
51		P0_1						AN6
52		P0_2						AN5
53		P0_3						AN4
54		P0_4						AN3
55		P6_2						
56		P6_1						
57		P0_5			CLK1			AN2
58		P0_6						AN1/DA0
59	VSS/AVSS							
60		P0_7						AN0/DA1
61	VREF							
62	VCC/AVCC							
63		P3_7				SSO		
64		P3_5				SSCK	SCL	

1.5 Pin Functions

Tables 1.9 and 1.10 list Pin Functions.

Table 1.9 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRA0	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO12	O	Timer RF output pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 4.8 SFR Information (8)⁽¹⁾

Address	Register	Symbol	After reset
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾	R8C/2A Group	100 ⁽³⁾	–	–	times
		R8C/2B Group	1,000 ⁽³⁾	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
tr _{th}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

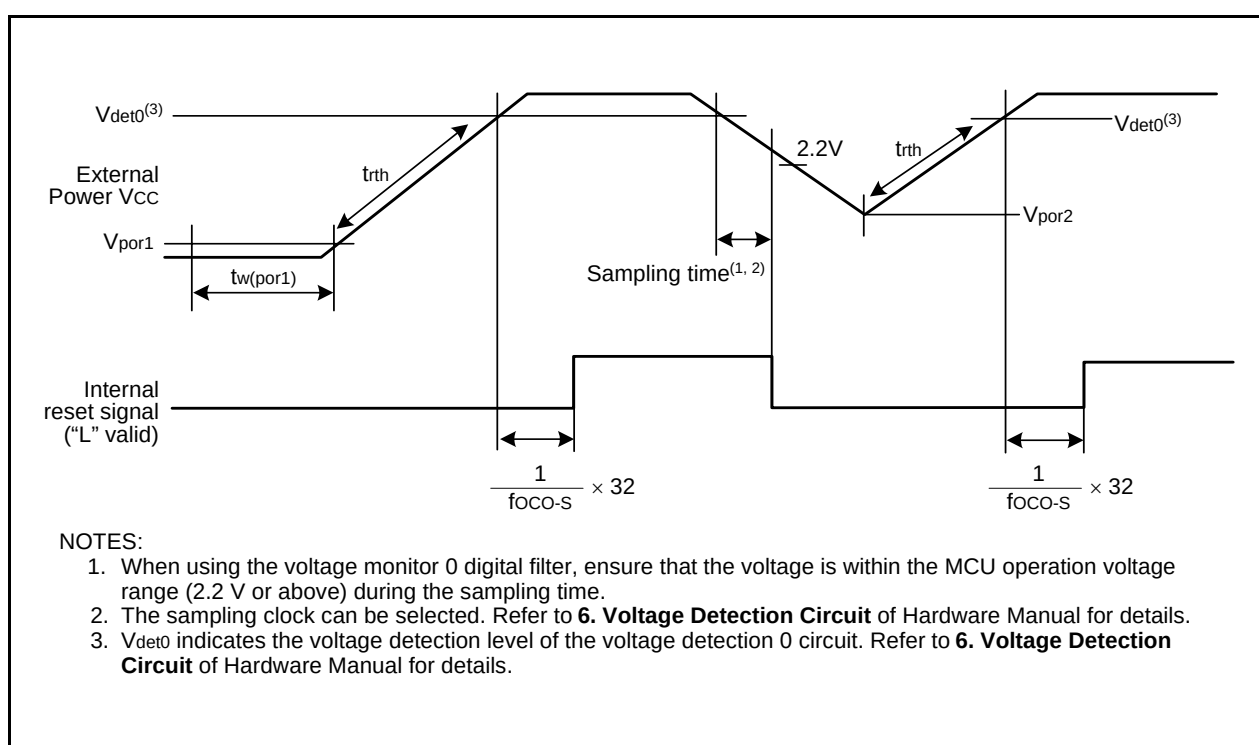
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	SCS setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	SCS hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
tsa	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

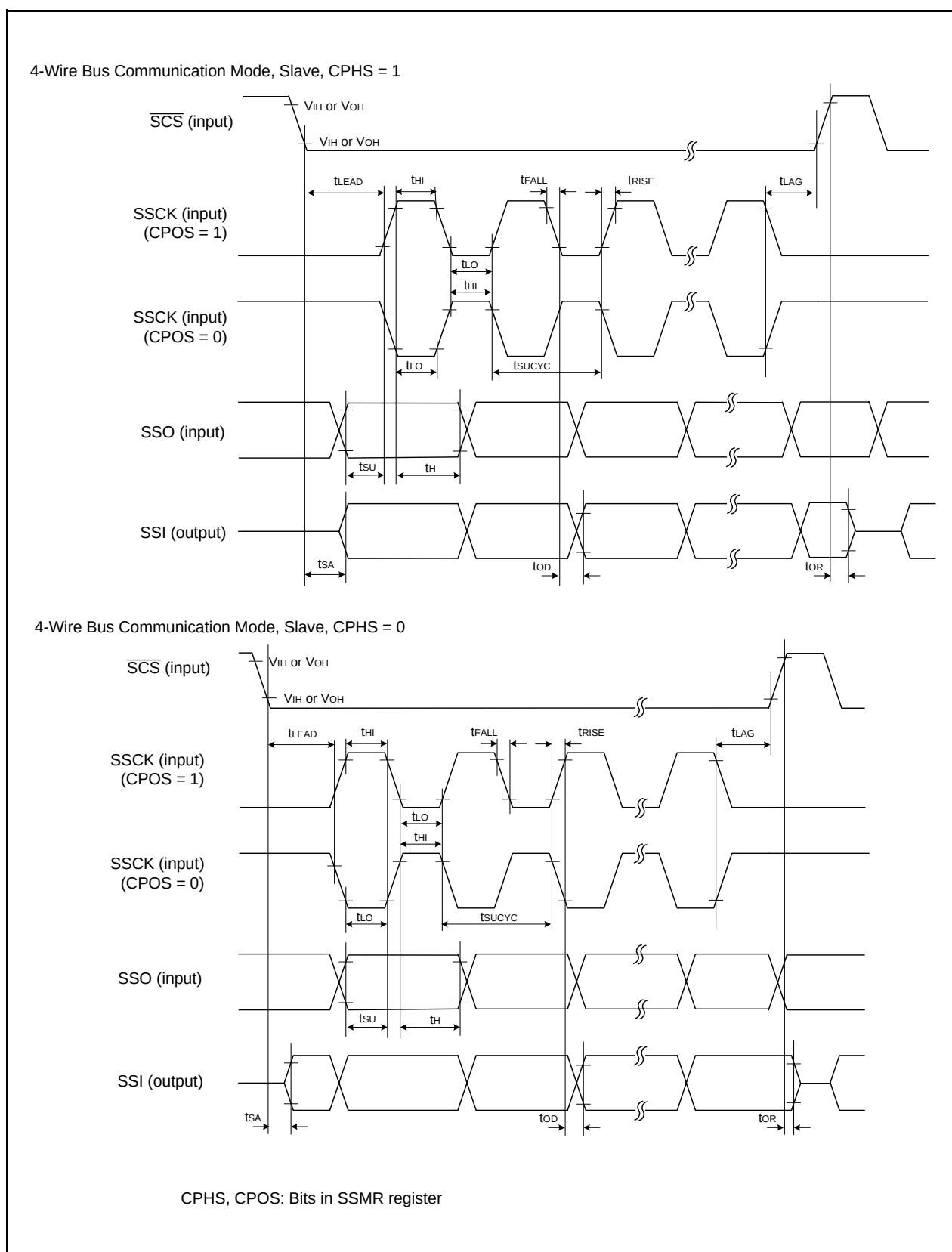
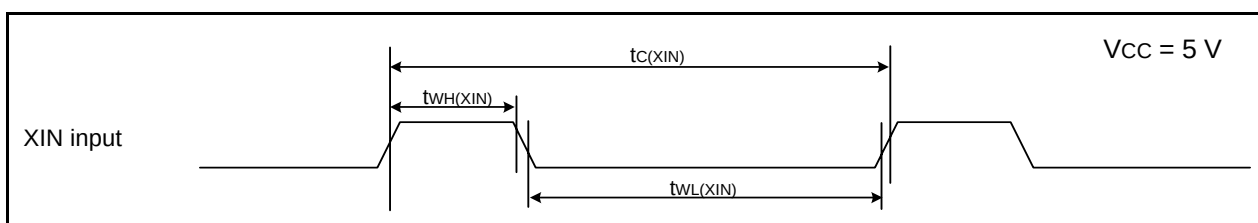


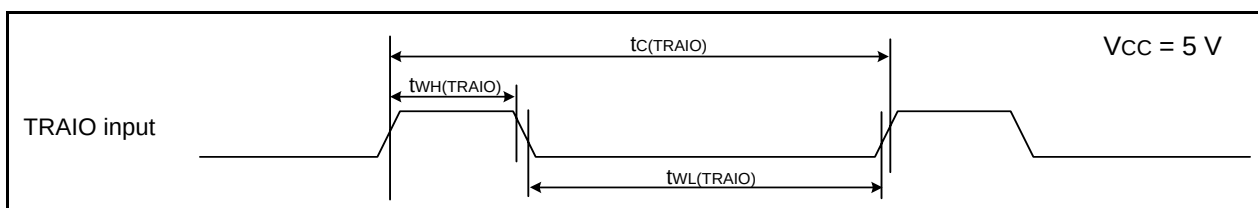
Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^\circ\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.18 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

**Figure 5.9 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

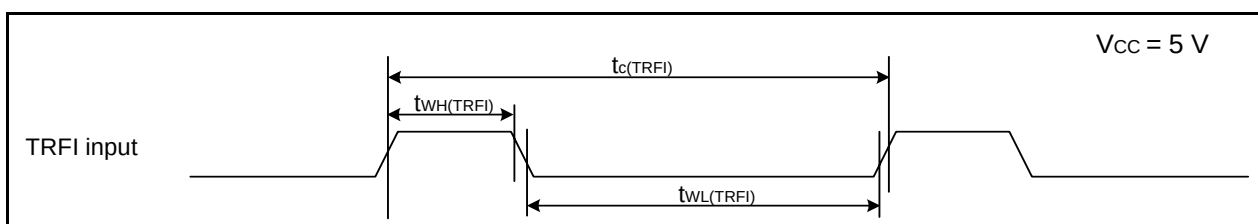
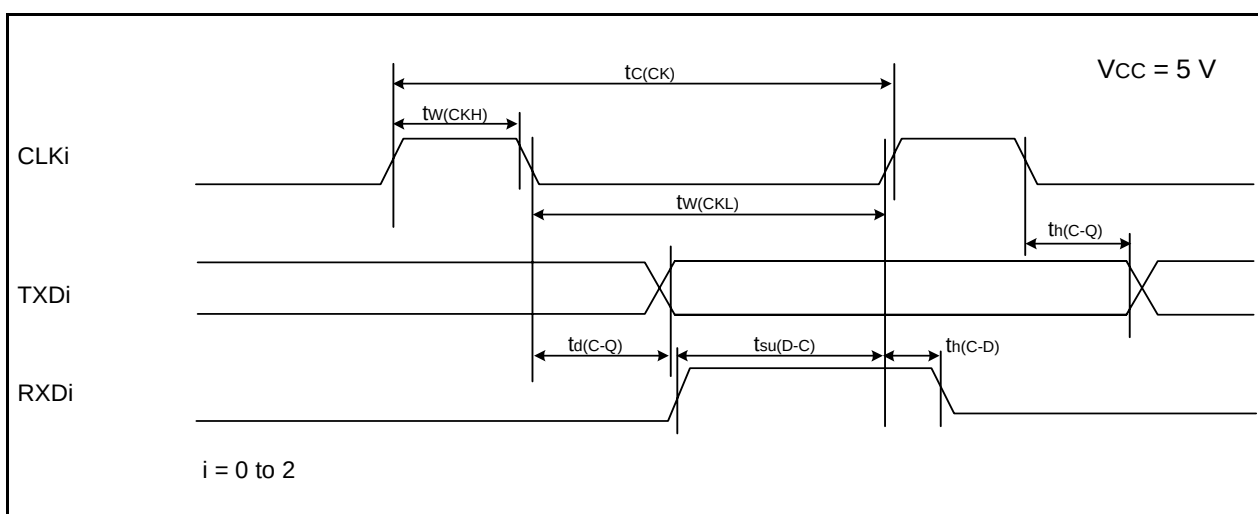
**Figure 5.10 TRFI Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

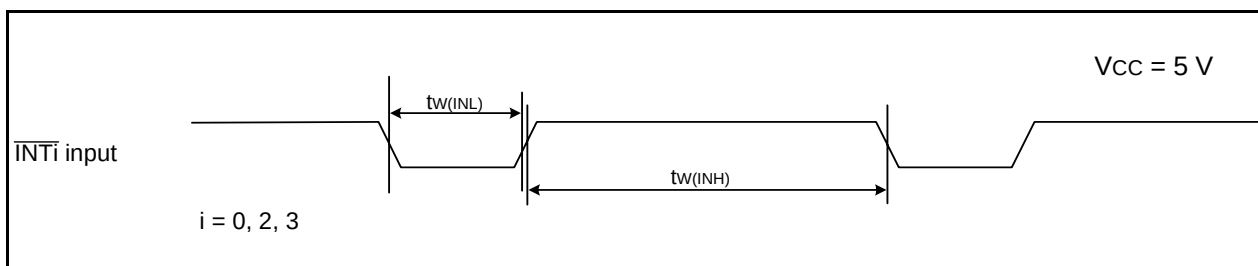
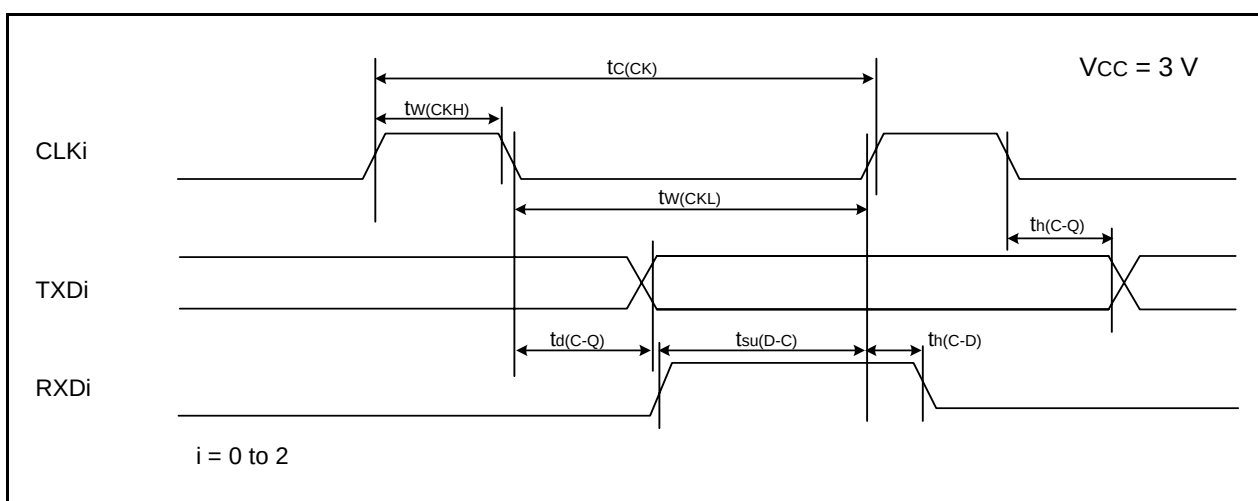
**Figure 5.12 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.28 Serial Interface

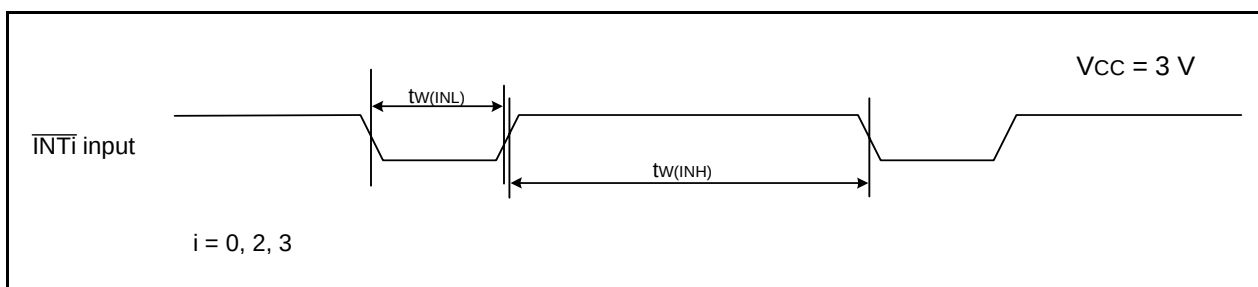
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.29 External Interrupt $\overline{INTi}$ ($i = 0, 2, 3$) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	380 ⁽²⁾	—	ns

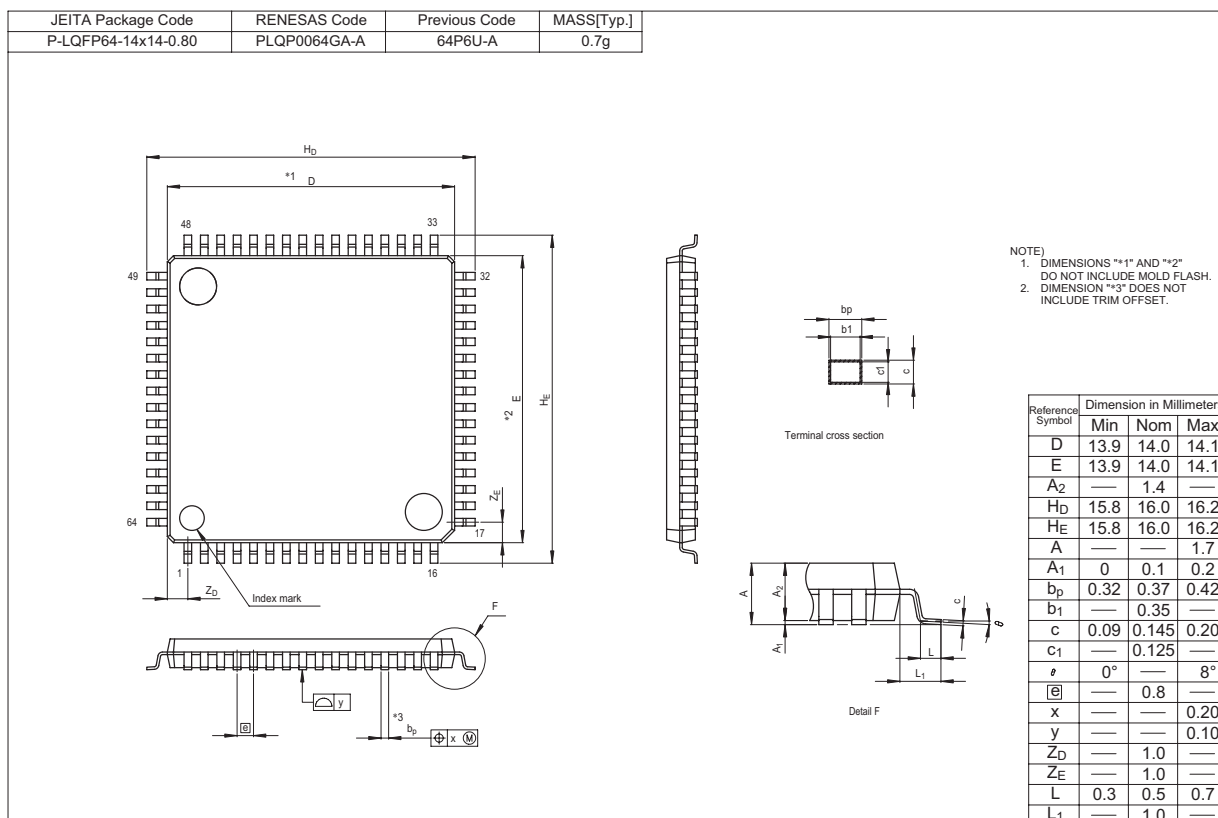
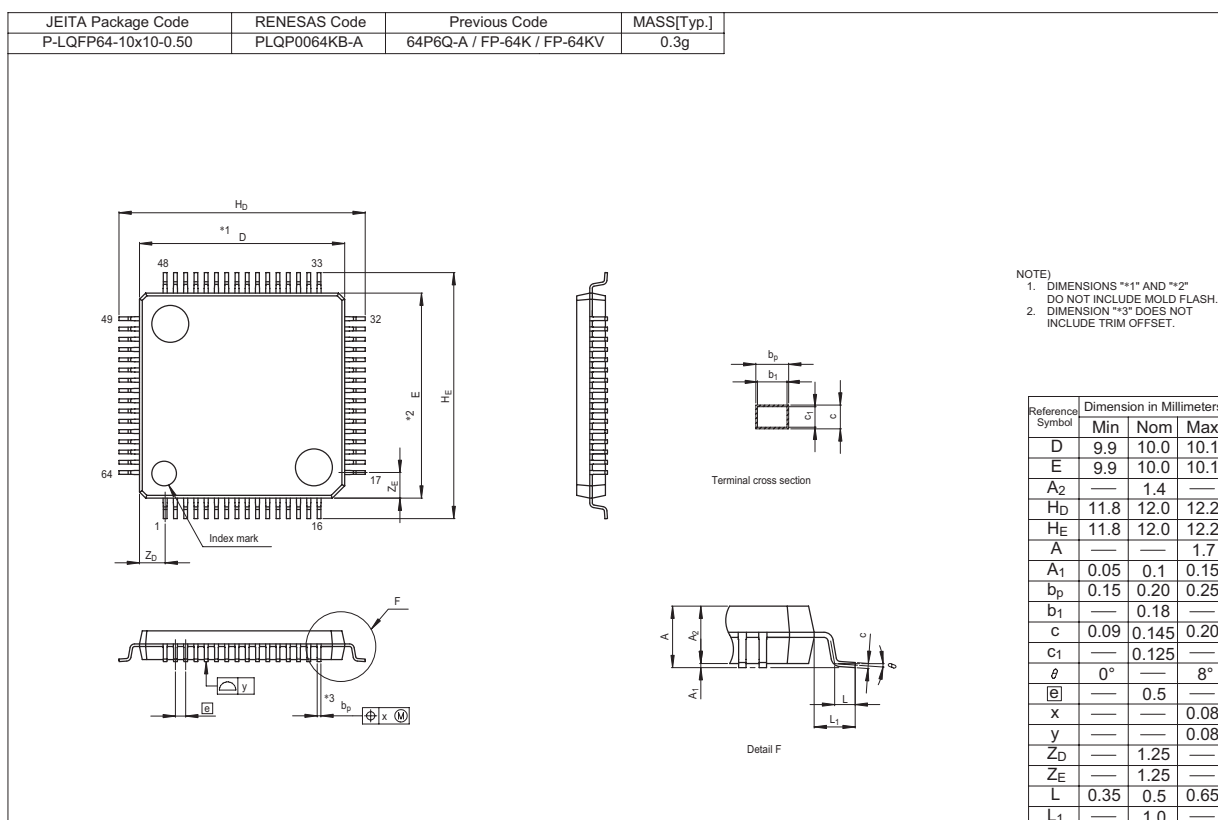
NOTES:

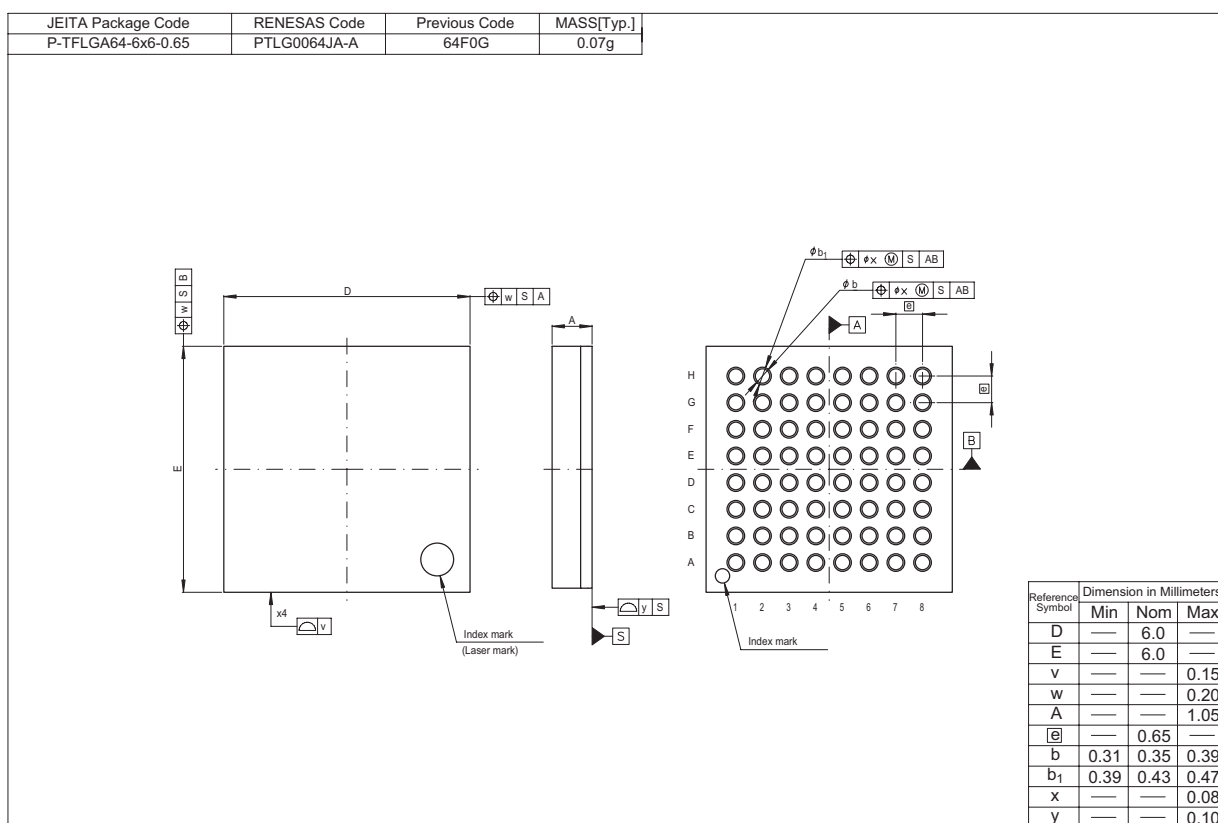
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

**Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.





REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 03, 2006	–	First Edition issued
0.10	Jun 26, 2006	All pages	Pin name revised CMP0_0 → TRFO00, CMP0_1 → TRFO01, CMP0_2 → TRFO02, CMP1_0 → TRFO10, CMP1_1 → TRFO11, CMP1_2 → TRFO12, TRFIN → TRFI
		2, 4	Table 1.1 Specifications for R8C/2A Group (1) and Table 1.3 Specifications for R8C/2B Group (1); I/O Ports: • Input-only: 3 pins → 2 pins revised Interrupts: • Internal: 17 sources → 23 sources revised
		3, 5	Table 1.2 Specifications for R8C/2A Group (2) and Table 1.4 Specifications for R8C/2B Group (2); ROM Correction Function deleted
		8	Figure 1.3 Block Diagram revised
		9	Figure 1.4 Pin Assignment (Top View) revised
		10, 11	Table 1.7 Pin Name Information by Pin Number (1) and Table 1.8 Pin Name Information by Pin Number (2) revised
		12, 13	Table 1.9 Pin Functions (1) and Table 1.10 Pin Functions (2) revised
		19	Table 4.1 SFR Information (1); • 0008h: Module Standby Control Register, MSTCR, 00h added • 001Ch: “00h” → “00h, 10000000b” revised • NOTE6 added
		20	Table 4.2 SFR Information (2); • 005Fh: Capture Interrupt Control Register, CAPIC, XXXXX000b added
		22	Table 4.4 SFR Information (4); • 00DCh: “00DDh” → “00DCh” revised • 00F5h: “XXXX00XXb” → “00h” revised
		23	Table 4.5 SFR Information (5); • 0105h: LIN Special Function Register, LINCR2, 00h added
		30	Table 4.12 SFR Information (12); • 02C2h, 02C3h: A/D Register 1, AD1, XXh deleted • 02C4h, 02C5h: A/D Register 2, AD2, XXh deleted • 02C6h, 02C7h: A/D Register 3, AD3, XXh deleted
		31	Package Dimensions; “Diagrams showing the latest package dimensions... in the “Packages” section of the Renesas Technology website.” added
0.20	Sep 15, 2006	31 to 54	5. Electrical Characteristics added
0.30	Dec 22, 2006	6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.30	Dec 22, 2006	19	Table 4.1; • 000Ah: "00XX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "0001111b" → "00X1111b" revised
		37	Table 5.11 revised
1.00	Feb 09, 2007	All pages	"Preliminary" deleted
		3	Table 1.2 revised
		5	Table 1.4 revised
		6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XX000b" → "00h" revised • 000Fh: "0001111b" → "00X1111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added
		23	Table 4.5; 0105h: "LIN Control Register 2" register name revised
		31	Table 5.2 revised
		32	Table 5.3 and Table 5.4; NOTE1 revised
		37	Table 5.11 revised
		44	Table 5.17 revised
		46	Table 5.21 and Figure 5.11; "i = 0 to 2" revised
		48	Table 5.24 revised
		50	Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised
		52	Table 5.31 revised
		53	Table 5.34 revised
		54	Table 5.35 and Figure 5.21; "i = 0 to 2" revised
2.00	Oct 17, 2007	All pages	"PTLG0064JA-A (64F0G) package" added
		3, 5	Table 1.2 and Table 1.4; • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added
		6 to 7	Table 1.5 and Figure 1.1 revised
		8	Table 1.6 and Figure 1.2 revised
		10	Figure 1.4 "64-pin LQFP Package" added
		11	Figure 1.5 added
		19 to 20	Figure 3.1 and Figure 3.2 revised
		24	Table 4.4; 00F5h: "00h" → "000000XXb" revised

Notes:

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