# Renesas Electronics America Inc - R5F212A8SDFA#V2 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 55 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212a8sdfa-v2 |

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## 1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

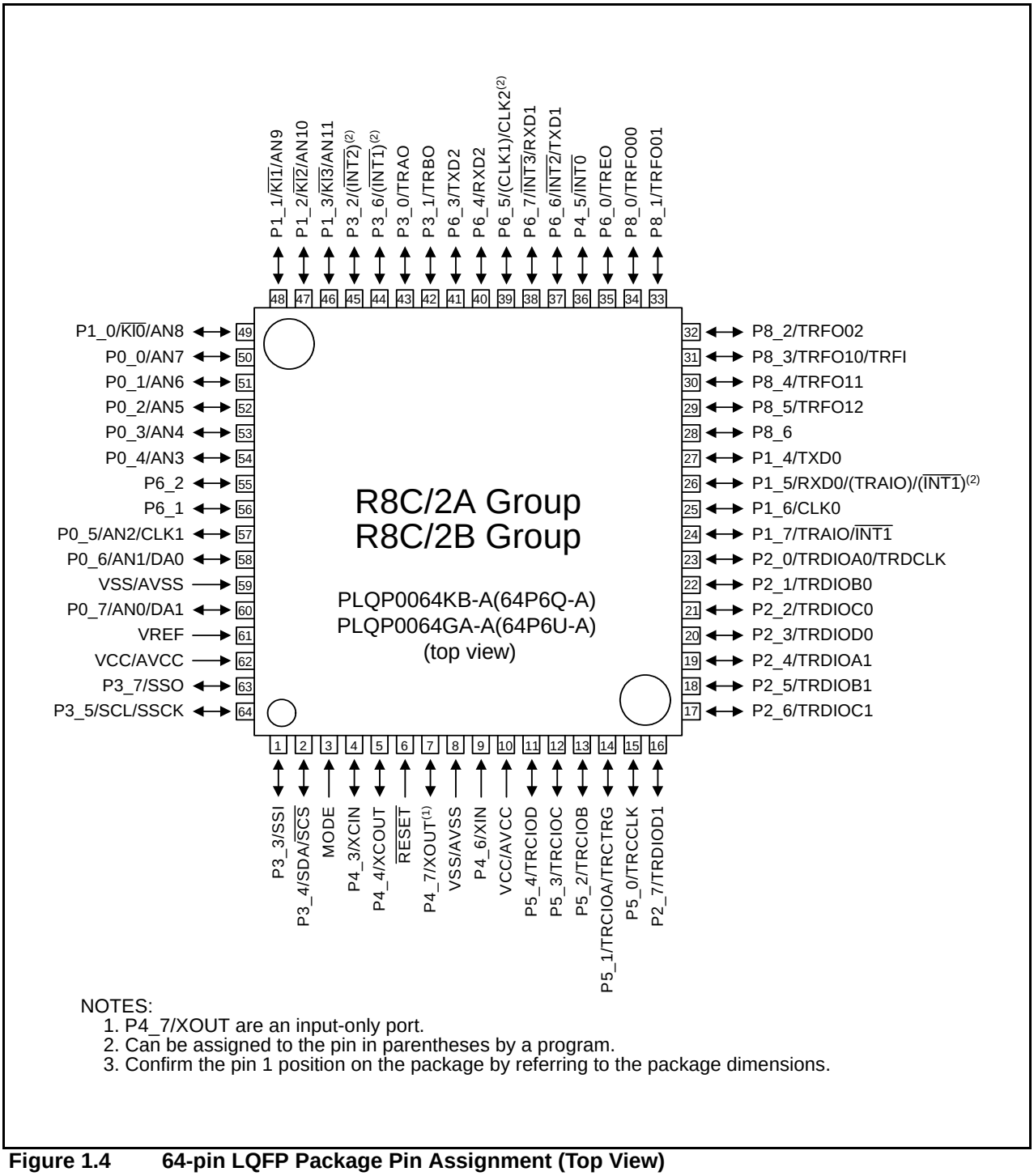
**Table 1.5 Product List for R8C/2A Group** **Current of Nov. 2007**

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks | |
|---|---|---|---|---|---|
| R5F212A7SNFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | N version | |
| R5F212A7SNFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNLG | 48 Kbytes | 2.5 Kbytes | PTLG0064JA-A | | |
| R5F212A8SNFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SNFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212A8SNLG | 64 Kbytes | 3 Kbytes | PLTG0064JA-A | | |
| R5F212AASNFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASNFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212AASNLG | 96 Kbytes | 7 Kbytes | PLTG0064JA-A | | |
| R5F212ACSNFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSNFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212ACSNLG | 128 Kbytes | 7.5 Kbytes | PLTG0064JA-A | | |
| R5F212A7SDFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | D version | |
| R5F212A7SDFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A8SDFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SDFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212AASDFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASDFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212ACSDFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSDFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNXXXFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | N version | Factory programming product(1) |
| R5F212A7SNXXXFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNXXXLG | 48 Kbytes | 2.5 Kbytes | PTLG0064JA-A | | |
| R5F212A8SNXXXFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SNXXXFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212A8SNXXXLG | 64 Kbytes | 3 Kbytes | PLTG0064JA-A | | |
| R5F212AASNXXXFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASNXXXFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212AASNXXXLG | 96 Kbytes | 7 Kbytes | PLTG0064JA-A | | |
| R5F212ACSNXXXFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSNXXXFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212ACSNXXXLG | 128 Kbytes | 7.5 Kbytes | PLTG0064JA-A | | |
| R5F212A7SDXXXFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | D version | |
| R5F212A7SDXXXFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A8SDXXXFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SDXXXFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212AASDXXXFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASDXXXFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212ACSDXXXFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSDXXXFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |

NOTE:
1. The user ROM is programmed before shipment.

## 1.4 Pin Assignment

Figure 1.4 shows 64-pin LQFP Package Pin Assignment (Top View). Figure 1.5 shows 64-pin FLGA Package Pin Assignment (Top Perspective View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.




NOTES:
1. P4_7/XOUT are an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

**Figure 1.4 64-pin LQFP Package Pin Assignment (Top View)**

**Table 1.7 Pin Name Information by Pin Number (1)**

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | $I^2C$ bus | A/D Converter, D/A Converter |
| 1 | | P3_3 | | | | SSI | | |
| 2 | | P3_4 | | | | SCS | SDA | |
| 3 | MODE | | | | | | | |
| 4 | XCIN | P4_3 | | | | | | |
| 5 | XCOUT | P4_4 | | | | | | |
| 6 | $\overline{\text{RESET}}$ | | | | | | | |
| 7 | XOUT | P4_7 | | | | | | |
| 8 | VSS/AVSS | | | | | | | |
| 9 | XIN | P4_6 | | | | | | |
| 10 | VCC/AVCC | | | | | | | |
| 11 | | P5_4 | | TRCIOD | | | | |
| 12 | | P5_3 | | TRCIOC | | | | |
| 13 | | P5_2 | | TRCIOB | | | | |
| 14 | | P5_1 | | TRCIOA/TRCTRG | | | | |
| 15 | | P5_0 | | TRCCLK | | | | |
| 16 | | P2_7 | | TRDIOD1 | | | | |
| 17 | | P2_6 | | TRDIOC1 | | | | |
| 18 | | P2_5 | | TRDIOB1 | | | | |
| 19 | | P2_4 | | TRDIOA1 | | | | |
| 20 | | P2_3 | | TRDIOD0 | | | | |
| 21 | | P2_2 | | TRDIOC0 | | | | |
| 22 | | P2_1 | | TRDIOB0 | | | | |
| 23 | | P2_0 | | TRDIOA0/TRDCLK | | | | |
| 24 | | P1_7 | $\overline{\text{INT1}}$ | TRAIO | | | | |
| 25 | | P1_6 | | | CLK0 | | | |
| 26 | | P1_5 | ($\overline{\text{INT1}}$)(1) | (TRAIO)(1) | RXD0 | | | |
| 27 | | P1_4 | | | TXD0 | | | |
| 28 | | P8_6 | | | | | | |
| 29 | | P8_5 | | TRFO12 | | | | |
| 30 | | P8_4 | | TRFO11 | | | | |
| 31 | | P8_3 | | TRFO10/TRFI | | | | |
| 32 | | P8_2 | | TRFO02 | | | | |
| 33 | | P8_1 | | TRFO01 | | | | |
| 34 | | P8_0 | | TRFO00 | | | | |
| 35 | | P6_0 | | TREO | | | | |
| 36 | | P4_5 | $\overline{\text{INT0}}$ | $\overline{\text{INT0}}$ | | | | |
| 37 | | P6_6 | $\overline{\text{INT2}}$ | | TXD1 | | | |
| 38 | | P6_7 | $\overline{\text{INT3}}$ | | RXD1 | | | |
| 39 | | P6_5 | | | (CLK1)(1)/ CLK2 | | | |
| 40 | | P6_4 | | | RXD2 | | | |
| 41 | | P6_3 | | | TXD2 | | | |
| 42 | | P3_1 | | TRBO | | | | |
| 43 | | P3_0 | | TRAO | | | | |
| 44 | | P3_6 | ($\overline{\text{INT1}}$)(1) | | | | | |
| 45 | | P3_2 | ($\overline{\text{INT2}}$)(1) | | | | | |

NOTE:
1. Can be assigned to the pin in parentheses by a program.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

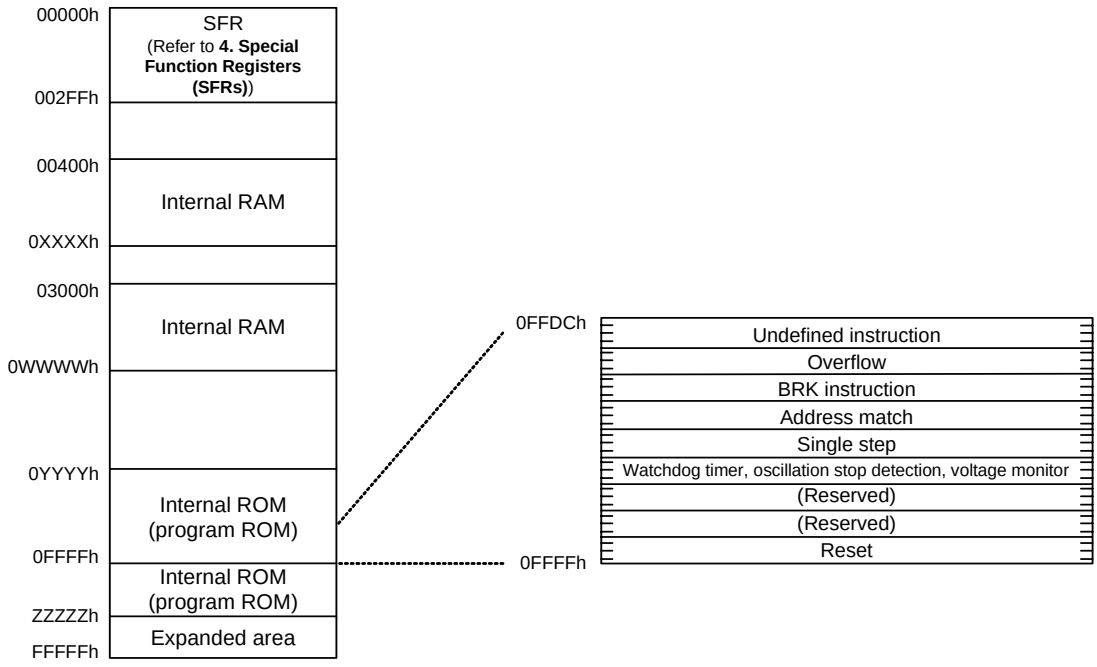
### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

# 3. Memory

## 3.1 R8C/2A Group

Figure 3.1 is a Memory Map of R8C/2A Group. The R8C/2A group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

| Internal ROM | | | Internal RAM | | |
|---|---|---|---|---|---|
| Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh | Address 0WWWWh |
| 48 Kbytes | 04000h | – | 2.5 Kbytes | 00DFFh | – |
| 64 Kbytes | 04000h | 13FFFh | 3 Kbytes | 00FFFh | – |
| 96 Kbytes | 04000h | 1BFFFh | 7 Kbytes | 011FFh | 03DFFh |
| 128 Kbytes | 04000h | 23FFFh | 7.5 Kbytes | 011FFh | 03FFFh |

**Figure 3.1 Memory Map of R8C/2A Group**

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

**Table 4.1 SFR Information (1)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Module Operation Enable Register | MSTCR | 00h |
| 0009h | | | |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00X11111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | 00h |
| 0013h | Address Match Interrupt Enable Register | AIER | 00h |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | 00h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h<br>10000000b[6] |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | | | |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag | CPSRF | 00h |
| 0029h | | | |
| 002Ah | | | |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When Shipping |
| 0030h | | | |
| 0031h | Voltage Detection Register 1[2] | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2[2] | VCA2 | 00h[3]<br>00100000b[4] |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register[5] | VW1C | 00001000b |
| 0037h | Voltage Monitor 2 Circuit Control Register[5] | VW2C | 00h |
| 0038h | Voltage Monitor 0 Circuit Control Register[2] | VW0C | 0000X000b[3]<br>0100X001b[4] |
| 0039h | | | |
| 003Ah | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

**Table 4.3 SFR Information (3)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 00A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 00AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 00ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 00AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 00AFh | | | XXh |
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | SS Control Register H / IIC bus Control Register 1(2) | SSCRH / ICCR1 | 00h |
| 00B9h | SS Control Register L / IIC bus Control Register 2(2) | SSCRL / ICCR2 | 01111101b |
| 00BAh | SS Mode Register / IIC bus Mode Register(2) | SSMR / ICMR | 00011000b |
| 00BBh | SS Enable Register / IIC bus Interrupt Enable Register(2) | SSER / ICIER | 00h |
| 00BCh | SS Status Register / IIC bus Status Register(2) | SSSR / ICSR | 00h / 0000X000b |
| 00BDh | SS Mode Register 2 / Slave Address Register(2) | SSMR2 / SAR | 00h |
| 00BEh | SS Transmit Data Register / IIC bus Transmit Data Register(2) | SSTDR / ICDRT | FFh |
| 00BFh | SS Receive Data Register / IIC bus Receive Data Register(2) | SSRDR / ICDRR | FFh |

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

**Table 4.7 SFR Information (7)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0180h | | | |
| 0181h | | | |
| 0182h | | | |
| 0183h | | | |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | | | |
| 0189h | | | |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 4.11 SFR Information (11)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0280h | | | |
| 0281h | | | |
| 0282h | | | |
| 0283h | | | |
| 0284h | | | |
| 0285h | | | |
| 0286h | | | |
| 0287h | | | |
| 0288h | | | |
| 0289h | | | |
| 028Ah | | | |
| 028Bh | | | |
| 028Ch | | | |
| 028Dh | | | |
| 028Eh | | | |
| 028Fh | | | |
| 0290h | Timer RF Register | TRF | 00h |
| 0291h | | | 00h |
| 0292h | | | |
| 0293h | | | |
| 0294h | | | |
| 0295h | | | |
| 0296h | | | |
| 0297h | | | |
| 0298h | | | |
| 0299h | | | |
| 029Ah | Timer RF Control Register 0 | TRFCR0 | 00h |
| 029Bh | Timer RF Control Register 1 | TRFCR1 | 00h |
| 029Ch | Capture / Compare 0 Register | TRFM0 | 0000h[2] |
| 029Dh | | | FFFFh[3] |
| 029Eh | Compare 1 Register | TRFM1 | FFh |
| 029Fh | | | FFh |
| 02A0h | | | |
| 02A1h | | | |
| 02A2h | | | |
| 02A3h | | | |
| 02A4h | | | |
| 02A5h | | | |
| 02A6h | | | |
| 02A7h | | | |
| 02A8h | | | |
| 02A9h | | | |
| 02AAh | | | |
| 02ABh | | | |
| 02ACh | | | |
| 02ADh | | | |
| 02AEh | | | |
| 02AFh | | | |
| 02B0h | | | |
| 02B1h | | | |
| 02B2h | | | |
| 02B3h | | | |
| 02B4h | | | |
| 02B5h | | | |
| 02B6h | | | |
| 02B7h | | | |
| 02B8h | | | |
| 02B9h | | | |
| 02BAh | | | |
| 02BBh | | | |
| 02BCh | | | |
| 02BDh | | | |
| 02BEh | | | |
| 02BFh | | | |

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

**Table 4.12 SFR Information (12)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 02C0h | A/D Register 0 | AD0 | XXh |
| 02C1h | | | XXh |
| 02C2h | | | |
| 02C3h | | | |
| 02C4h | | | |
| 02C5h | | | |
| 02C6h | | | |
| 02C7h | | | |
| 02C8h | | | |
| 02C9h | | | |
| 02CAh | | | |
| 02CBh | | | |
| 02CCh | | | |
| 02CDh | | | |
| 02CEh | | | |
| 02CFh | | | |
| 02D0h | | | |
| 02D1h | | | |
| 02D2h | | | |
| 02D3h | | | |
| 02D4h | A/D Control Register 2 | ADCON2 | 00001000b |
| 02D5h | | | |
| 02D6h | A/D Control Register 0 | ADCON0 | 00000011b |
| 02D7h | A/D Control Register 1 | ADCON1 | 00h |
| 02D8h | | | |
| 02D9h | | | |
| 02DAh | | | |
| 02DBh | | | |
| 02DCh | | | |
| 02DDh | | | |
| 02DEh | | | |
| 02DFh | | | |
| 02E0h | | | |
| 02E1h | | | |
| 02E2h | | | |
| 02E3h | | | |
| 02E4h | Port P8 Direction Register | PD8 | 00h |
| 02E5h | | | |
| 02E6h | Port P8 Register | P8 | XXh |
| 02E7h | | | |
| 02E8h | | | |
| 02E9h | | | |
| 02EAh | | | |
| 02EBh | | | |
| 02ECh | | | |
| 02EDh | | | |
| 02EEh | | | |
| 02EFh | | | |
| 02F0h | | | |
| 02F1h | | | |
| 02F2h | | | |
| 02F3h | | | |
| 02F4h | | | |
| 02F5h | | | |
| 02F6h | | | |
| 02F7h | | | |
| 02F8h | | | |
| 02F9h | | | |
| 02FAh | | | |
| 02FBh | | | |
| 02FCh | Pull-Up Control Register 2 | PUR2 | XXX00000b |
| 02FDh | | | |
| 02FEh | | | |
| 02FFh | Timer RF Output Control Register | TRFOUT | 00h |
| FFFFh | Option Function Select Register | OFS | (Note 2) |

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

# 5. Electrical Characteristics

The electrical characteristics of N version (Topr = –20°C to 85°C) and D version (Topr = –40°C to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = –20°C to 105°C).

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | -0.3 to 6.5 | V |
| $V_I$ | Input voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | $T_{opr}$ = 25°C | 700 | mW |
| $T_{opr}$ | Operating ambient temperature | | -20 to 85 (N version) / -40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |

**Table 5.5 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | R8C/2A Group | 100(3) | – | – | times |
| | | R8C/2B Group | 1,000(3) | – | – | times |
| – | Byte program time | | – | 50 | 400 | µs |
| – | Block erase time | | – | 0.4 | 9 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time(7) | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.6 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)**

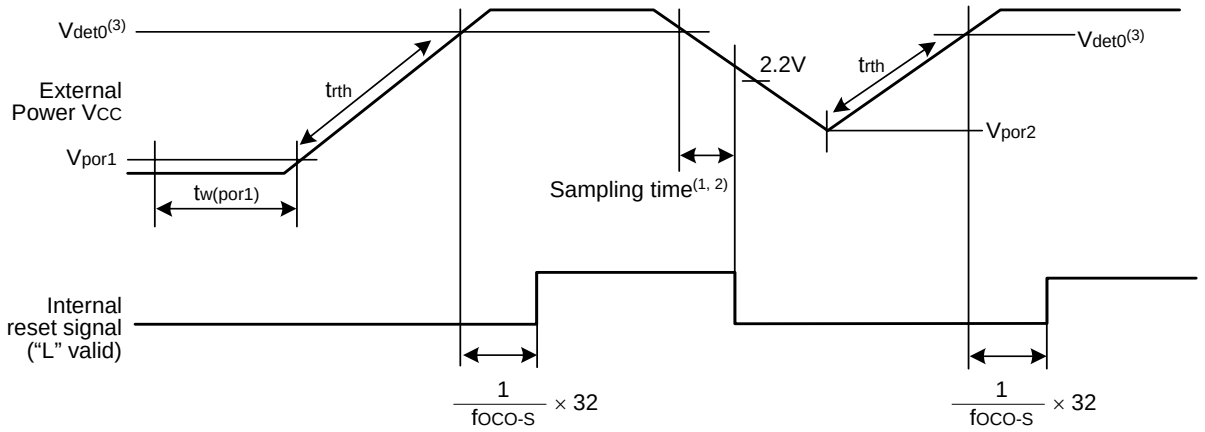
| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | | 10,000(3) | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | µs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | µs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | -20(8) | – | 85 | °C |
| – | Data hold time(9) | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage(4) | | – | – | 0.1 | V |
| $V_{por2}$ | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | $V_{det0}$ | V |
| $t_{rth}$ | External power $V_{CC}$ rise gradient(2) | | 20 | – | – | mV/msec |

NOTES:
1. The measurement condition is $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power VCC rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power $V_{CC}$ must be held below the effective voltage ($V_{por1}$) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if $-20°C \leq T_{opr} \leq 85°C$, maintain $t_{w(por1)}$ for 3,000 s or more if $-40°C \leq T_{opr} < -20°C$.




NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

**Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{SUCYC}$ | SSCK clock cycle time | | | 4 | – | – | $t_{CYC}$(2) |
| $t_{HI}$ | SSCK clock “H” width | | | 0.4 | – | 0.6 | $t_{SUCYC}$ |
| $t_{LO}$ | SSCK clock “L” width | | | 0.4 | – | 0.6 | $t_{SUCYC}$ |
| $t_{RISE}$ | SSCK clock rising time | Master | | – | – | 1 | $t_{CYC}$(2) |
| | | Slave | | – | – | 1 | µs |
| $t_{FALL}$ | SSCK clock falling time | Master | | – | – | 1 | $t_{CYC}$(2) |
| | | Slave | | – | – | 1 | µs |
| $t_{SU}$ | SSO, SSI data input setup time | | | 100 | – | – | ns |
| $t_H$ | SSO, SSI data input hold time | | | 1 | – | – | $t_{CYC}$(2) |
| $t_{LEAD}$ | $\overline{SCS}$ setup time | Slave | | 1$t_{CYC}$ + 50 | – | – | ns |
| $t_{LAG}$ | $\overline{SCS}$ hold time | Slave | | 1$t_{CYC}$ + 50 | – | – | ns |
| $t_{OD}$ | SSO, SSI data output delay time | | | – | – | 1 | $t_{CYC}$(2) |
| $t_{SA}$ | SSI slave access time | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 1.5$t_{CYC}$ + 100 | ns |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | – | – | 1.5$t_{CYC}$ + 200 | ns |
| $t_{OR}$ | SSI slave out open time | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 1.5$t_{CYC}$ + 100 | ns |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | – | – | 1.5$t_{CYC}$ + 200 | ns |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $V_{SS}$ = 0 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1$t_{CYC}$ = 1/f1(s)

**Table 5.16 Electrical Characteristics (1) [$V_{CC}$ = 5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = -5 mA | | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | $I_{OH}$ = -200 µA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = -20 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = -5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -1 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = -500 µA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 5 mA | | – | – | 2.0 | V |
| | | | $I_{OL}$ = 200 µA | | – | – | 0.45 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 500 µA | – | – | 2.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.0 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | -5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 30 | 50 | 167 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 18 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. $V_{CC}$ = 4.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.28 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 to 2

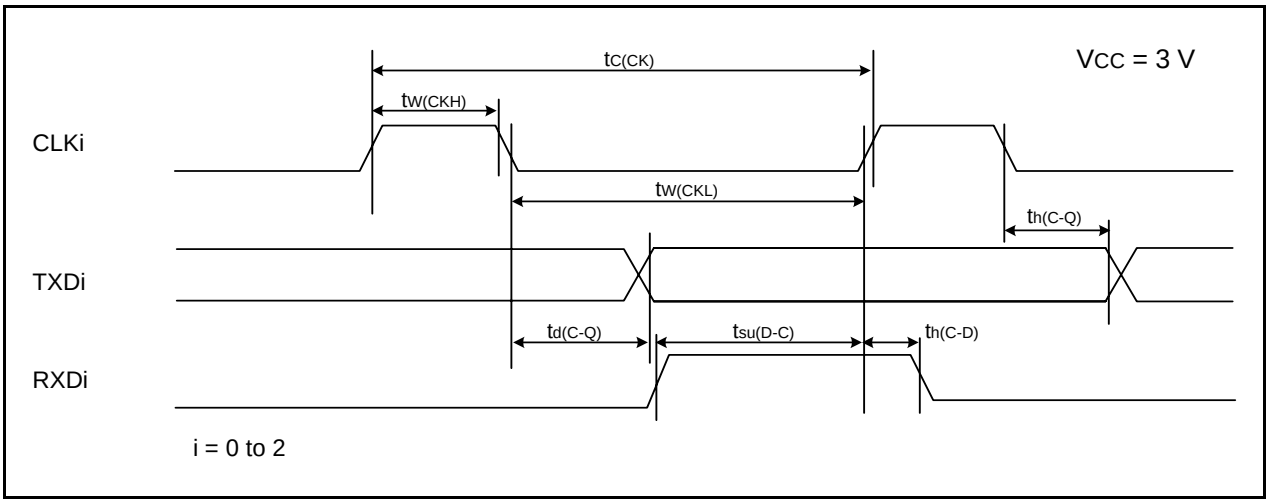



**Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.29 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

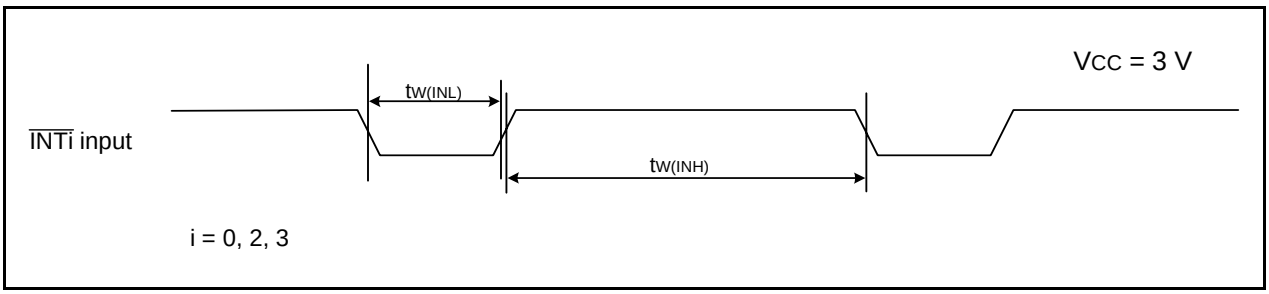



**Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V**

**Table 5.31 Electrical Characteristics (6) [Vcc = 2.2 V]**
**(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 2.5 | – | mA |
| | | | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 4 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.7 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 110 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>FMR47 = 1 | – | 125 | 350 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>Program operation on RAM<br>Flash memory off, FMSTP = 1 | – | 27 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 20 | 60 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 12 | 40 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (high drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 2.8 | – | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (low drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 1.9 | – | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.6 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.60 | – | µA |

| REVISION HISTORY | R8C/2A Group, R8C/2B Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Oct 17, 2007 | 33 | Table 5.1;<br>Pd: Rated Value “TBD” → “700” revised, “NOTE1” added |
| | | 59 | Package Dimensions “PTLG0064JA-A (64F0G) package” added |
| 2.10 | Nov 26, 2007 | 2, 4 | Table 1.1, Table 1.3 Clock: “Real-time clock (timer RE)” added |
| | | 6, 7 | Table 1.5 and Figure 1.1 revised |
| | | 8, 9 | Table 1.6 and Figure 1.2 revised |
| | | 20, 21 | Figure 3.1 and Figure 3.2 revised |
| | | 22 | Table 4.1 002Ch: High-Speed On-Chip Oscillator Control Register 7 added |
| | | 35 | Table 5.2 NOTE2 revised |
| | | 41 | Table 5.11 revised |
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