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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212aasdfa-v2

1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2A Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2B Group.

Table 1.1 Specifications for R8C/2A Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) • Multiplier: 16 bits $\times$ 16 bits $\rightarrow$ 32 bits • Multiply-accumulate instruction: 16 bits $\times$ 16 bits + 32 bits $\rightarrow$ 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to Table 1.5 Product List for R8C/2A Group .
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: - Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits $\times$ 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits $\times$ 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits $\times$ 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits $\times$ 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits $\times$ 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode

Table 1.4 Specifications for R8C/2B Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I ² C-bus)
I ² C bus ⁽¹⁾		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

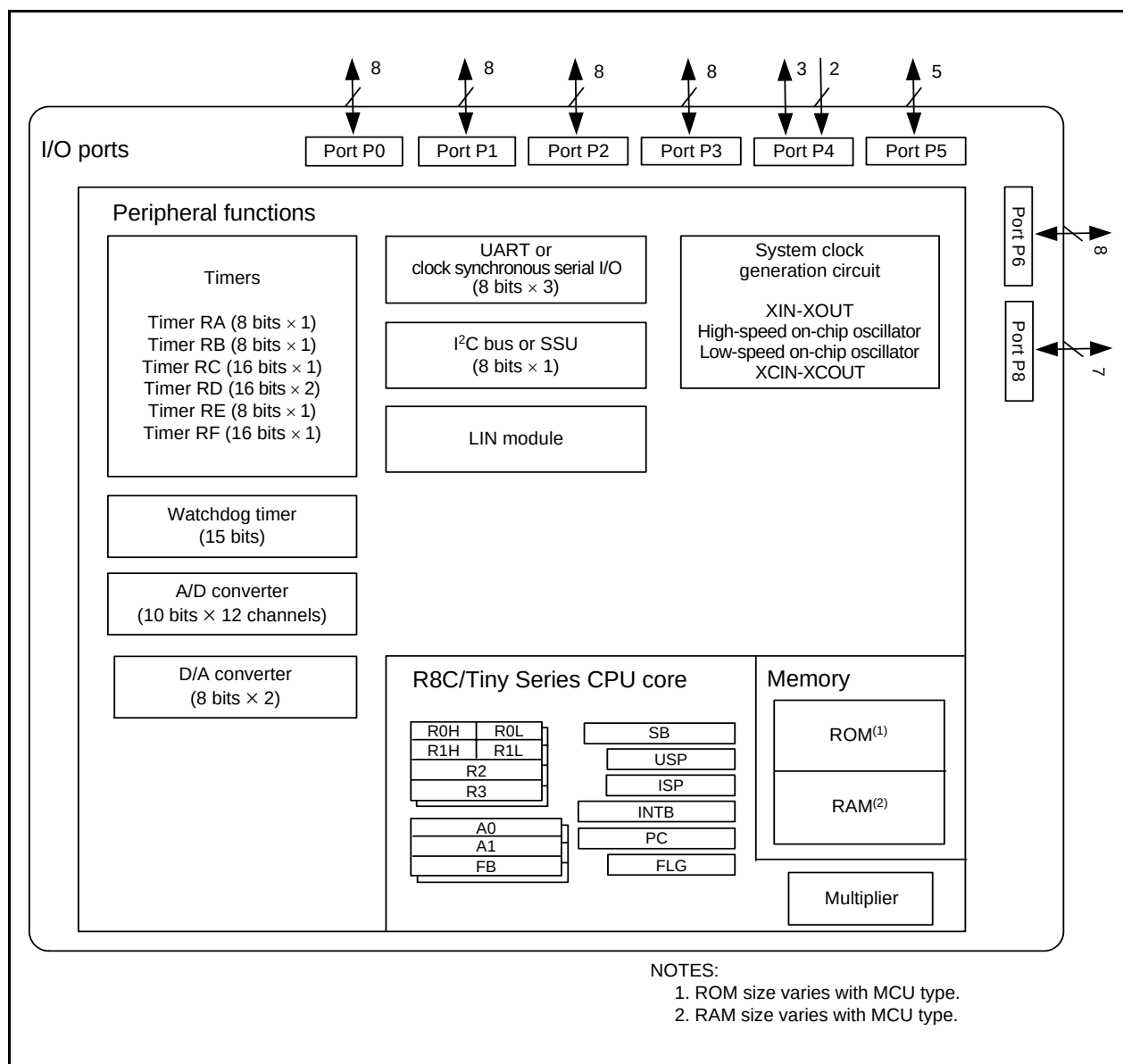


Figure 1.3 Block Diagram

Table 1.8 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter
46		P1_3	$\overline{\text{KI3}}$					AN11
47		P1_2	$\overline{\text{KI2}}$					AN10
48		P1_1	$\overline{\text{KI1}}$					AN9
49		P1_0	$\overline{\text{KI0}}$					AN8
50		P0_0						AN7
51		P0_1						AN6
52		P0_2						AN5
53		P0_3						AN4
54		P0_4						AN3
55		P6_2						
56		P6_1						
57		P0_5			CLK1			AN2
58		P0_6						AN1/DA0
59	VSS/AVSS							
60		P0_7						AN0/DA1
61	VREF							
62	VCC/AVCC							
63		P3_7				SSO		
64		P3_5				SSCK	SCL	

1.5 Pin Functions

Tables 1.9 and 1.10 list Pin Functions.

Table 1.9 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO12	O	Timer RF output pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

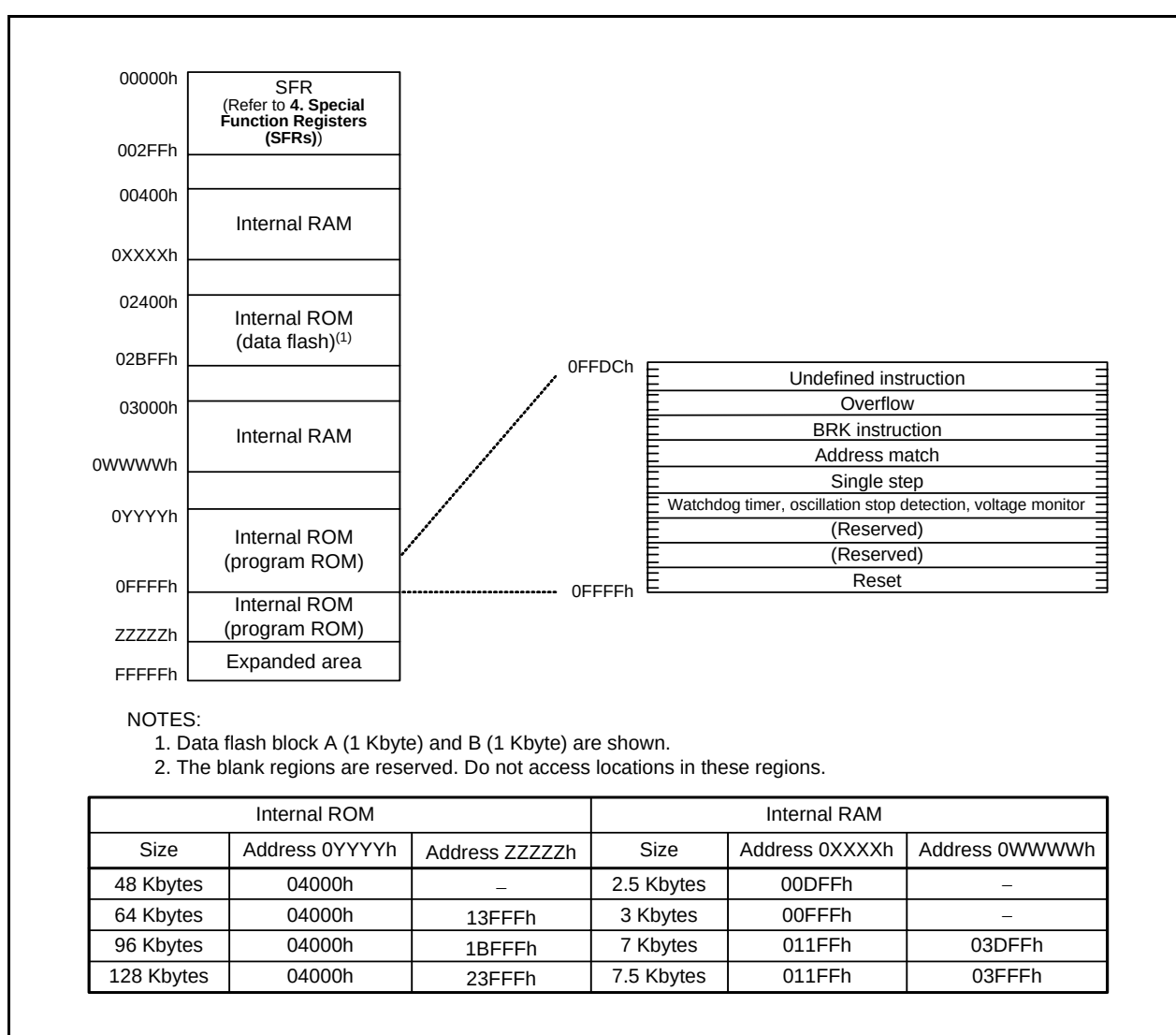


Figure 3.2 Memory Map of R8C/2B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Operation Enable Register	MSTCR	00h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁶⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	000000XXb
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX000000b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)(1)

Address	Register	Symbol	After reset
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh			
026Fh			
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

The electrical characteristics of N version ($T_{opr} = -20^{\circ}\text{C}$ to 85°C) and D version ($T_{opr} = -40^{\circ}\text{C}$ to 85°C) are listed below.

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version ($T_{opr} = -20^{\circ}\text{C}$ to 105°C).

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to $V_{CC} + 0.3$	V
V_O	Output voltage		-0.3 to $V_{CC} + 0.3$	V
P_d	Power dissipation	$T_{opr} = 25^{\circ}\text{C}$	700	mW
T_{opr}	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-65 to 150	$^{\circ}\text{C}$

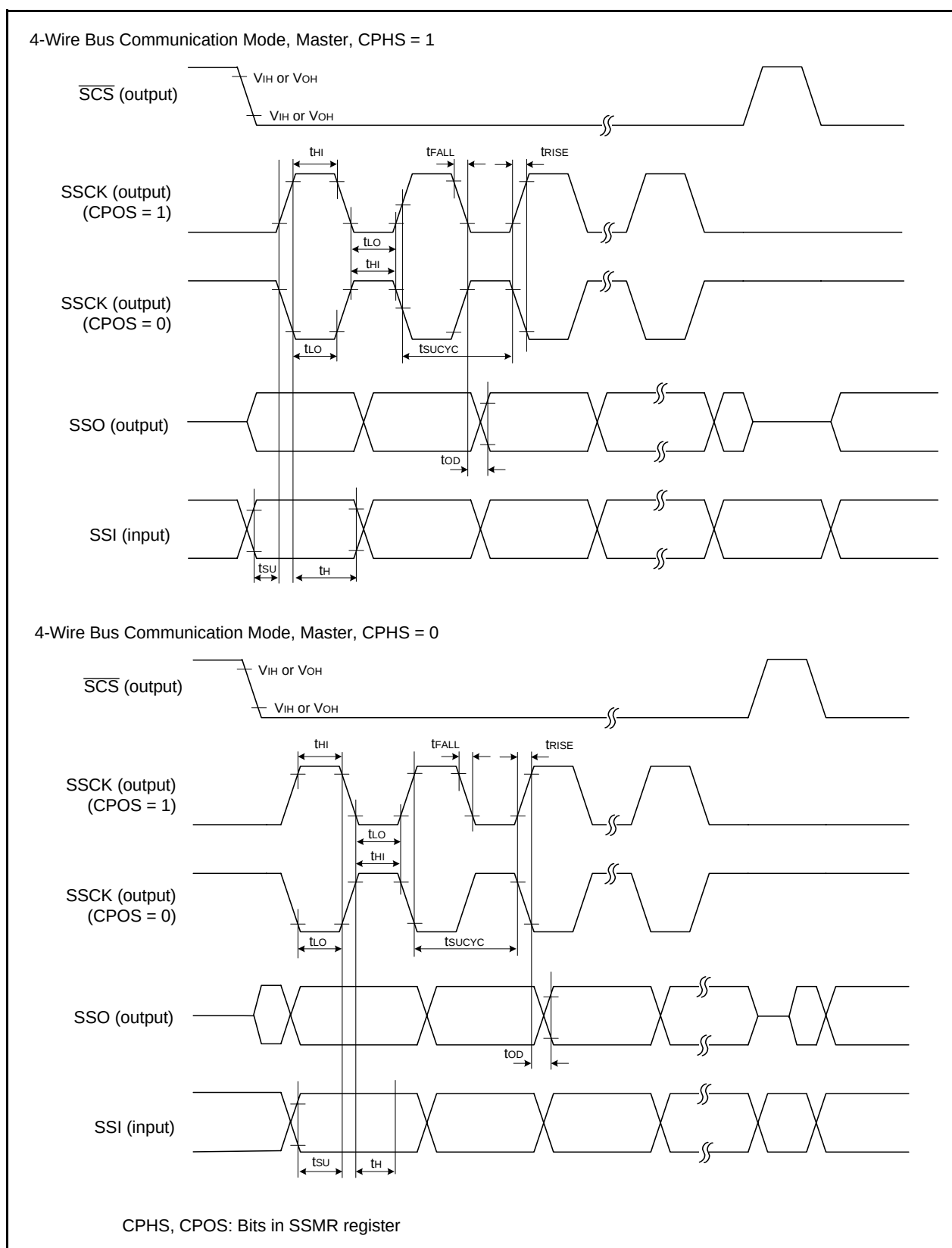


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

Table 5.16 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μ A	V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μ A	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μ A	—	—	0.45	V
		P2_0 to P2_7	Drive capacity HIGH I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μ A	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	<u>INT0</u> , <u>INT1</u> , <u>INT2</u> , <u>INT3</u> , <u>KI0</u> , <u>KI1</u> , <u>KI2</u> , <u>KI3</u> , <u>TRAIO</u> , <u>TRFI</u> , <u>RXD0</u> , <u>RXD1</u> , <u>CLK0</u> , <u>CLK1</u> , <u>CLK2</u> , <u>SSI</u> , <u>SCL</u> , <u>SDA</u> , <u>SSO</u>		0.1	0.5	—	V
		<u>RESET</u>		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V	—	—	5.0	μ A
I _{IL}	Input "L" current		V _I = 0 V	—	—	-5.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V	30	50	167	k Ω
R _{FXIN}	Feedback resistance	XIN		—	1.0	—	M Ω
R _{FXCIN}	Feedback resistance	XCIN		—	18	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.17 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	12	20	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	10	16	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	7	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	5.5	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4.5	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	6	12	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	150	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	—	150	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	—	35	—	μA
			Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	30	90
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1		—	18	55	μA
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1		—	3.5	—	μA
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1		—	2.3	—	μA
		Stop mode		XIN clock off, T _{opr} = 25°C High-speed oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.7	3.0
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	1.7	—	μA

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

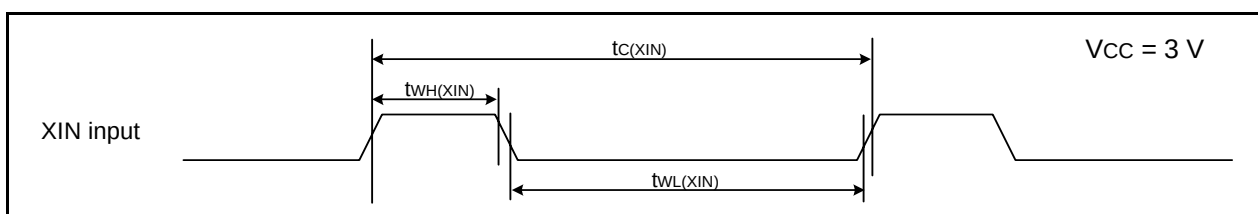
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

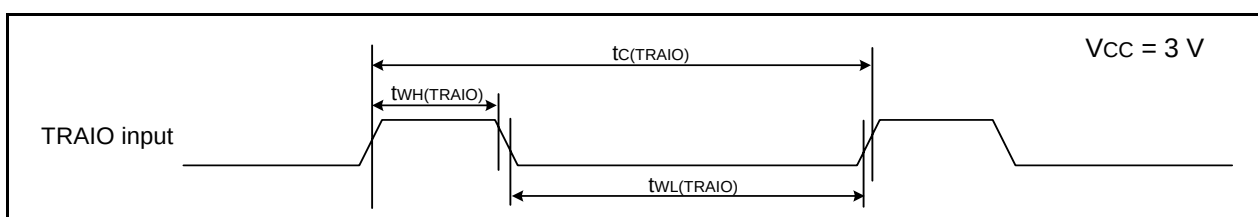
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.25 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.13 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.26 TRAIO Input, $\overline{\text{INT1}}$ Input**

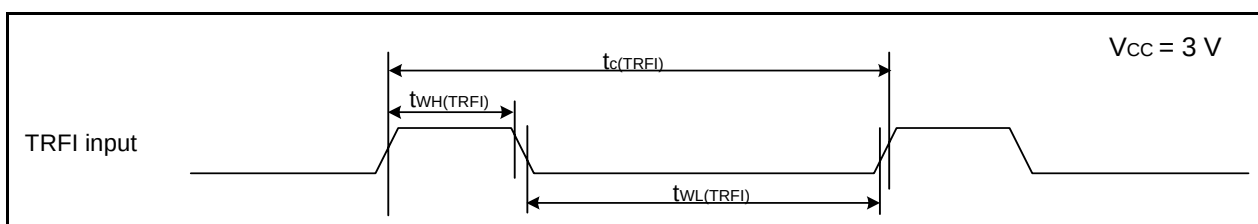
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

**Figure 5.14 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	1200 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	600 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	600 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

**Figure 5.15 TRFI Input Timing Diagram when $V_{CC} = 3\text{ V}$**

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
2.00	Oct 17, 2007	33	Table 5.1; Pd: Rated Value "TBD" → "700" revised, "NOTE1" added
		59	Package Dimensions "PTLG0064JA-A (64F0G) package" added
2.10	Nov 26, 2007	2, 4	Table 1.1, Table 1.3 Clock: "Real-time clock (timer RE)" added
		6, 7	Table 1.5 and Figure 1.1 revised
		8, 9	Table 1.6 and Figure 1.2 revised
		20, 21	Figure 3.1 and Figure 3.2 revised
		22	Table 4.1 002Ch: High-Speed On-Chip Oscillator Control Register 7 added
		35	Table 5.2 NOTE2 revised
		41	Table 5.11 revised

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