Renesas Electronics America Inc - R5F212AASNLG#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFLGA
Supplier Device Package	64-TFLGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212aasnlg-u0

1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2A Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2B Group.

Table 1.1 Specifications for R8C/2A Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.5 Product List for R8C/2A Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode

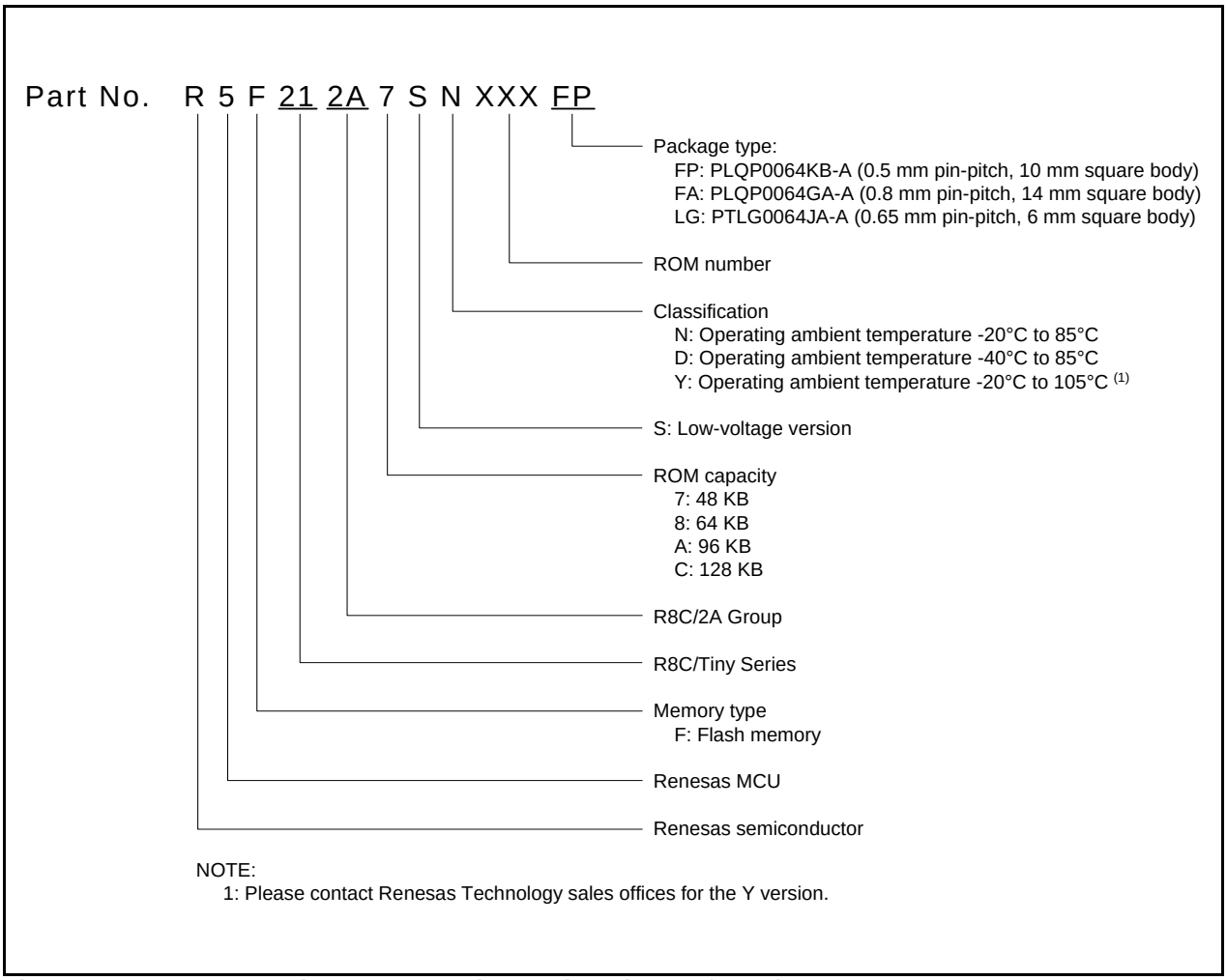
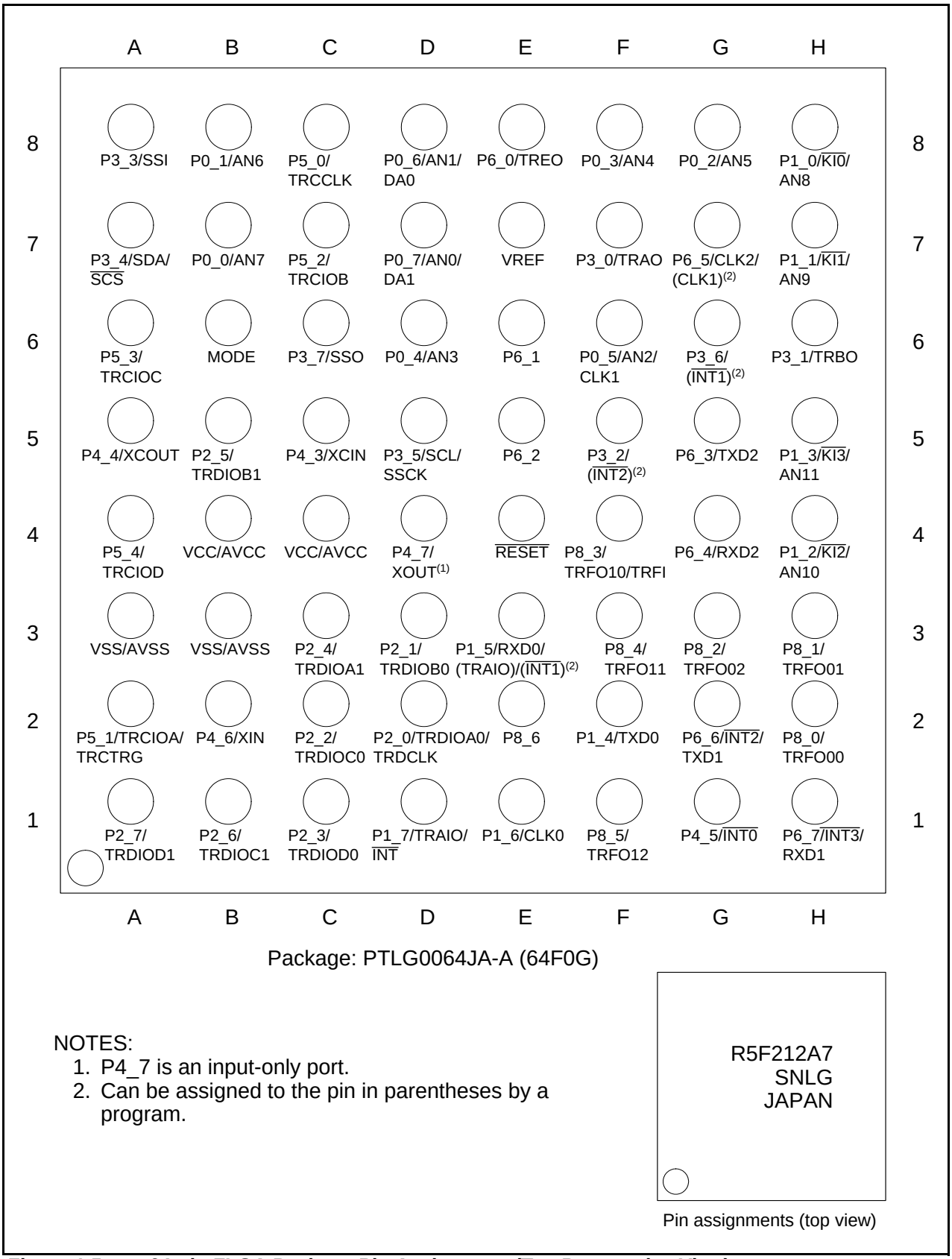


Figure 1.1 Part Number, Memory Size, and Package of R8C/2A Group

Table 1.6 Product List for R8C/2B Group **Current of Nov. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F212B7SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	N version	
R5F212B7SNFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B7SNLG	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PTLG0064JA-A		
R5F212B8SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SNFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212B8SNLG	64 Kbytes	1 Kbyte × 2	3 Kbytes	PTLG0064JA-A		
R5F212BASNFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASNFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BASNLG	96 Kbytes	1 Kbyte × 2	7 Kbytes	PTLG0064JA-A		
R5F212BCSNFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSNFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212BCSNLG	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PTLG0064JA-A		
R5F212B7SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	D version	
R5F212B7SDFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B8SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SDFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212BASDFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASDFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BCSDFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSDFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212B7SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product(1)
R5F212B7SNXXXFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B7SNXXXLG	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PTLG0064JA-A		
R5F212B8SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SNXXXFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212B8SNXXXLG	64 Kbytes	1 Kbyte × 2	3 Kbytes	PTLG0064JA-A		
R5F212BASNXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASNXXXFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BASNXXXLG	96 Kbytes	1 Kbyte × 2	7 Kbytes	PTLG0064JA-A		
R5F212BCSNXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSNXXXFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212BCSNXXXLG	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PTLG0064JA-A		
R5F212B7SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	D version	
R5F212B7SDXXXFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B8SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SDXXXFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212BASDXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASDXXXFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BCSDXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSDXXXFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		

NOTE:
1. The user ROM is programmed before shipment.



Package: PTLG0064JA-A (64F0G)

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.

Pin assignments (top view)

Figure 1.5 64-pin FLGA Package Pin Assignment (Top Perspective View)

Table 1.7 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter
1		P3_3				SSI		
2		P3_4				SCS	SDA	
3	MODE							
4	XCIN	P4_3						
5	XCOUT	P4_4						
6	$\overline{\text{RESET}}$							
7	XOUT	P4_7						
8	VSS/AVSS							
9	XIN	P4_6						
10	VCC/AVCC							
11		P5_4		TRCIOD				
12		P5_3		TRCIOC				
13		P5_2		TRCIOB				
14		P5_1		TRCIOA/TRCTRG				
15		P5_0		TRCCLK				
16		P2_7		TRDIOD1				
17		P2_6		TRDIOC1				
18		P2_5		TRDIOB1				
19		P2_4		TRDIOA1				
20		P2_3		TRDIOD0				
21		P2_2		TRDIOC0				
22		P2_1		TRDIOB0				
23		P2_0		TRDIOA0/TRDCLK				
24		P1_7	$\overline{\text{INT1}}$	TRAIO				
25		P1_6			CLK0			
26		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0			
27		P1_4			TXD0			
28		P8_6						
29		P8_5		TRFO12				
30		P8_4		TRFO11				
31		P8_3		TRFO10/TRFI				
32		P8_2		TRFO02				
33		P8_1		TRFO01				
34		P8_0		TRFO00				
35		P6_0		TREO				
36		P4_5	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$				
37		P6_6	$\overline{\text{INT2}}$		TXD1			
38		P6_7	$\overline{\text{INT3}}$		RXD1			
39		P6_5			(CLK1)(1)/ CLK2			
40		P6_4			RXD2			
41		P6_3			TXD2			
42		P3_1		TRBO				
43		P3_0		TRAO				
44		P3_6	($\overline{\text{INT1}}$)(1)					
45		P3_2	($\overline{\text{INT2}}$)(1)					

NOTE:
1. Can be assigned to the pin in parentheses by a program.

Table 1.8 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter
46		P1_3	$\overline{KI3}$					AN11
47		P1_2	$\overline{KI2}$					AN10
48		P1_1	$\overline{KI1}$					AN9
49		P1_0	$\overline{KI0}$					AN8
50		P0_0						AN7
51		P0_1						AN6
52		P0_2						AN5
53		P0_3						AN4
54		P0_4						AN3
55		P6_2						
56		P6_1						
57		P0_5			CLK1			AN2
58		P0_6						AN1/DA0
59	VSS/AVSS							
60		P0_7						AN0/DA1
61	VREF							
62	VCC/AVCC							
63		P3_7				SSO		
64		P3_5				SSCK	SCL	

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

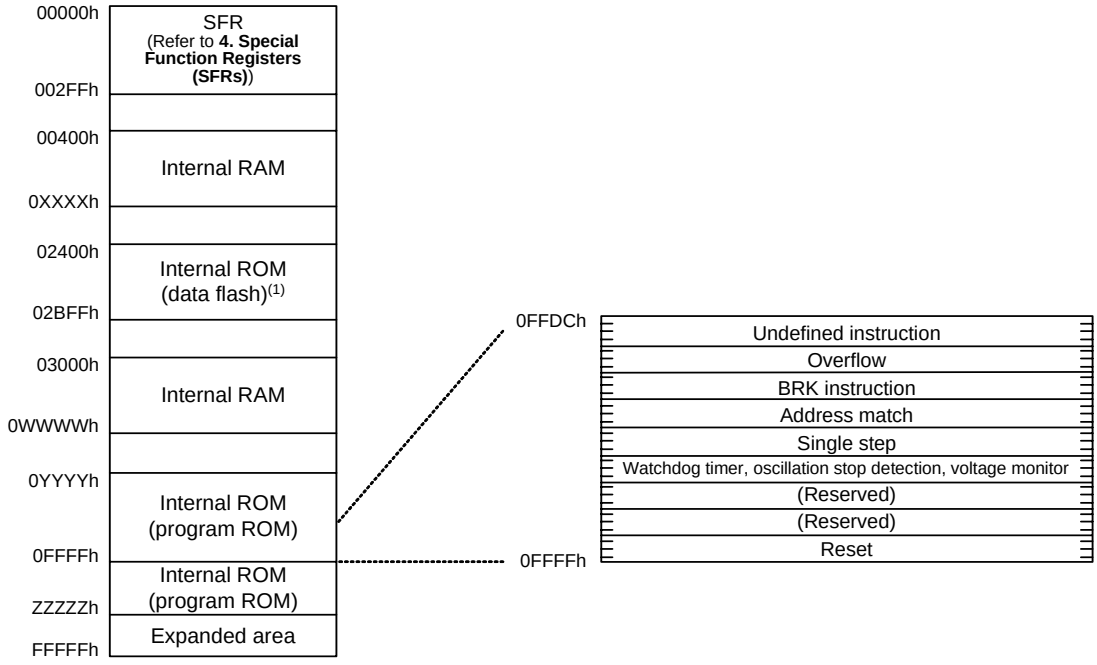
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Internal ROM			Internal RAM		
Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0WWWWh
48 Kbytes	04000h	–	2.5 Kbytes	00DFFh	–
64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	–
96 Kbytes	04000h	1BFFFh	7 Kbytes	011FFh	03DFFh
128 Kbytes	04000h	23FFFh	7.5 Kbytes	011FFh	03FFFh

Figure 3.2 Memory Map of R8C/2B Group

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)[1]

Address	Register	Symbol	After reset
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h			
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture / Compare 0 Register	TRFM0	0000h[2]
029Dh			FFFFh[3]
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
02C0h	A/D Register 0	AD0	XXh
02C1h			XXh
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h	A/D Control Register 2	ADCON2	00001000b
02D5h			
02D6h	A/D Control Register 0	ADCON0	00000011b
02D7h	A/D Control Register 1	ADCON1	00h
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h	Port P8 Direction Register	PD8	00h
02E5h			
02E6h	Port P8 Register	P8	XXh
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh	Pull-Up Control Register 2	PUR2	XXX00000b
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	00h
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

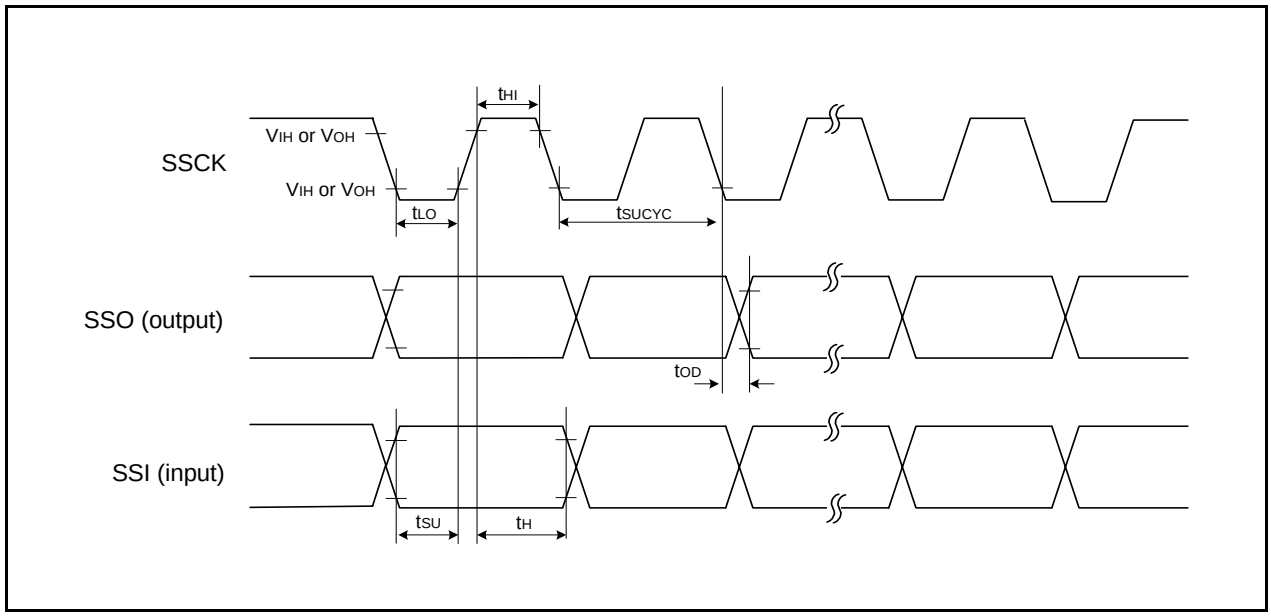


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

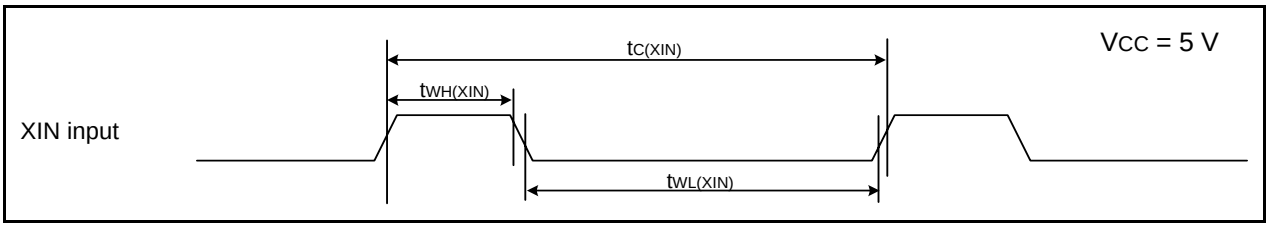


Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

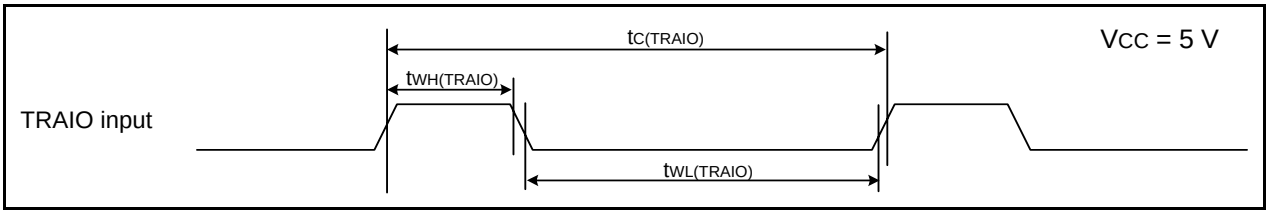


Figure 5.9 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 5 V

Table 5.20 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400(1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200(2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200(2)	–	ns

NOTES:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

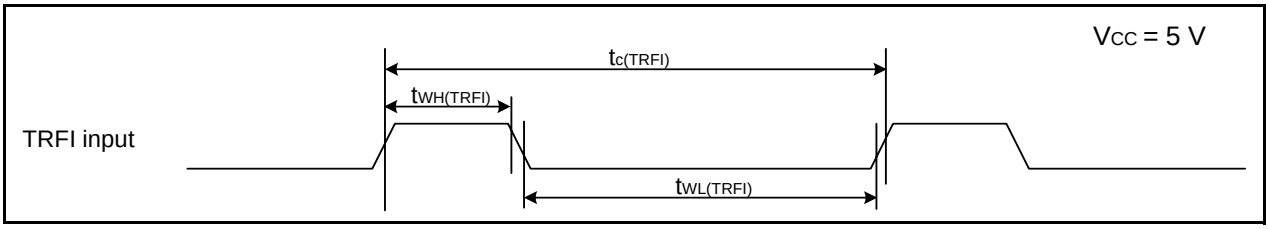


Figure 5.10 TRFI Input Timing Diagram when Vcc = 5 V

Table 5.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

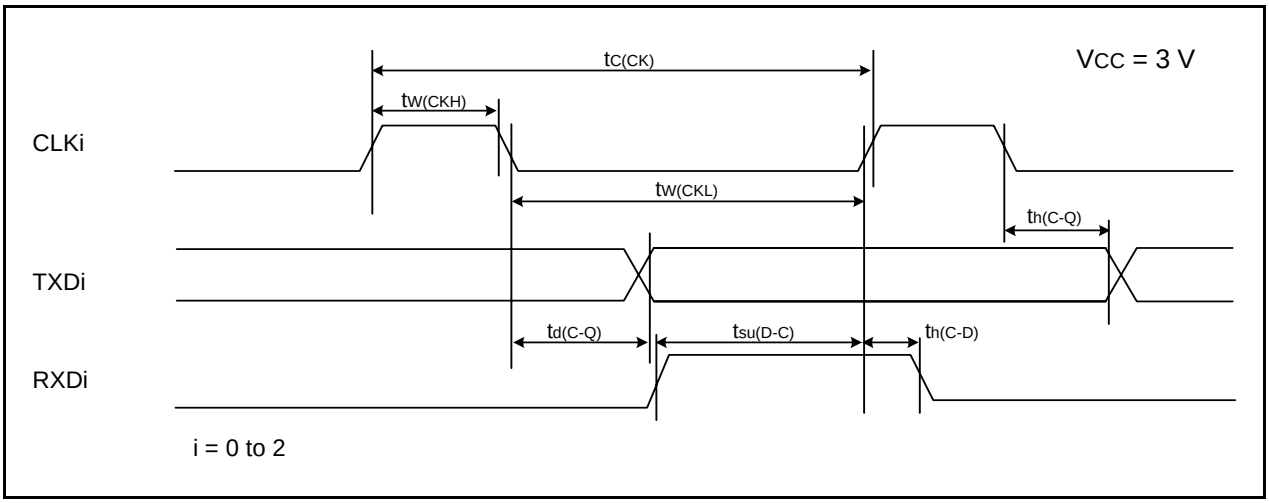


Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V

Table 5.29 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

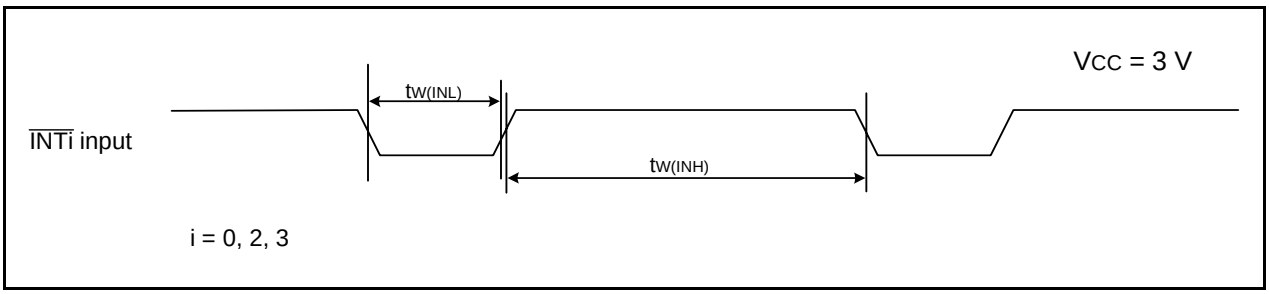


Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.30 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -2 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.32 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

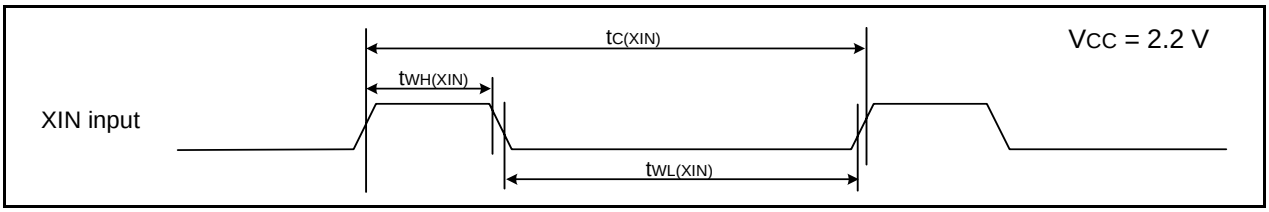


Figure 5.18 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	TBD	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	TBD	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	TBD	–	ns

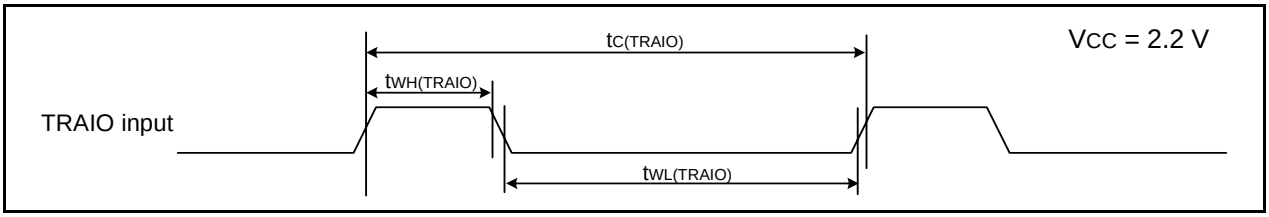


Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 2.2 V

Table 5.34 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	2000(1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	1000(2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	1000(2)	–	ns

NOTES:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

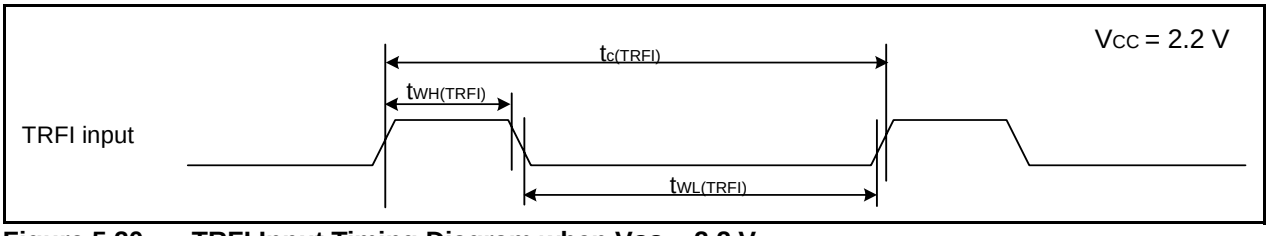
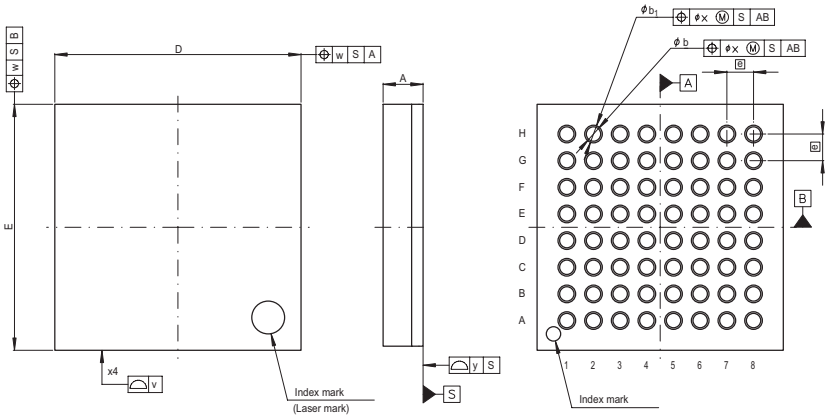


Figure 5.20 TRFI Input Timing Diagram when Vcc = 2.2 V

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.30	Dec 22, 2006	19	Table 4.1; • 000Ah: "00XXX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "00011111b" → "00X11111b" revised
		37	Table 5.11 revised
1.00	Feb 09, 2007	All pages	"Preliminary" deleted
		3	Table 1.2 revised
		5	Table 1.4 revised
		6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XXX000b" → "00h" revised • 000Fh: "00011111b" → "00X11111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added
		23	Table 4.5; 0105h: "LIN Control Register 2" register name revised
		31	Table 5.2 revised
		32	Table 5.3 and Table 5.4; NOTE1 revised
		37	Table 5.11 revised
		44	Table 5.17 revised
		46	Table 5.21 and Figure 5.11; "i = 0 to 2" revised
		48	Table 5.24 revised
		50	Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised
		52	Table 5.31 revised
		53	Table 5.34 revised
		54	Table 5.35 and Figure 5.21; "i = 0 to 2" revised
2.00	Oct 17, 2007	All pages	"PTLG0064JA-A (64F0G) package" added
		3, 5	Table 1.2 and Table 1.4; • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added
		6 to 7	Table 1.5 and Figure 1.1 revised
		8	Table 1.6 and Figure 1.2 revised
		10	Figure 1.4 "64-pin LQFP Package" added
		11	Figure 1.5 added
		19 to 20	Figure 3.1 and Figure 3.2 revised
		24	Table 4.4; 00F5h: "00h" → "000000XXb" revised