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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212acsdfa-x6

1. Overview

1.1 Features

The R8C/2A Group and R8C/2B Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2B Group has on-chip data flash (1 KB $\times$ 2 blocks).

The difference between the R8C/2A Group and R8C/2B Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

Table 1.3 Specifications for R8C/2B Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) • Multiplier: 16 bits $\times$ 16 bits $\rightarrow$ 32 bits • Multiply-accumulate instruction: 16 bits $\times$ 16 bits + 32 bits $\rightarrow$ 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to Table 1.6 Product List for R8C/2B Group .
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: - Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits $\times$ 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits $\times$ 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits $\times$ 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits $\times$ 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits $\times$ 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits $\times$ 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode

Table 1.4 Specifications for R8C/2B Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I ² C-bus)
I ² C bus ⁽¹⁾		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

Table 1.5 Product List for R8C/2A Group

Current of Nov. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F212A7SNFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version		
R5F212A7SNFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product ⁽¹⁾	
R5F212A7SNXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNXXXLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNXXXLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNXXXLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			

NOTE:

1. The user ROM is programmed before shipment.

1.4 Pin Assignment

Figure 1.4 shows 64-pin LQFP Package Pin Assignment (Top View). Figure 1.5 shows 64-pin FLGA Package Pin Assignment (Top Perspective View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.

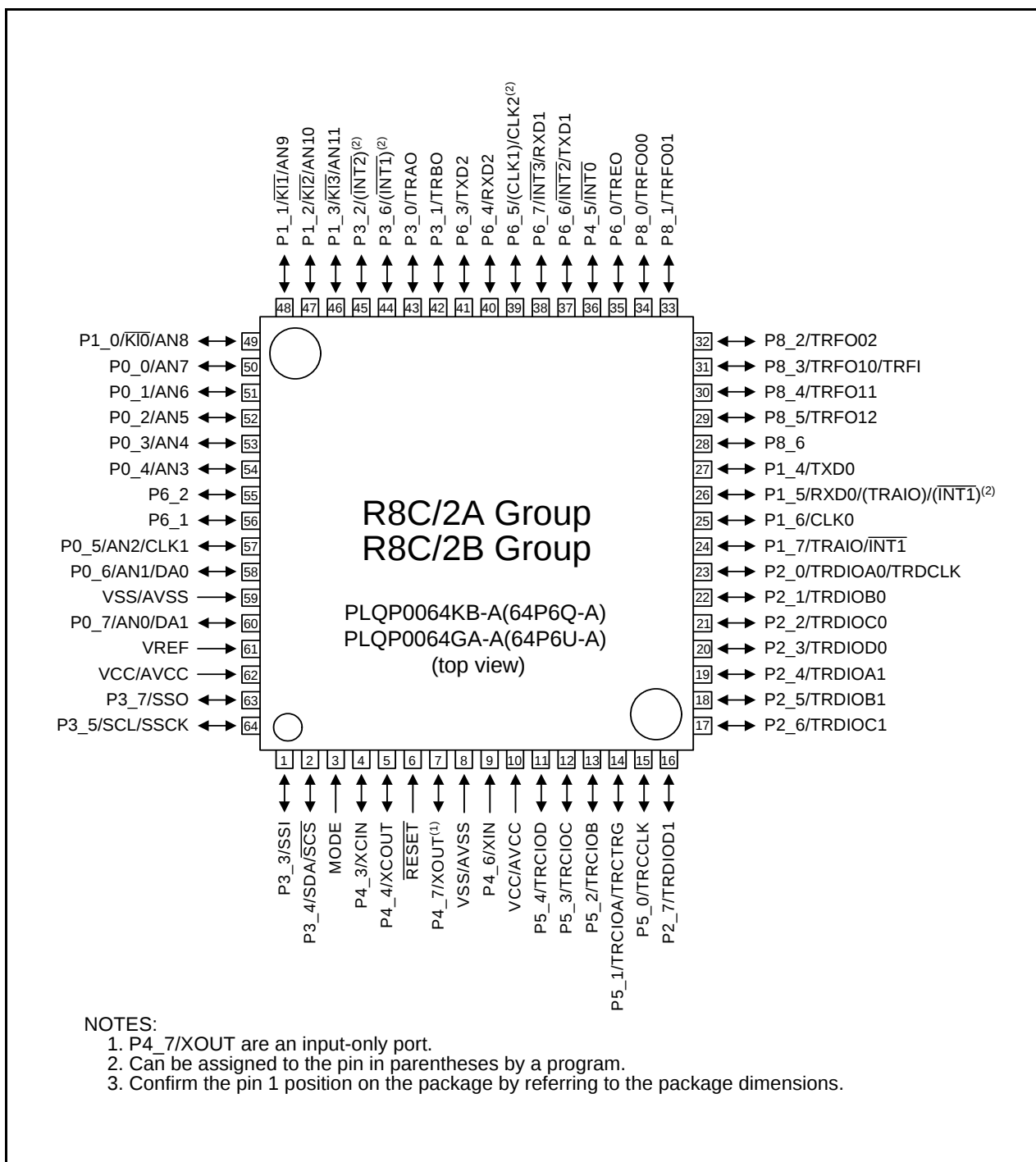


Figure 1.4 64-pin LQFP Package Pin Assignment (Top View)

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Operation Enable Register	MSTCR	00h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			00h
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁶⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	000000XXb
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX000000b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Clock Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

NOTE:

1. The blank regions are reserved. Do not access locations in these regions

Table 4.7 SFR Information (7)⁽¹⁾

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)⁽¹⁾

Address	Register	Symbol	After reset
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h			
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture / Compare 0 Register	TRFM0	0000h ⁽²⁾
029Dh			FFFFh ⁽³⁾
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 5.3 A/D Converter Characteristics⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bit
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency	Without sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	0.25	—	10	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	1	—	10	MHz
		Without sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	0.25	—	5	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	1	—	5	MHz

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics⁽¹⁾

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	1.0	%
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		4	10	20	$k\Omega$
I_{vref}	Reference power input current	(NOTE 2)	—	—	1.5	mA

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DAi register ($i = 0 \text{ or } 1$) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (V_{REF} not connected), I_{vref} flows into the D/A converters.

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 2.7 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.0	40	41.0	MHz
		V _{CC} = 2.2 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	V _{CC} = 5.0 V, T _{opr} = 25°C	–	36.864	–	MHz
		V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	550	–	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
tsa	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

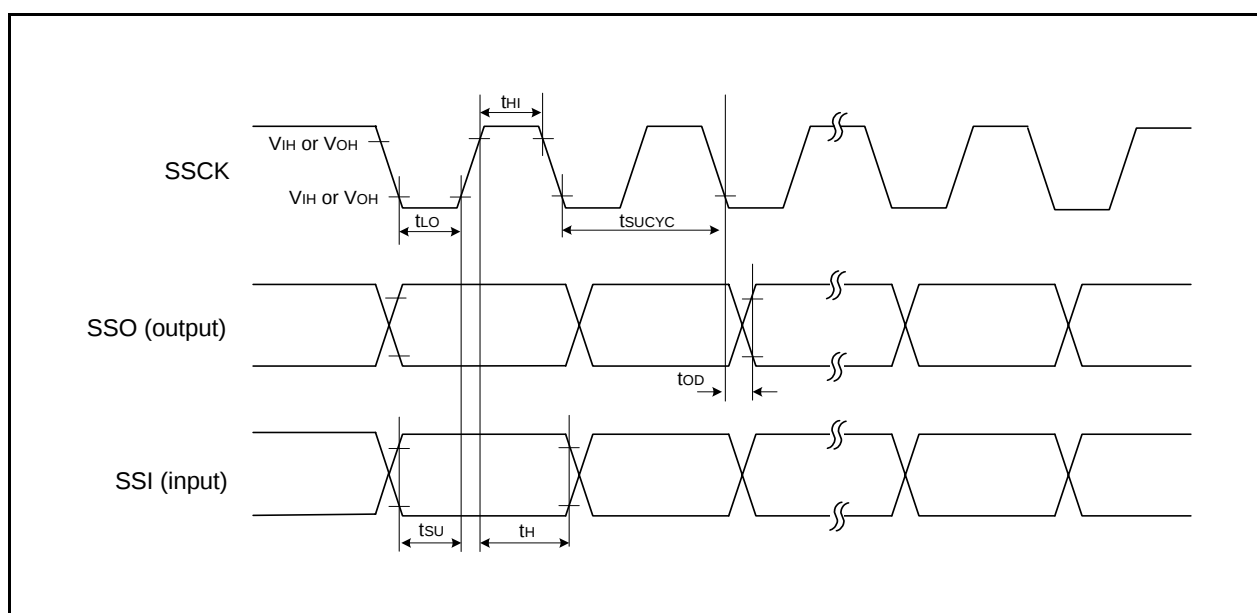


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

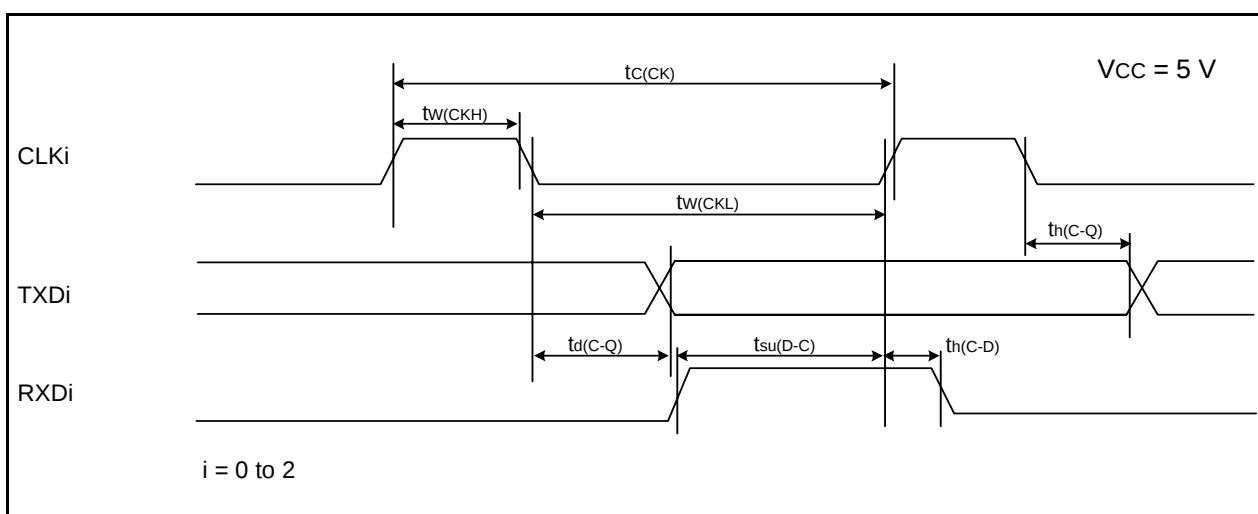
Table 5.17 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	12	20	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	10	16	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	7	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	5.5	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4.5	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	6	12	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	150	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	—	150	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	—	35	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	30	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	18	55	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	3.5	—	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	2.3	—	μA
			Stop mode	XIN clock off, T _{opr} = 25°C High-speed oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.7	3.0
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	1.7	—	μA

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

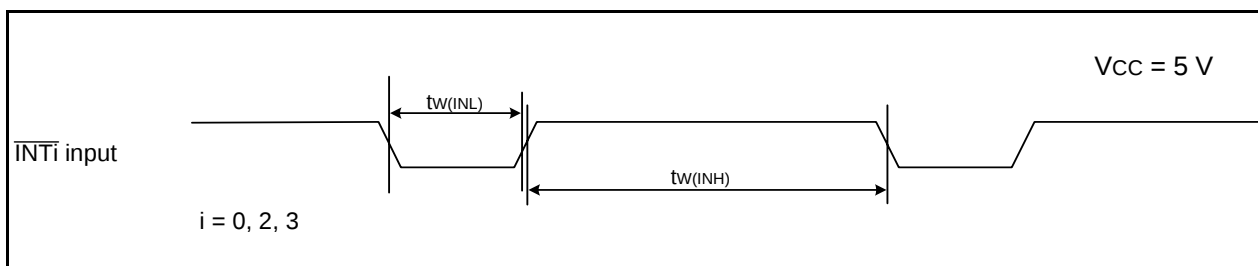
**Figure 5.12 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{IXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 03, 2006	–	First Edition issued
0.10	Jun 26, 2006	All pages	Pin name revised CMP0_0 → TRFO00, CMP0_1 → TRFO01, CMP0_2 → TRFO02, CMP1_0 → TRFO10, CMP1_1 → TRFO11, CMP1_2 → TRFO12, TRFIN → TRFI
		2, 4	Table 1.1 Specifications for R8C/2A Group (1) and Table 1.3 Specifications for R8C/2B Group (1); I/O Ports: • Input-only: 3 pins → 2 pins revised Interrupts: • Internal: 17 sources → 23 sources revised
		3, 5	Table 1.2 Specifications for R8C/2A Group (2) and Table 1.4 Specifications for R8C/2B Group (2); ROM Correction Function deleted
		8	Figure 1.3 Block Diagram revised
		9	Figure 1.4 Pin Assignment (Top View) revised
		10, 11	Table 1.7 Pin Name Information by Pin Number (1) and Table 1.8 Pin Name Information by Pin Number (2) revised
		12, 13	Table 1.9 Pin Functions (1) and Table 1.10 Pin Functions (2) revised
		19	Table 4.1 SFR Information (1); • 0008h: Module Standby Control Register, MSTCR, 00h added • 001Ch: “00h” → “00h, 10000000b” revised • NOTE6 added
		20	Table 4.2 SFR Information (2); • 005Fh: Capture Interrupt Control Register, CAPIC, XXXXX000b added
		22	Table 4.4 SFR Information (4); • 00DCh: “00DDh” → “00DCh” revised • 00F5h: “XXXX00XXb” → “00h” revised
		23	Table 4.5 SFR Information (5); • 0105h: LIN Special Function Register, LINCR2, 00h added
		30	Table 4.12 SFR Information (12); • 02C2h, 02C3h: A/D Register 1, AD1, XXh deleted • 02C4h, 02C5h: A/D Register 2, AD2, XXh deleted • 02C6h, 02C7h: A/D Register 3, AD3, XXh deleted
		31	Package Dimensions; “Diagrams showing the latest package dimensions... in the “Packages” section of the Renesas Technology website.” added
0.20	Sep 15, 2006	31 to 54	5. Electrical Characteristics added
0.30	Dec 22, 2006	6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.30	Dec 22, 2006	19	Table 4.1; • 000Ah: "00XXX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "00011111b" → "00X11111b" revised
		37	Table 5.11 revised
1.00	Feb 09, 2007	All pages	"Preliminary" deleted
		3	Table 1.2 revised
		5	Table 1.4 revised
		6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XXX000b" → "00h" revised • 000Fh: "00011111b" → "00X11111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added
		23	Table 4.5; 0105h: "LIN Control Register 2" register name revised
		31	Table 5.2 revised
		32	Table 5.3 and Table 5.4; NOTE1 revised
		37	Table 5.11 revised
		44	Table 5.17 revised
		46	Table 5.21 and Figure 5.11; "i = 0 to 2" revised
		48	Table 5.24 revised
		50	Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised
		52	Table 5.31 revised
		53	Table 5.34 revised
		54	Table 5.35 and Figure 5.21; "i = 0 to 2" revised
2.00	Oct 17, 2007	All pages	"PTLG0064JA-A (64F0G) package" added
		3, 5	Table 1.2 and Table 1.4; • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added
		6 to 7	Table 1.5 and Figure 1.1 revised
		8	Table 1.6 and Figure 1.2 revised
		10	Figure 1.4 "64-pin LQFP Package" added
		11	Figure 1.5 added
		19 to 20	Figure 3.1 and Figure 3.2 revised
		24	Table 4.4; 00F5h: "00h" → "000000XXb" revised