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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212acsdfp-v2

Table 1.2 Specifications for R8C/2A Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I ² C-bus)
I ² C bus ⁽¹⁾		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.4 Specifications for R8C/2B Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I ² C-bus)
I ² C bus ⁽¹⁾		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

Table 1.5 Product List for R8C/2A Group

Current of Nov. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F212A7SNFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version		
R5F212A7SNFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product ⁽¹⁾	
R5F212A7SNXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNXXXLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNXXXLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNXXXLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			

NOTE:

1. The user ROM is programmed before shipment.

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

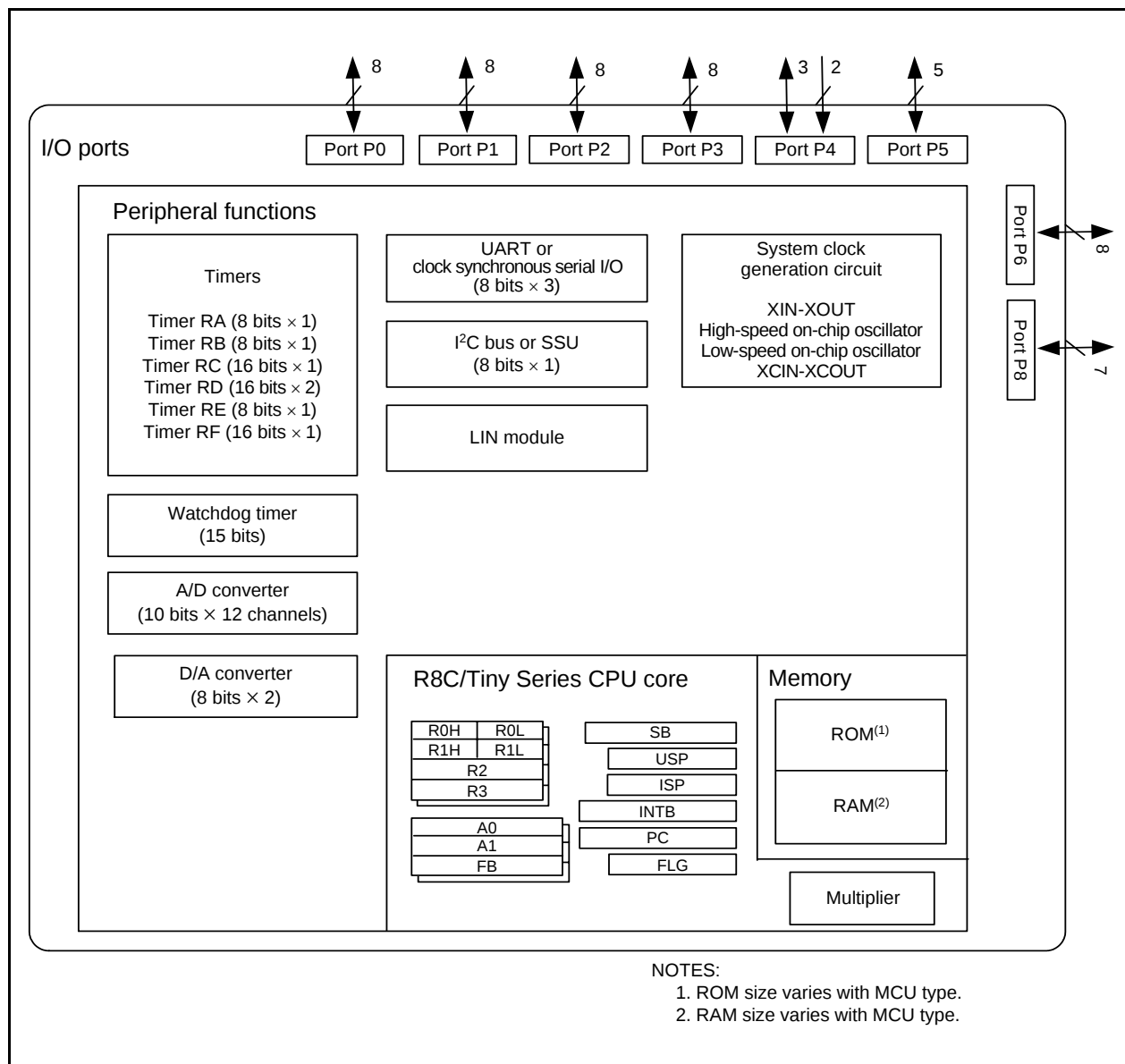


Figure 1.3 Block Diagram

Table 1.7 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter
1		P3_3				SSI		
2		P3_4				SCS	SDA	
3	MODE							
4	XCIN	P4_3						
5	XCOUT	P4_4						
6	RESET							
7	XOUT	P4_7						
8	VSS/AVSS							
9	XIN	P4_6						
10	VCC/AVCC							
11		P5_4		TRCIOD				
12		P5_3		TRCIOC				
13		P5_2		TRCIOB				
14		P5_1		TRCIOA/TRCTRG				
15		P5_0		TRCCLK				
16		P2_7		TRDIOD1				
17		P2_6		TRDIOC1				
18		P2_5		TRDIOB1				
19		P2_4		TRDIOA1				
20		P2_3		TRDIOD0				
21		P2_2		TRDIOC0				
22		P2_1		TRDIOB0				
23		P2_0		TRDIOA0/TRDCLK				
24		P1_7	INT1	TRAIO				
25		P1_6			CLK0			
26		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0			
27		P1_4			TXD0			
28		P8_6						
29		P8_5		TRFO12				
30		P8_4		TRFO11				
31		P8_3		TRFO10/TRFI				
32		P8_2		TRFO02				
33		P8_1		TRFO01				
34		P8_0		TRFO00				
35		P6_0		TREO				
36		P4_5	INT0	INT0				
37		P6_6	INT2		TXD1			
38		P6_7	INT3		RXD1			
39		P6_5			(CLK1) ⁽¹⁾ / CLK2			
40		P6_4			RXD2			
41		P6_3			TXD2			
42		P3_1		TRBO				
43		P3_0		TRA0				
44		P3_6	(INT1) ⁽¹⁾					
45		P3_2	(INT2) ⁽¹⁾					

NOTE:

1. Can be assigned to the pin in parentheses by a program.

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

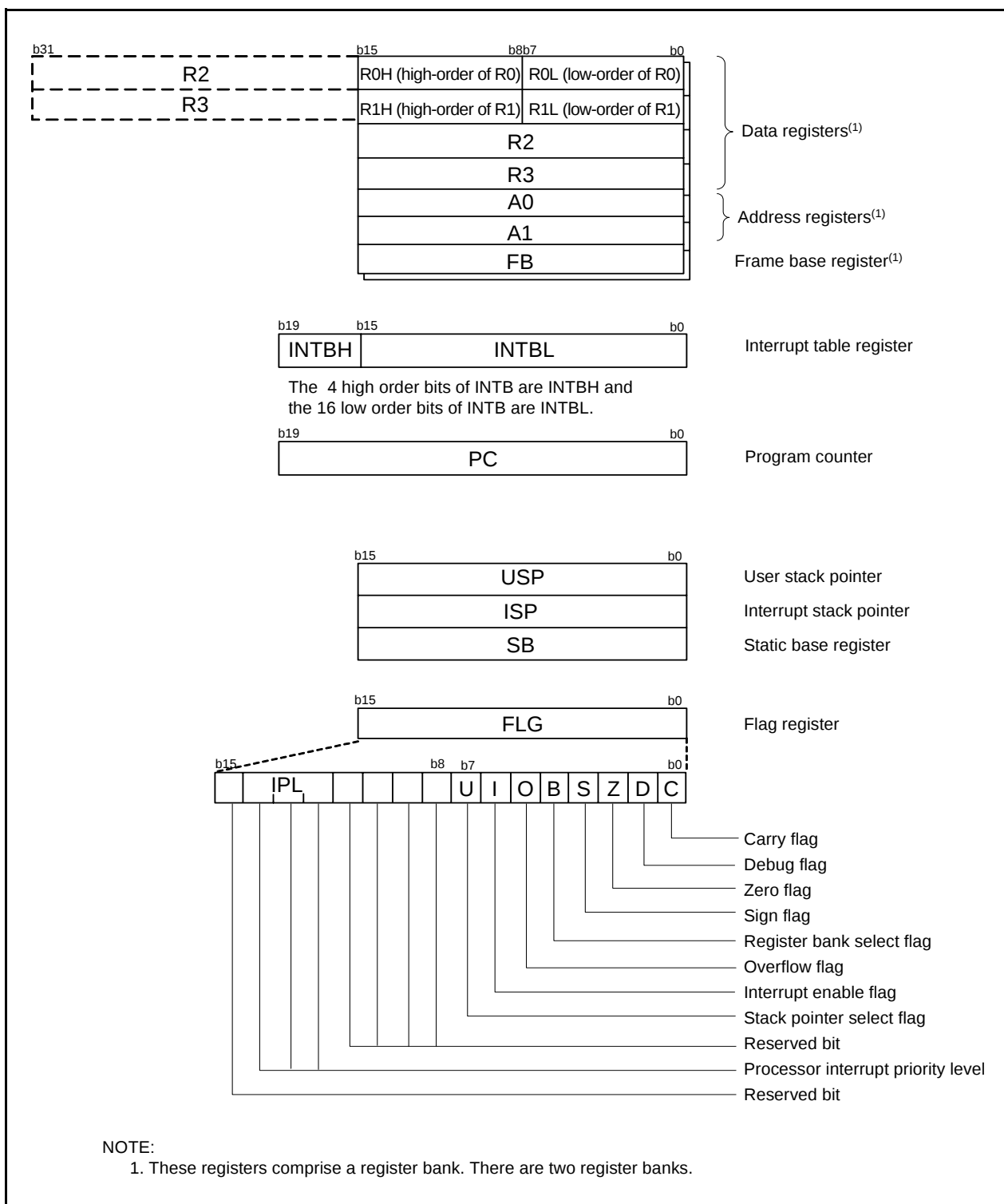


Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/2A Group

Figure 3.1 is a Memory Map of R8C/2A Group. The R8C/2A group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

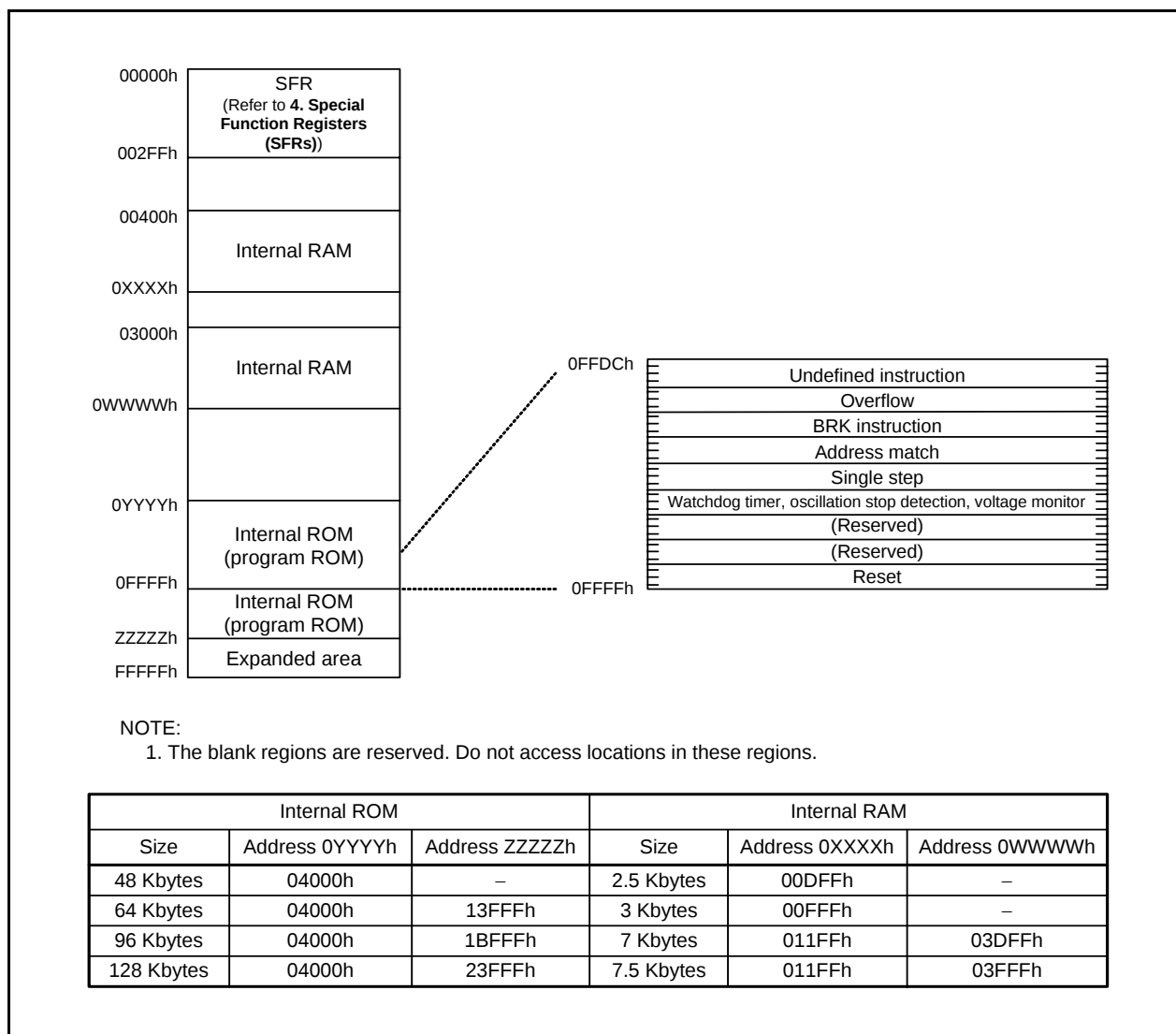


Figure 3.1 Memory Map of R8C/2A Group

3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

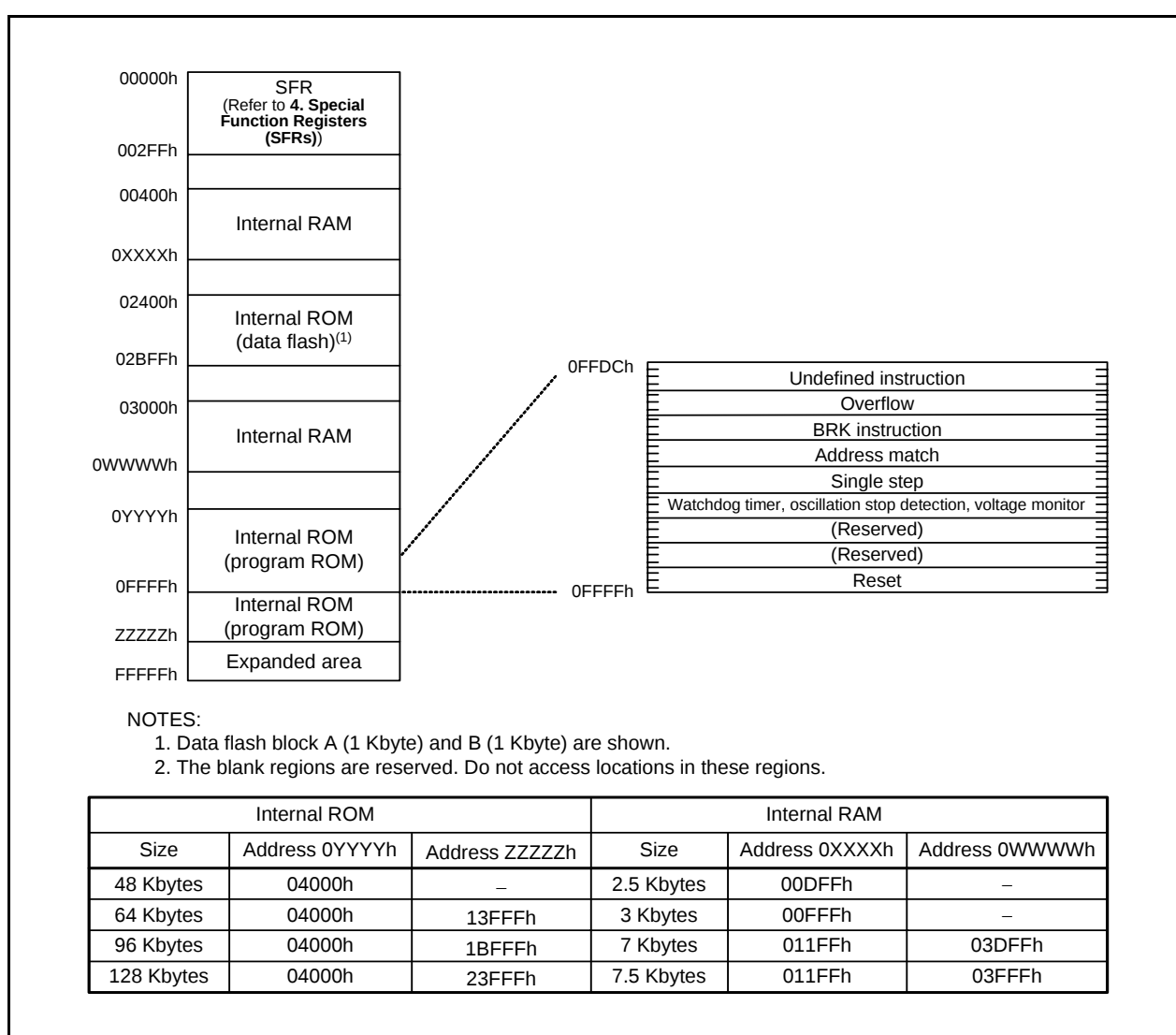


Figure 3.2 Memory Map of R8C/2B Group

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU/IIC Interrupt Control Register ⁽²⁾	SSUIC / IICIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 2.7 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.0	40	41.0	MHz
		V _{CC} = 2.2 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	V _{CC} = 5.0 V, T _{opr} = 25°C	–	36.864	–	MHz
		V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	550	–	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

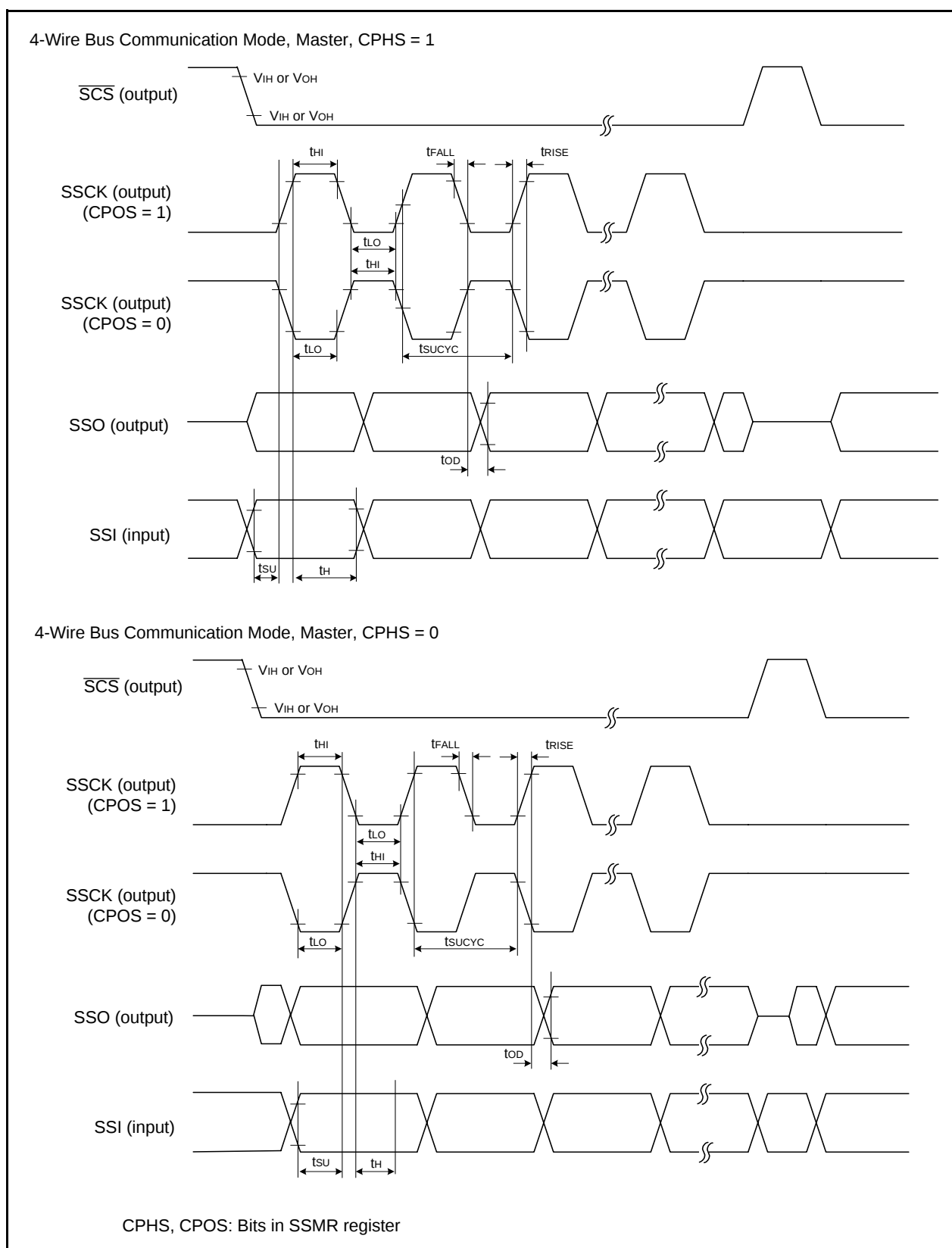


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

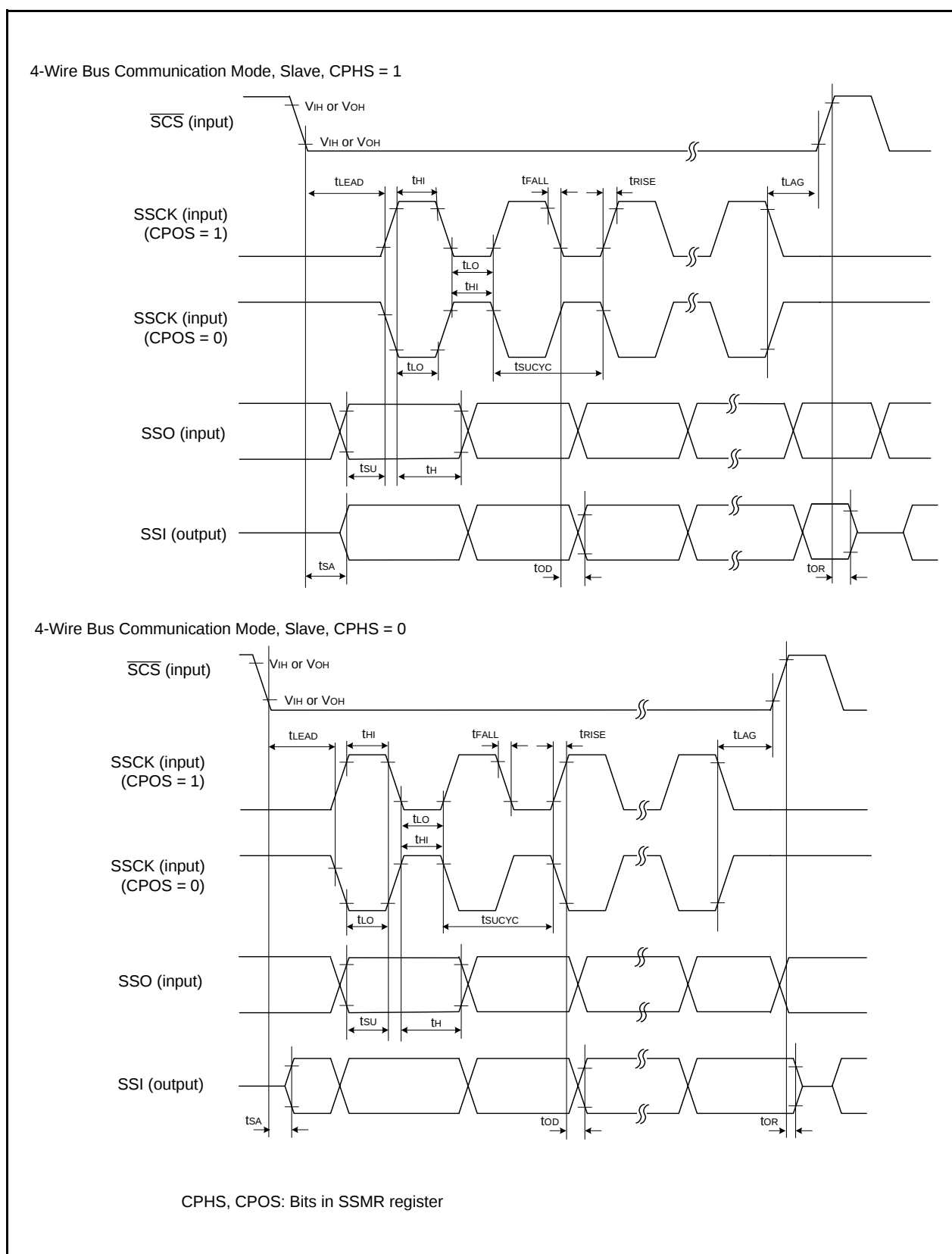
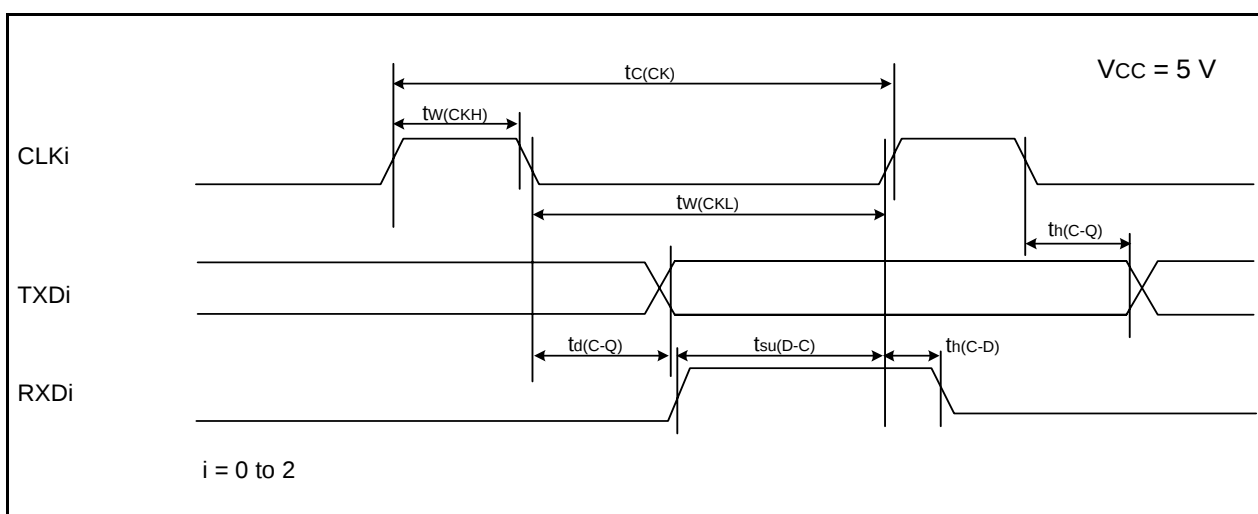


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

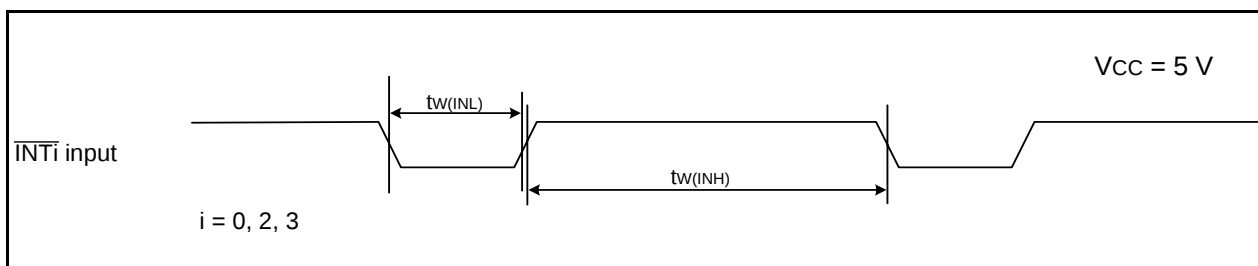
**Figure 5.12 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{IXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

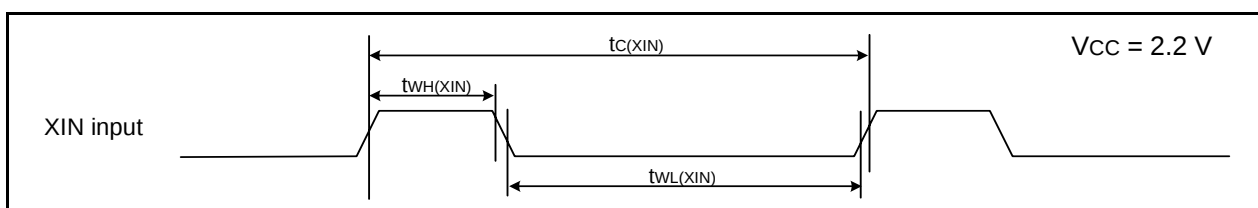
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.31 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

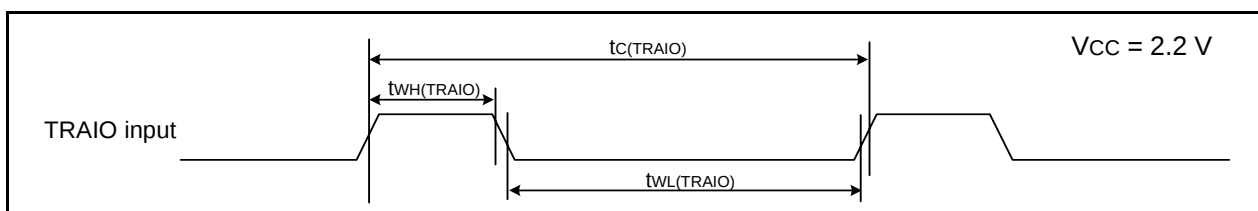
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	2.5	—	mA
				1		
		High-speed on-chip oscillator mode	—	4	—	mA
				1.7		
		Low-speed on- chip oscillator mode	—	110	300	μA
				125	350	
		Low-speed clock mode	—	27	—	μA
				20	60	
		Wait mode	—	12	40	μA
				2.8	—	
				1.9	—	
				0.6	3.0	
		Stop mode	—	1.60	—	μA
				—	—	

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.32 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.18 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(\text{TRAIO})}$	TRAIO input cycle time	TBD	–	ns
$t_{WH(\text{TRAIO})}$	TRAIO input “H” width	TBD	–	ns
$t_{WL(\text{TRAIO})}$	TRAIO input “L” width	TBD	–	ns

**Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.34 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(\text{TRFI})}$	TRFI input cycle time	2000 ⁽¹⁾	–	ns
$t_{WH(\text{TRFI})}$	TRFI input “H” width	1000 ⁽²⁾	–	ns
$t_{WL(\text{TRFI})}$	TRFI input “L” width	1000 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

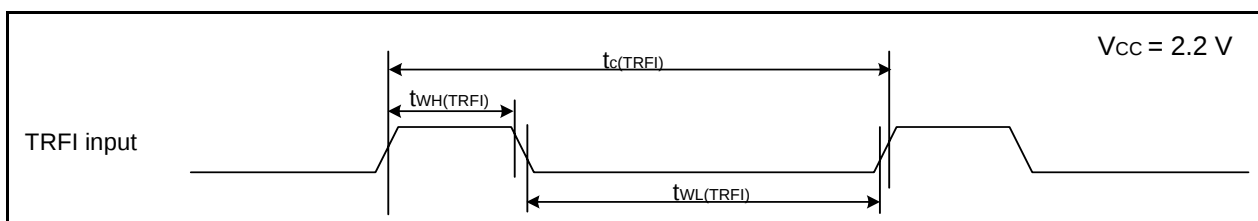
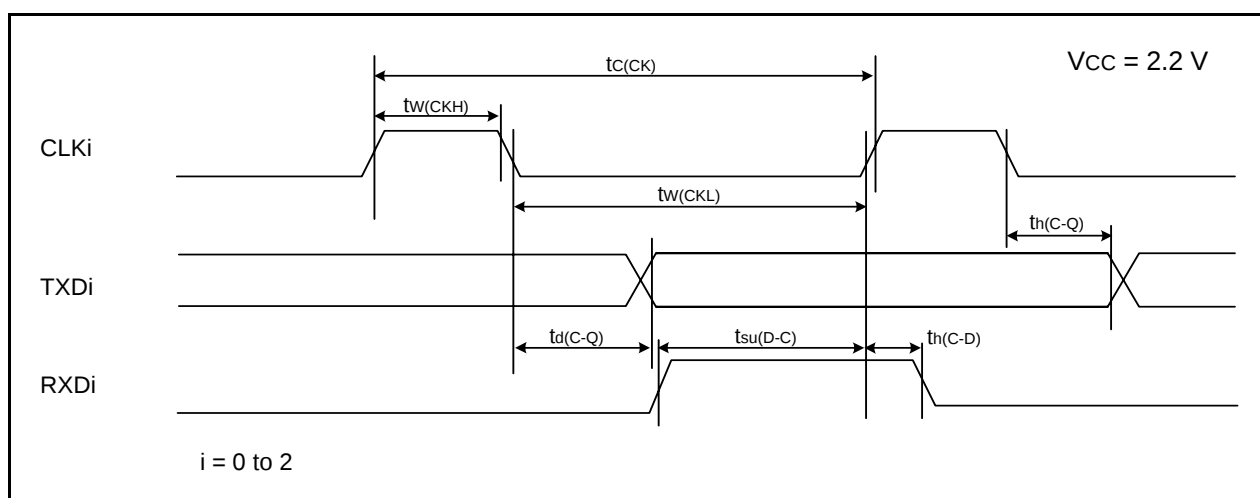
**Figure 5.20 TRFI Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.35 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

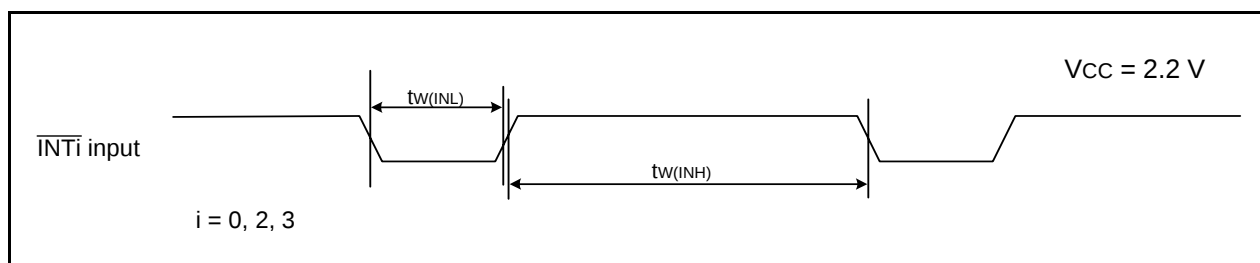
i = 0 to 2

**Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.36 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

**Figure 5.22 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

