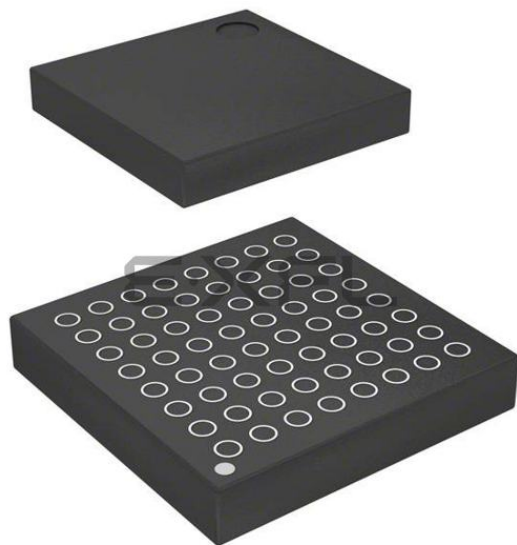




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFLGA
Supplier Device Package	64-TFLGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212acsnlg-u0

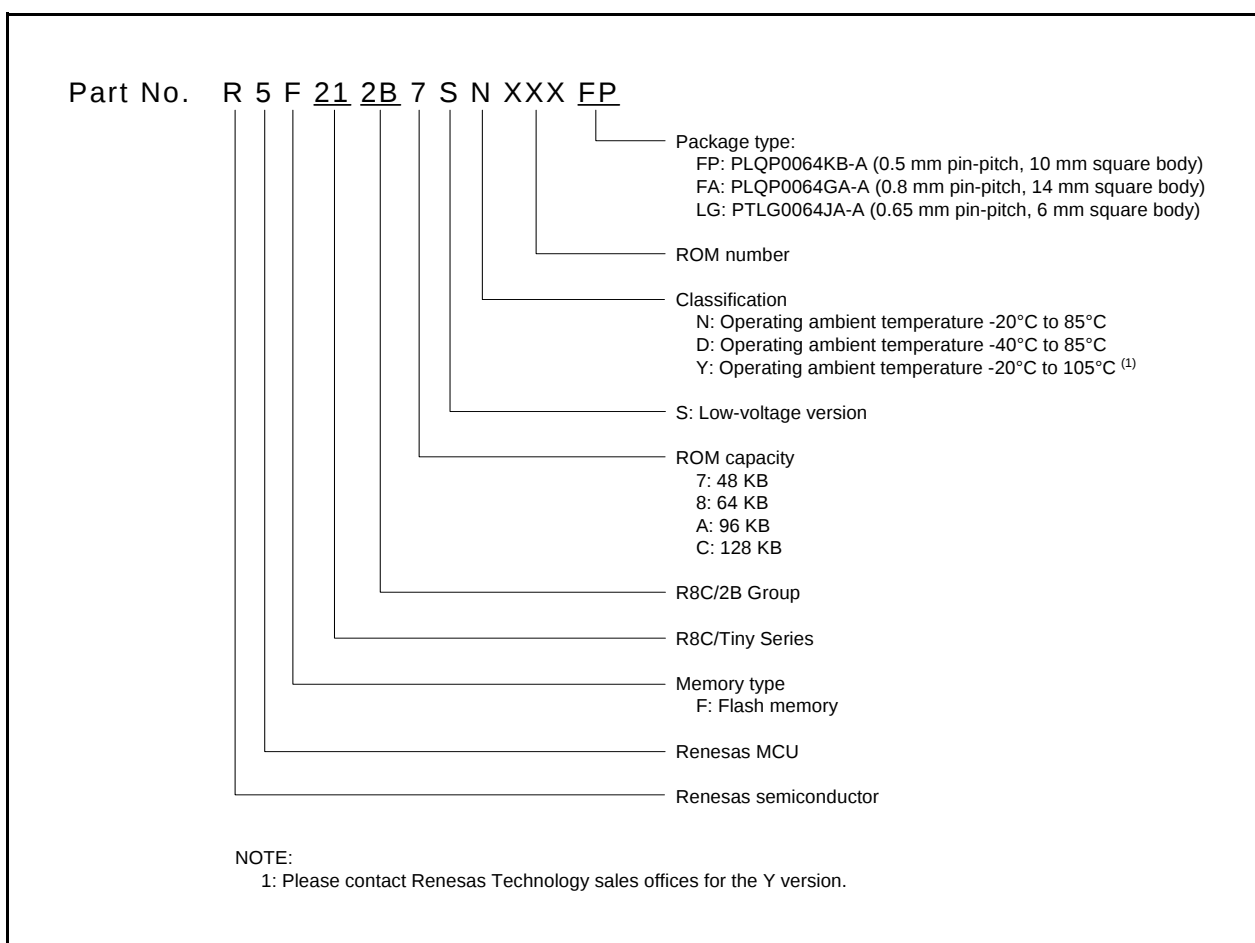


Figure 1.2 Part Number, Memory Size, and Package of R8C/2B Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

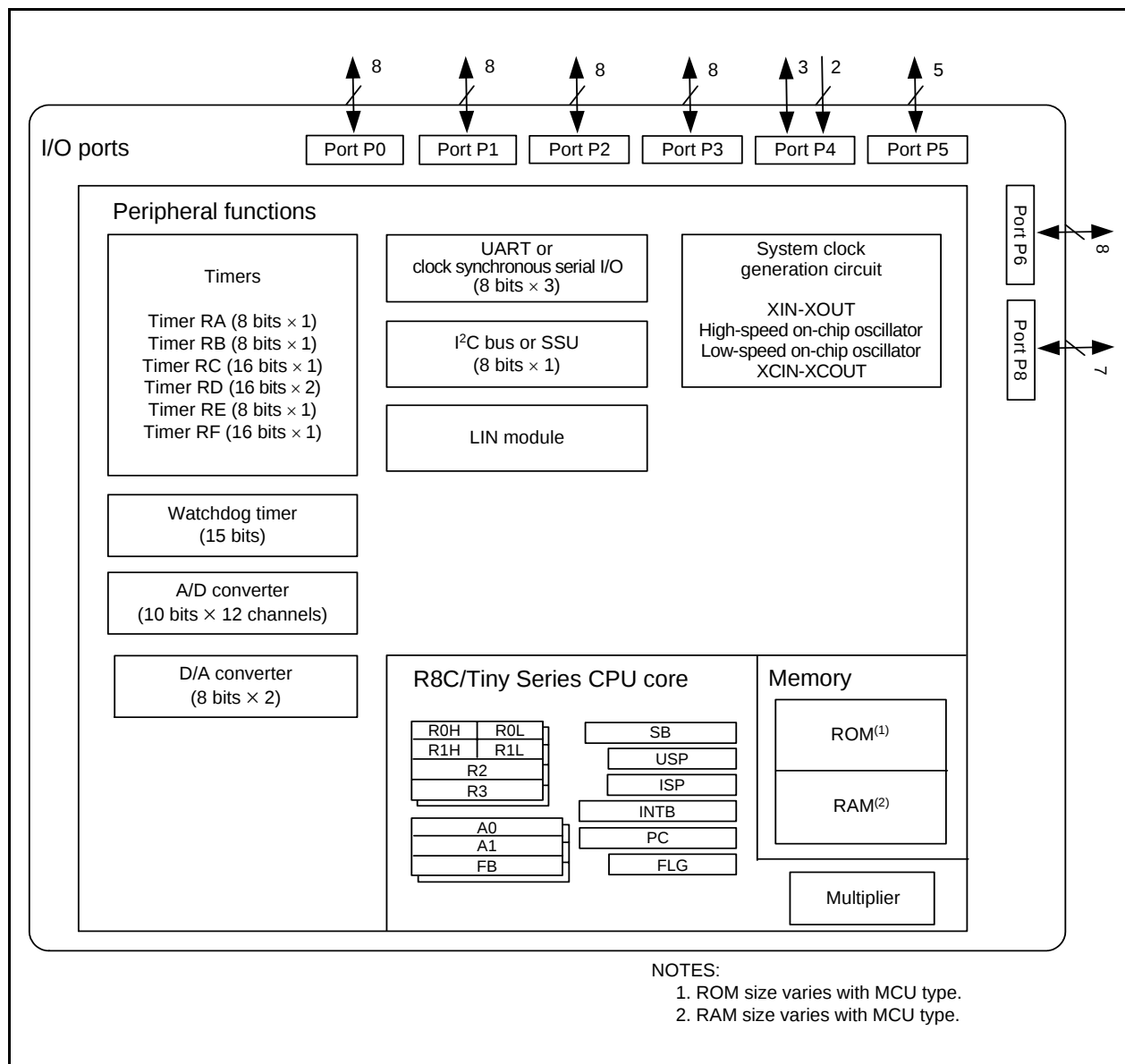


Figure 1.3 Block Diagram

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

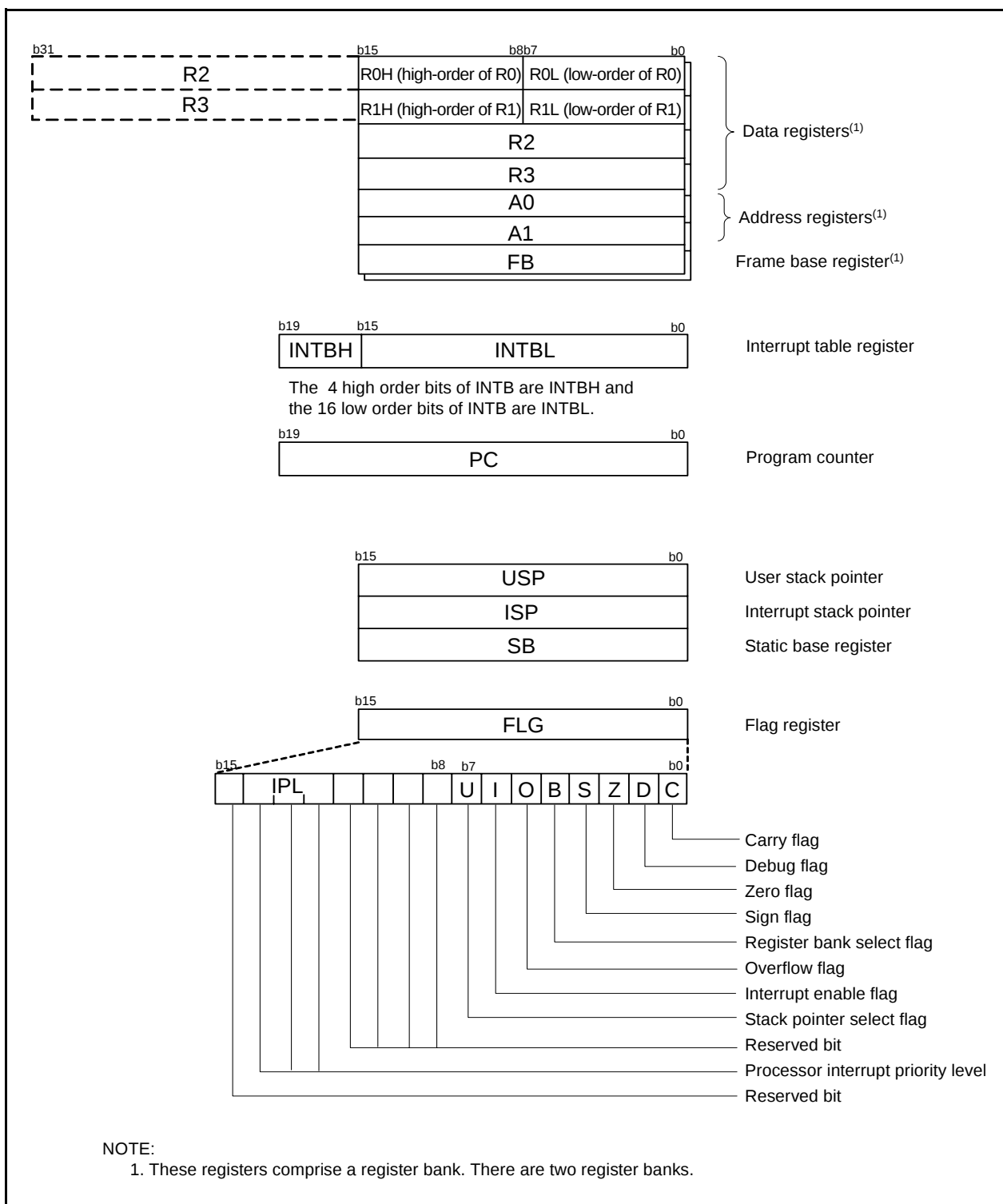


Figure 2.1 CPU Registers

3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

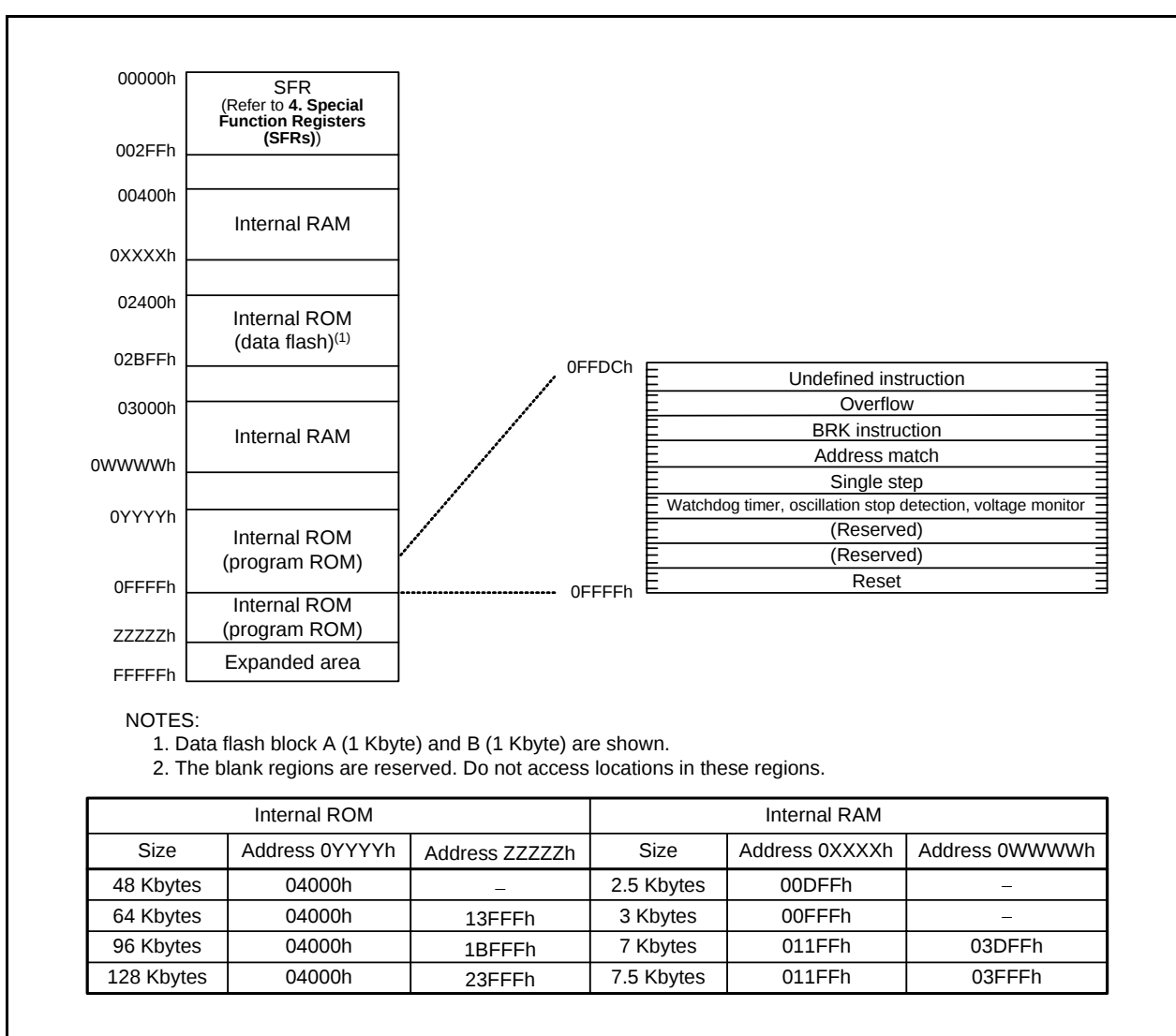


Figure 3.2 Memory Map of R8C/2B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Operation Enable Register	MSTCR	00h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X1111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			00h
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁶⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Clock Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

NOTE:

1. The blank regions are reserved. Do not access locations in these regions

Table 4.8 SFR Information (8)⁽¹⁾

Address	Register	Symbol	After reset
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)⁽¹⁾

Address	Register	Symbol	After reset
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h			
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture / Compare 0 Register	TRFM0	0000h ⁽²⁾
029Dh			FFFFh ⁽³⁾
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage			2.2	–	5.5	V
V _{SS} /AV _{SS}	Supply voltage			–	0	–	V
V _{IH}	Input “H” voltage			0.8 V _{CC}	–	V _{CC}	V
V _{IL}	Input “L” voltage			0	–	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output “H” current	Sum of all pins I _{OH} (peak)		–	–	–240	mA
I _{OH} (sum)	Average sum output “H” current	Sum of all pins I _{OH} (avg)		–	–	–120	mA
I _{OH} (peak)	Peak output “H” current	Except P2_0 to P2_7		–	–	–10	mA
		P2_0 to P2_7		–	–	–40	mA
I _{OH} (avg)	Average output “H” current	Except P2_0 to P2_7		–	–	–5	mA
		P2_0 to P2_7		–	–	–20	mA
I _{OL} (sum)	Peak sum output “L” current	Sum of all pins I _{OL} (peak)		–	–	240	mA
I _{OL} (sum)	Average sum output “L” current	Sum of all pins I _{OL} (avg)		–	–	120	mA
I _{OL} (peak)	Peak output “L” current	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
I _{OL} (avg)	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V _{CC} < 2.7 V	0	–	5	MHz
f _(XCIN)	XCIN clock input oscillation frequency		2.2 V ≤ V _{CC} ≤ 5.5 V	0	–	70	kHz
	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V _{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V _{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V _{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V _{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:

1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

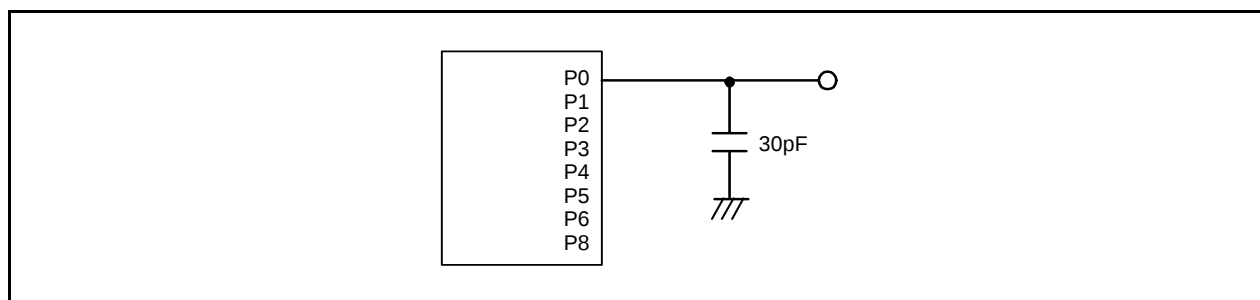
**Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit**

Table 5.3 A/D Converter Characteristics⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bit
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 5 \text{ MHz}$, $V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency	Without sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	0.25	—	10	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	1	—	10	MHz
		Without sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	0.25	—	5	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	1	—	5	MHz

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	8	Bit
—	Absolute accuracy			—	—	1.0	%
t_{su}	Setup time			—	—	3	μs
R_o	Output resistor			4	10	20	$k\Omega$
I_{vref}	Reference power input current		(NOTE 2)	—	—	1.5	mA

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DAi register ($i = 0 \text{ or } 1$) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (V_{REF} not connected), I_{vref} flows into the D/A converters.

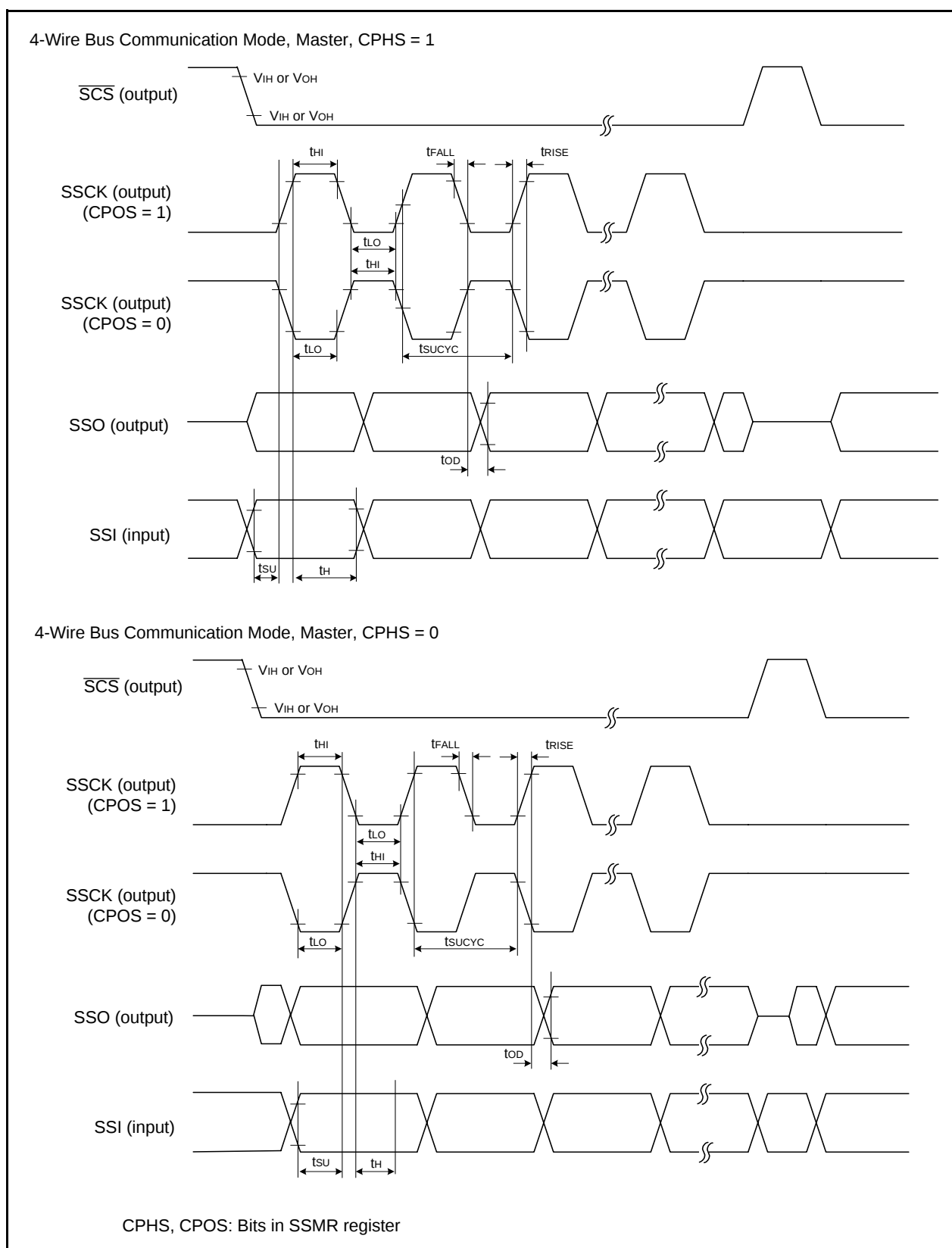


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

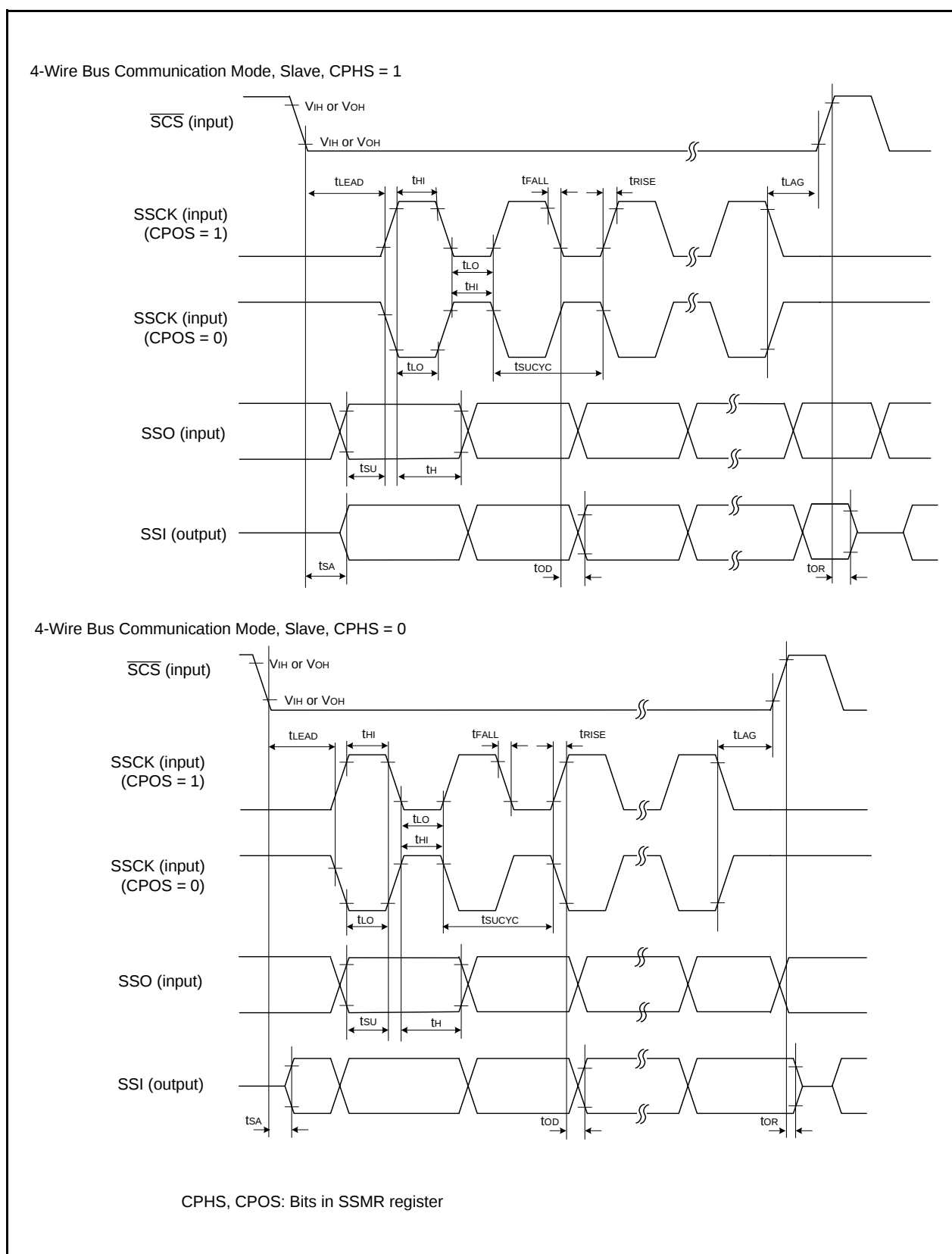


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.16 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA	V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μA	—	—	0.45	V
		P2_0 to P2_7	Drive capacity HIGH I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 5 mA	—	—	2.0	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	<u>INT0</u> , <u>INT1</u> , <u>INT2</u> , <u>INT3</u> , <u>KI0</u> , <u>KI1</u> , <u>KI2</u> , <u>KI3</u> , <u>TRAIO</u> , <u>TRFI</u> , <u>RXD0</u> , <u>RXD1</u> , <u>CLK0</u> , <u>CLK1</u> , <u>CLK2</u> , <u>SSI</u> , <u>SCL</u> , <u>SDA</u> , <u>SSO</u>		0.1	0.5	—	V
		<u>RESET</u>		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V	—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V	—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V	30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN		—	1.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN		—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

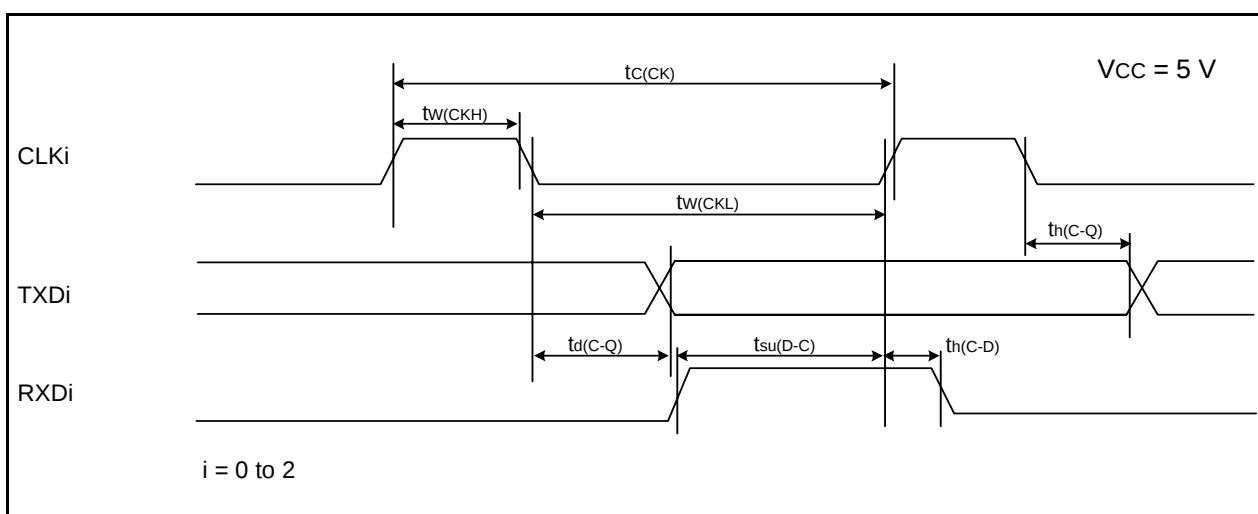
Table 5.17 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	12	20	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	10	16	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	7	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	5.5	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4.5	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	6	12	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	150	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	—	150	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	—	35	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	30	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	18	55	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	3.5	—	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	2.3	—	μA
			Stop mode	XIN clock off, T _{opr} = 25°C High-speed oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.7	3.0
		XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		—	1.7	—	μA

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

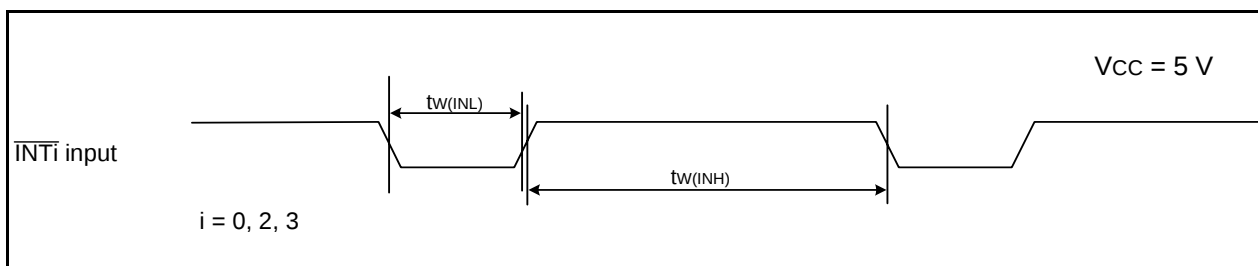
**Figure 5.12 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V**

Table 5.30 Electrical Characteristics (5) [V_{CC} = 2.2 V]

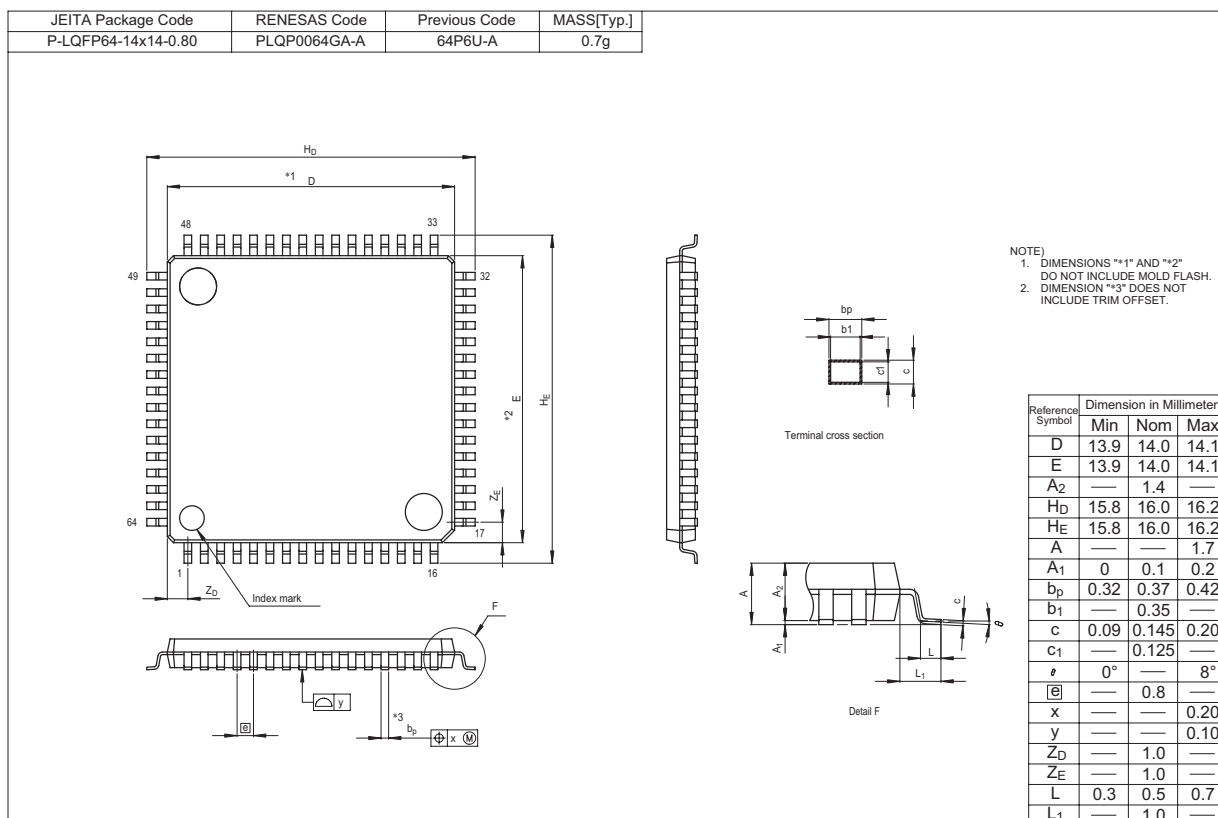
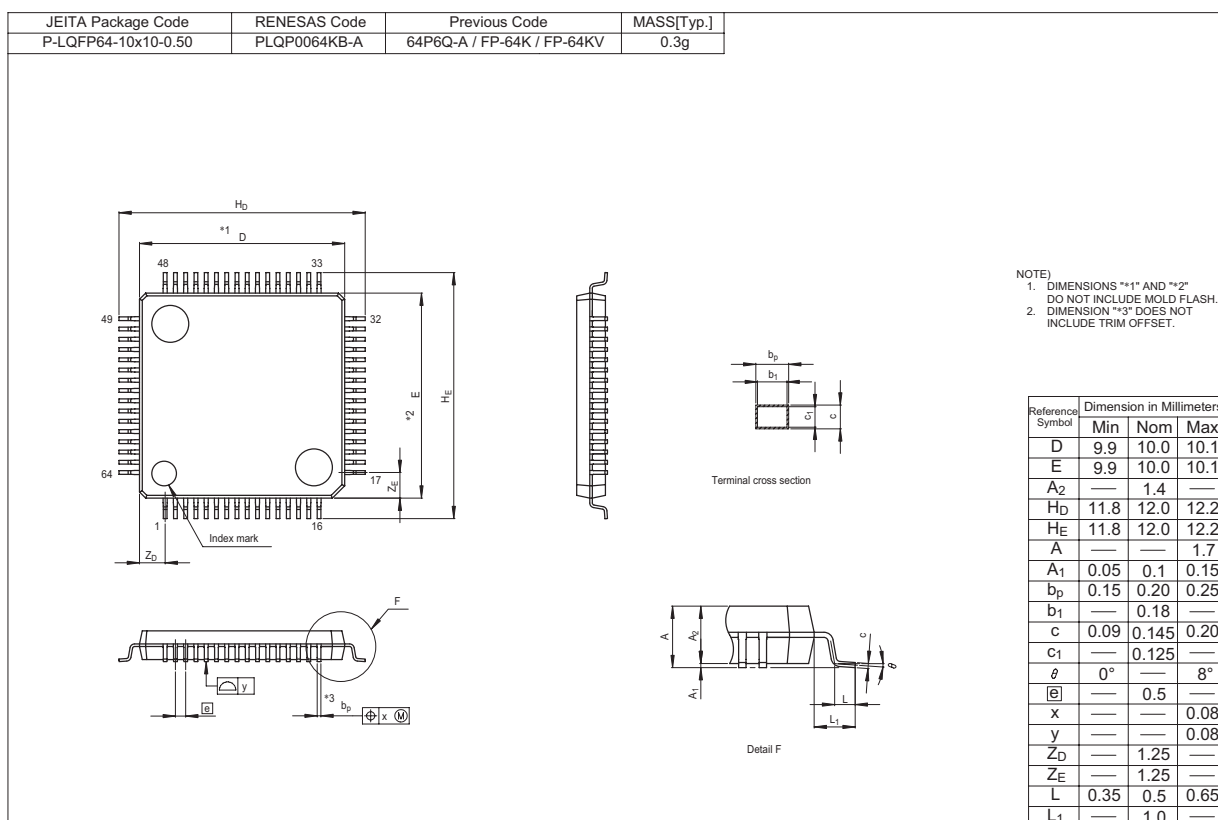
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.3	—	V
		RESET			0.05	0.15	—	V
I _{IH}	Input "H" current		V _I = 2.2 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		100	200	600	kΩ
R _{IXIN}	Feedback resistance	XIN			—	5	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	35	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.30	Dec 22, 2006	19	Table 4.1; • 000Ah: "00XXX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "00011111b" → "00X11111b" revised
		37	Table 5.11 revised
1.00	Feb 09, 2007	All pages	"Preliminary" deleted
		3	Table 1.2 revised
		5	Table 1.4 revised
		6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XXX000b" → "00h" revised • 000Fh: "00011111b" → "00X11111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added
		23	Table 4.5; 0105h: "LIN Control Register 2" register name revised
		31	Table 5.2 revised
		32	Table 5.3 and Table 5.4; NOTE1 revised
		37	Table 5.11 revised
		44	Table 5.17 revised
		46	Table 5.21 and Figure 5.11; "i = 0 to 2" revised
		48	Table 5.24 revised
		50	Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised
		52	Table 5.31 revised
		53	Table 5.34 revised
		54	Table 5.35 and Figure 5.21; "i = 0 to 2" revised
2.00	Oct 17, 2007	All pages	"PTLG0064JA-A (64F0G) package" added
		3, 5	Table 1.2 and Table 1.4; • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added
		6 to 7	Table 1.5 and Figure 1.1 revised
		8	Table 1.6 and Figure 1.2 revised
		10	Figure 1.4 "64-pin LQFP Package" added
		11	Figure 1.5 added
		19 to 20	Figure 3.1 and Figure 3.2 revised
		24	Table 4.4; 00F5h: "00h" → "000000XXb" revised