Renesas Electronics America Inc - R5F212BASNFP#V2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212basnfp-v2

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Table 1.3 Specifications for R8C/2B Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.6 Product List for R8C/2B Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2
I/O Ports	Programmable I/O ports	• Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode

Table 1.4 Specifications for R8C/2B Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I2C-bus)
I2C bus(1)		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 µA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 µA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version)(2) -20 to 105°C (Y version)(3)
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA • Package code: PTLG0064JA-A (previous code: 64F0G)

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

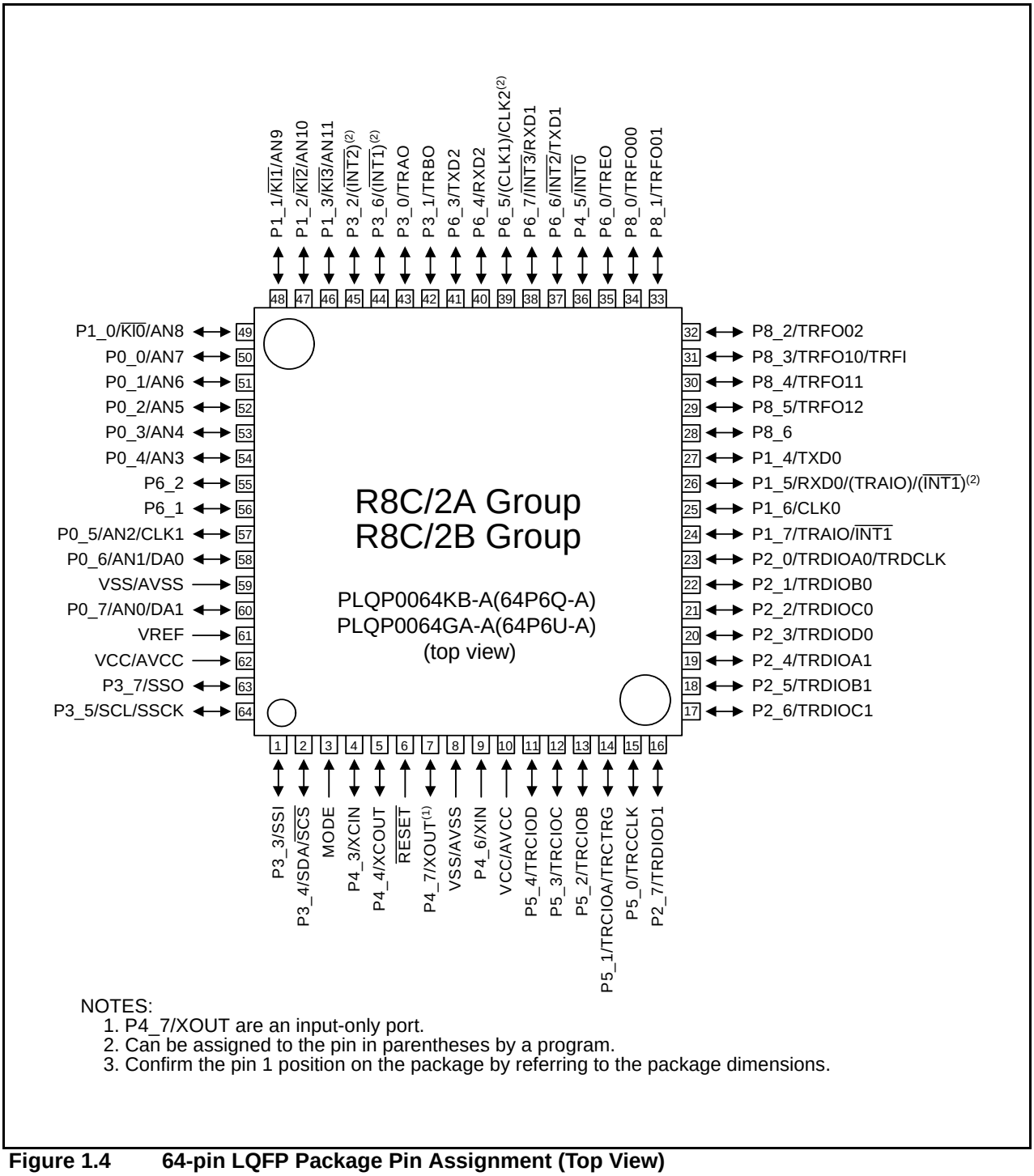
Table 1.6 Product List for R8C/2B Group **Current of Nov. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F212B7SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	N version	
R5F212B7SNFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B7SNLG	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PTLG0064JA-A		
R5F212B8SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SNFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212B8SNLG	64 Kbytes	1 Kbyte × 2	3 Kbytes	PTLG0064JA-A		
R5F212BASNFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASNFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BASNLG	96 Kbytes	1 Kbyte × 2	7 Kbytes	PTLG0064JA-A		
R5F212BCSNFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSNFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212BCSNLG	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PTLG0064JA-A		
R5F212B7SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	D version	
R5F212B7SDFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B8SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SDFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212BASDFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASDFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BCSDFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSDFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212B7SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product(1)
R5F212B7SNXXXFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B7SNXXXLG	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PTLG0064JA-A		
R5F212B8SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SNXXXFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212B8SNXXXLG	64 Kbytes	1 Kbyte × 2	3 Kbytes	PTLG0064JA-A		
R5F212BASNXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASNXXXFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BASNXXXLG	96 Kbytes	1 Kbyte × 2	7 Kbytes	PTLG0064JA-A		
R5F212BCSNXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSNXXXFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		
R5F212BCSNXXXLG	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PTLG0064JA-A		
R5F212B7SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064KB-A	D version	
R5F212B7SDXXXFA	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0064GA-A		
R5F212B8SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064KB-A		
R5F212B8SDXXXFA	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0064GA-A		
R5F212BASDXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064KB-A		
R5F212BASDXXXFA	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0064GA-A		
R5F212BCSDXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064KB-A		
R5F212BCSDXXXFA	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0064GA-A		

NOTE:
1. The user ROM is programmed before shipment.

1.4 Pin Assignment

Figure 1.4 shows 64-pin LQFP Package Pin Assignment (Top View). Figure 1.5 shows 64-pin FLGA Package Pin Assignment (Top Perspective View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.



NOTES:
1. P4_7/XOUT are an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 64-pin LQFP Package Pin Assignment (Top View)

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1(2)	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2(2)	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register(2)	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register(2)	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register(2)	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register(2)	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register(2)	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register(2)	SSRDR / ICDRR	FFh

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)[1]

Address	Register	Symbol	After reset
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h			
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture / Compare 0 Register	TRFM0	0000h[2]
029Dh			FFFFh[3]
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–240	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–120	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	-10	mA
		P2_0 to P2_7		–	–	-40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	-5	mA
		P2_0 to P2_7		–	–	-20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$		–	–	240	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$		–	–	120	mA
$I_{OL(peak)}$	Peak output “L” current	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency		2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

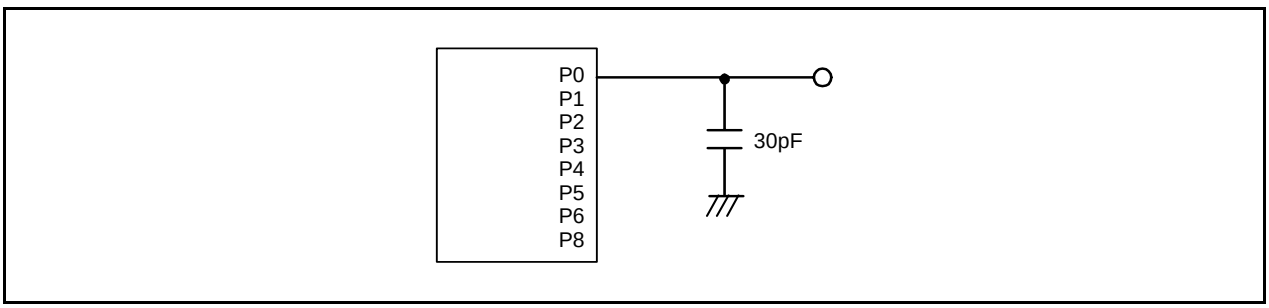


Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/2A Group	100(3)	–	–	times
		R8C/2B Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 2.7 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C(2)	39.2	40	40.8	MHz
		V_{CC} = 2.7 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C(2)	39.0	40	41.0	MHz
		V_{CC} = 2.2 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C(3)	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864	–	MHz
		V_{CC} = 2.7 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C	−3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	550	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.24 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	11	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	145	400	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	145	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	28	85	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	17	50	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.3	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.1	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.65	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.65	–	µA

Table 5.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

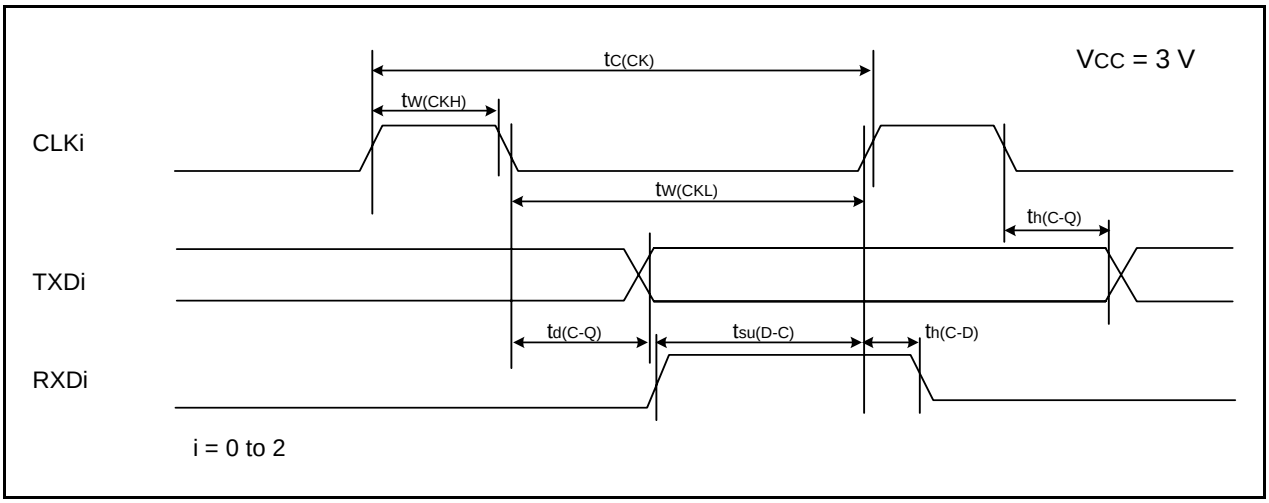


Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V

Table 5.29 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

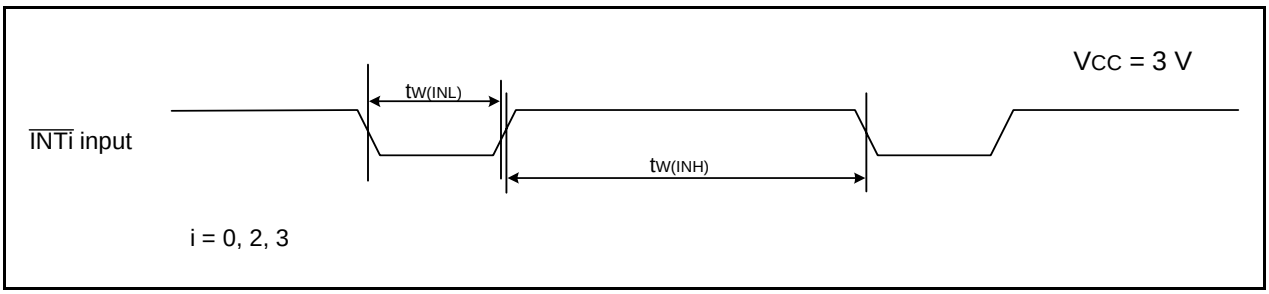


Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.35 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

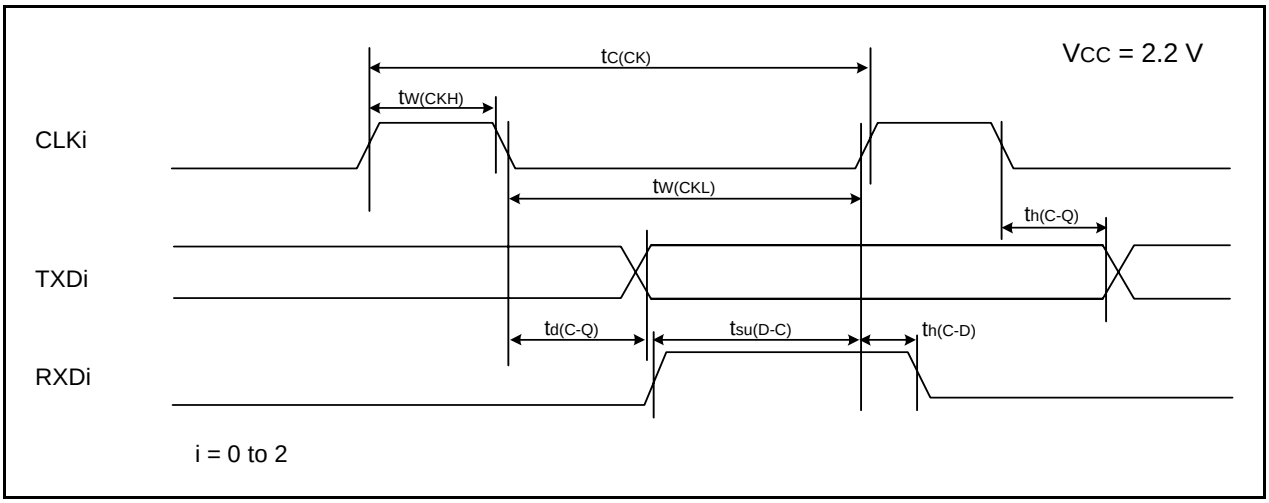


Figure 5.21 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.36 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

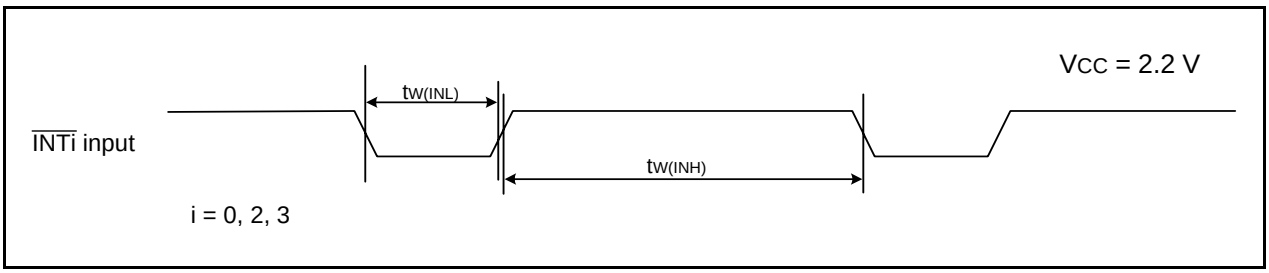
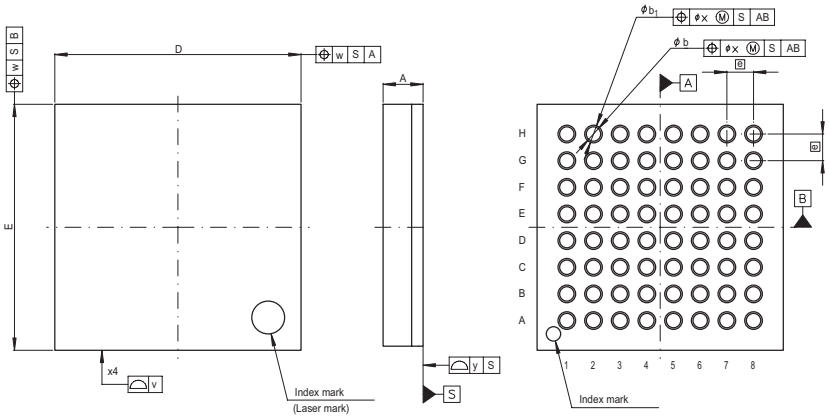


Figure 5.22 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Apr 03, 2006	–	First Edition issued
0.10	Jun 26, 2006	All pages	Pin name revised CMP0_0 → TRFO00, CMP0_1 → TRFO01, CMP0_2 → TRFO02, CMP1_0 → TRFO10, CMP1_1 → TRFO11, CMP1_2 → TRFO12, TRFIN → TRFI
		2, 4	Table 1.1 Specifications for R8C/2A Group (1) and Table 1.3 Specifications for R8C/2B Group (1); I/O Ports: • Input-only: 3 pins → 2 pins revised Interrupts: • Internal: 17 sources → 23 sources revised
		3, 5	Table 1.2 Specifications for R8C/2A Group (2) and Table 1.4 Specifications for R8C/2B Group (2); ROM Correction Function deleted
		8	Figure 1.3 Block Diagram revised
		9	Figure 1.4 Pin Assignment (Top View) revised
		10, 11	Table 1.7 Pin Name Information by Pin Number (1) and Table 1.8 Pin Name Information by Pin Number (2) revised
		12, 13	Table 1.9 Pin Functions (1) and Table 1.10 Pin Functions (2) revised
		19	Table 4.1 SFR Information (1); • 0008h: Module Standby Control Register, MSTCR, 00h added • 001Ch: “00h” → “00h, 10000000b” revised • NOTE6 added
		20	Table 4.2 SFR Information (2); • 005Fh: Capture Interrupt Control Register, CAPIC, XXXXX000b added
		22	Table 4.4 SFR Information (4); • 00DCh: “00DDh” → “00DCh” revised • 00F5h: “XXXX00XXb” → “00h” revised
		23	Table 4.5 SFR Information (5); • 0105h: LIN Special Function Register, LINCR2, 00h added
		30	Table 4.12 SFR Information (12); • 02C2h, 02C3h: A/D Register 1, AD1, XXh deleted • 02C4h, 02C5h: A/D Register 2, AD2, XXh deleted • 02C6h, 02C7h: A/D Register 3, AD3, XXh deleted
		31	Package Dimensions; “Diagrams showing the latest package dimensions... in the “Packages” section of the Renesas Technology website.” added
0.20	Sep 15, 2006	31 to 54	5. Electrical Characteristics added
0.30	Dec 22, 2006	6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Oct 17, 2007	33	Table 5.1; Pd: Rated Value “TBD” → “700” revised, “NOTE1” added
		59	Package Dimensions “PTLG0064JA-A (64F0G) package” added
2.10	Nov 26, 2007	2, 4	Table 1.1, Table 1.3 Clock: “Real-time clock (timer RE)” added
		6, 7	Table 1.5 and Figure 1.1 revised
		8, 9	Table 1.6 and Figure 1.2 revised
		20, 21	Figure 3.1 and Figure 3.2 revised
		22	Table 4.1 002Ch: High-Speed On-Chip Oscillator Control Register 7 added
		35	Table 5.2 NOTE2 revised
		41	Table 5.11 revised