



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212bcsnfp-x6

1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

Table 1.5 Product List for R8C/2A Group

Current of Nov. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F212A7SNFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version		
R5F212A7SNFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	N version	Factory programming product ⁽¹⁾	
R5F212A7SNXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A7SNXXXLG	48 Kbytes	2.5 Kbytes	PTLG0064JA-A			
R5F212A8SNXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SNXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212A8SNXXXLG	64 Kbytes	3 Kbytes	PLTG0064JA-A			
R5F212AASNXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASNXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212AASNXXXLG	96 Kbytes	7 Kbytes	PLTG0064JA-A			
R5F212ACSNXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSNXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			
R5F212ACSNXXXLG	128 Kbytes	7.5 Kbytes	PLTG0064JA-A			
R5F212A7SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0064KB-A	D version		
R5F212A7SDXXXFA	48 Kbytes	2.5 Kbytes	PLQP0064GA-A			
R5F212A8SDXXXFP	64 Kbytes	3 Kbytes	PLQP0064KB-A			
R5F212A8SDXXXFA	64 Kbytes	3 Kbytes	PLQP0064GA-A			
R5F212AASDXXXFP	96 Kbytes	7 Kbytes	PLQP0064KB-A			
R5F212AASDXXXFA	96 Kbytes	7 Kbytes	PLQP0064GA-A			
R5F212ACSDXXXFP	128 Kbytes	7.5 Kbytes	PLQP0064KB-A			
R5F212ACSDXXXFA	128 Kbytes	7.5 Kbytes	PLQP0064GA-A			

NOTE:

1. The user ROM is programmed before shipment.

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

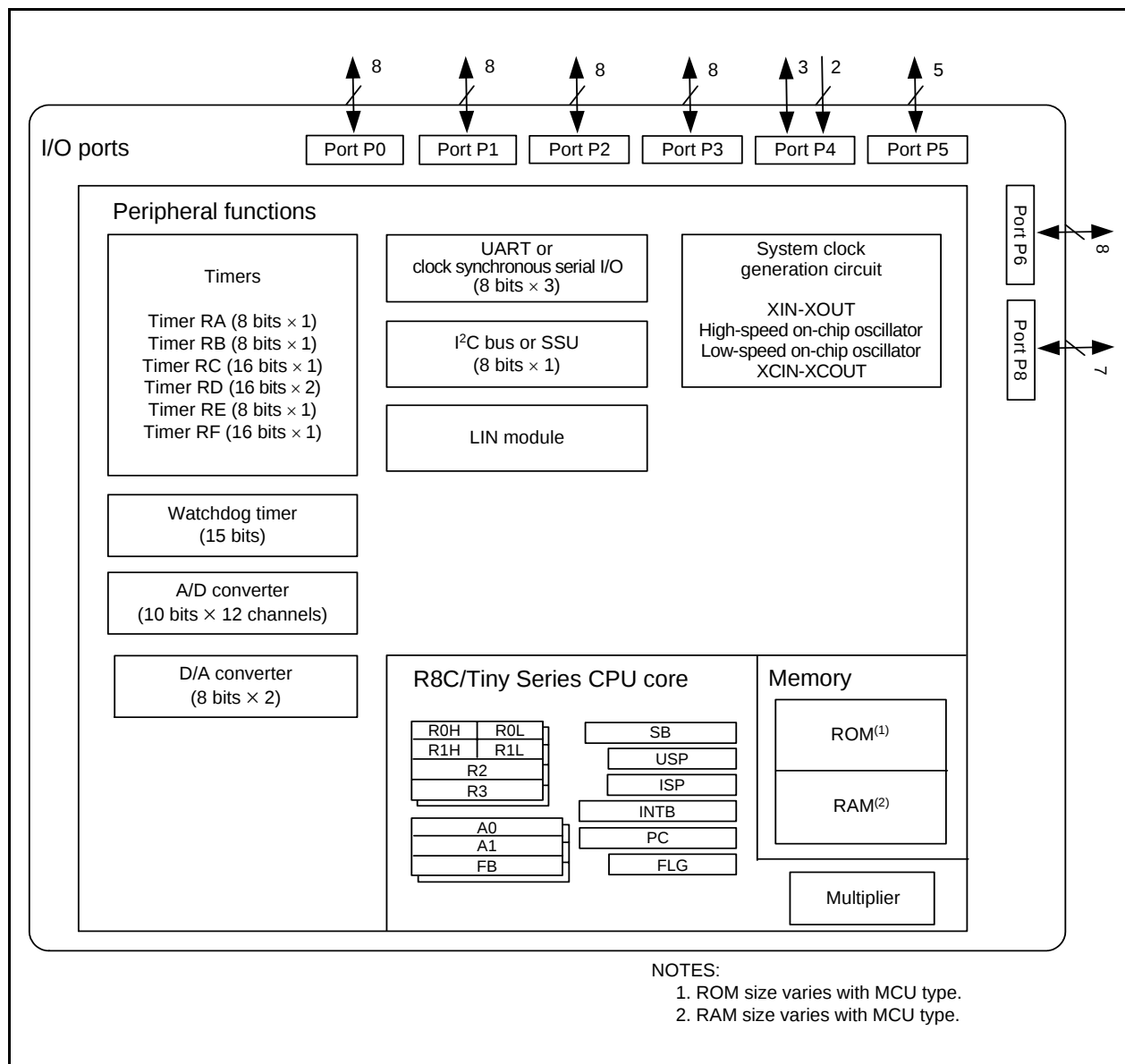


Figure 1.3 Block Diagram

1.4 Pin Assignment

Figure 1.4 shows 64-pin LQFP Package Pin Assignment (Top View). Figure 1.5 shows 64-pin FLGA Package Pin Assignment (Top Perspective View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.

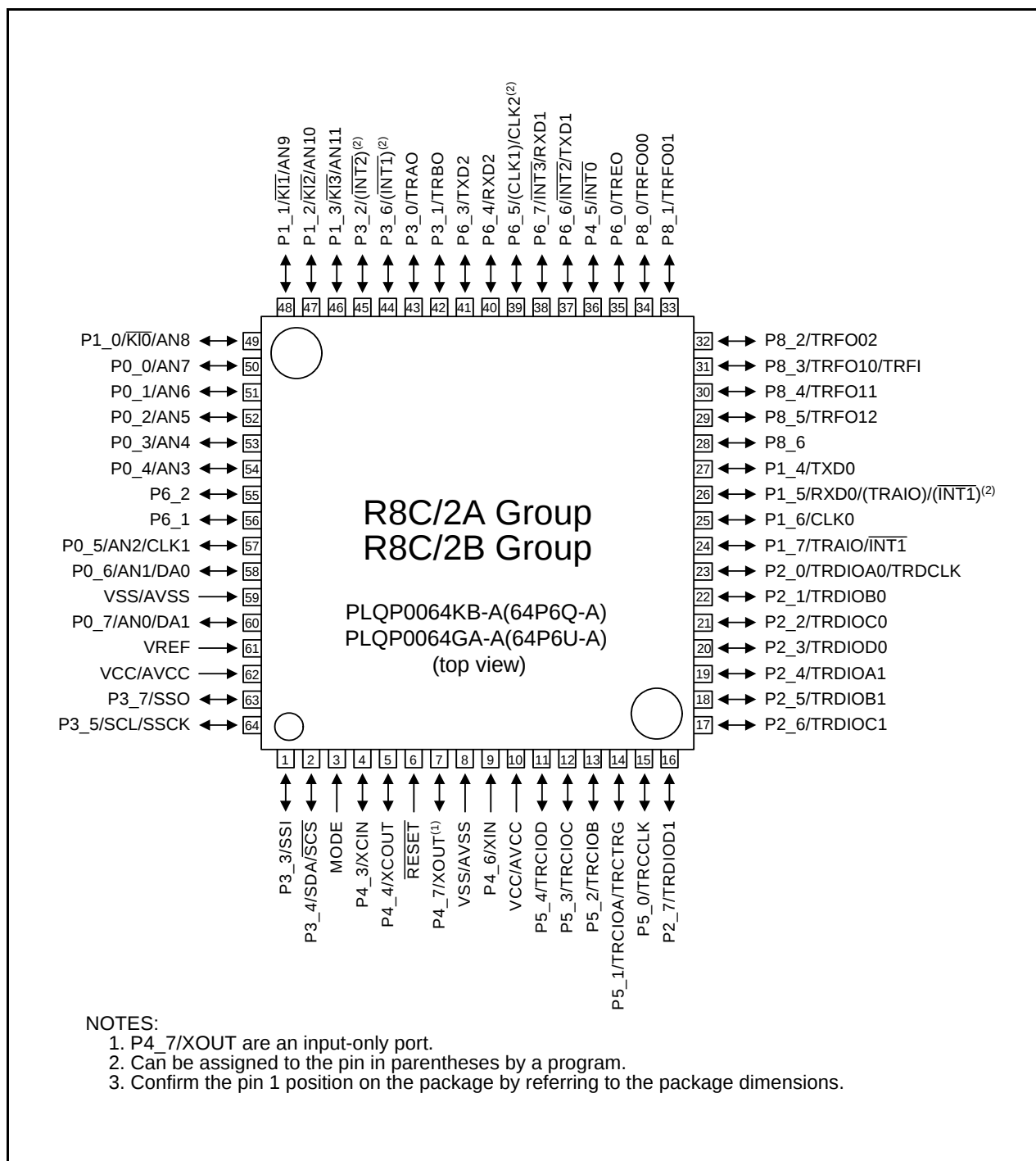


Figure 1.4 64-pin LQFP Package Pin Assignment (Top View)

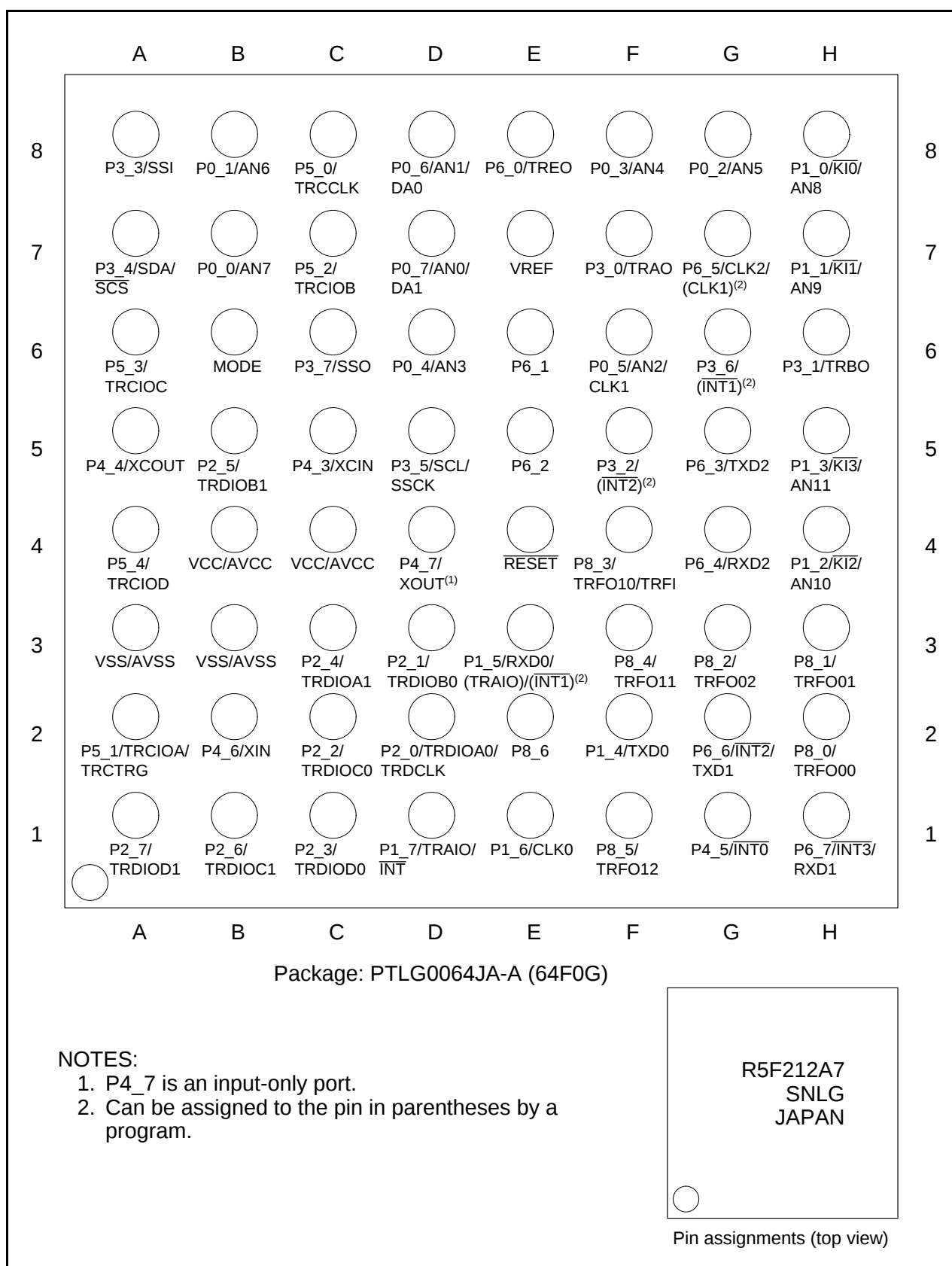


Figure 1.5 64-pin FLGA Package Pin Assignment (Top Perspective View)

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

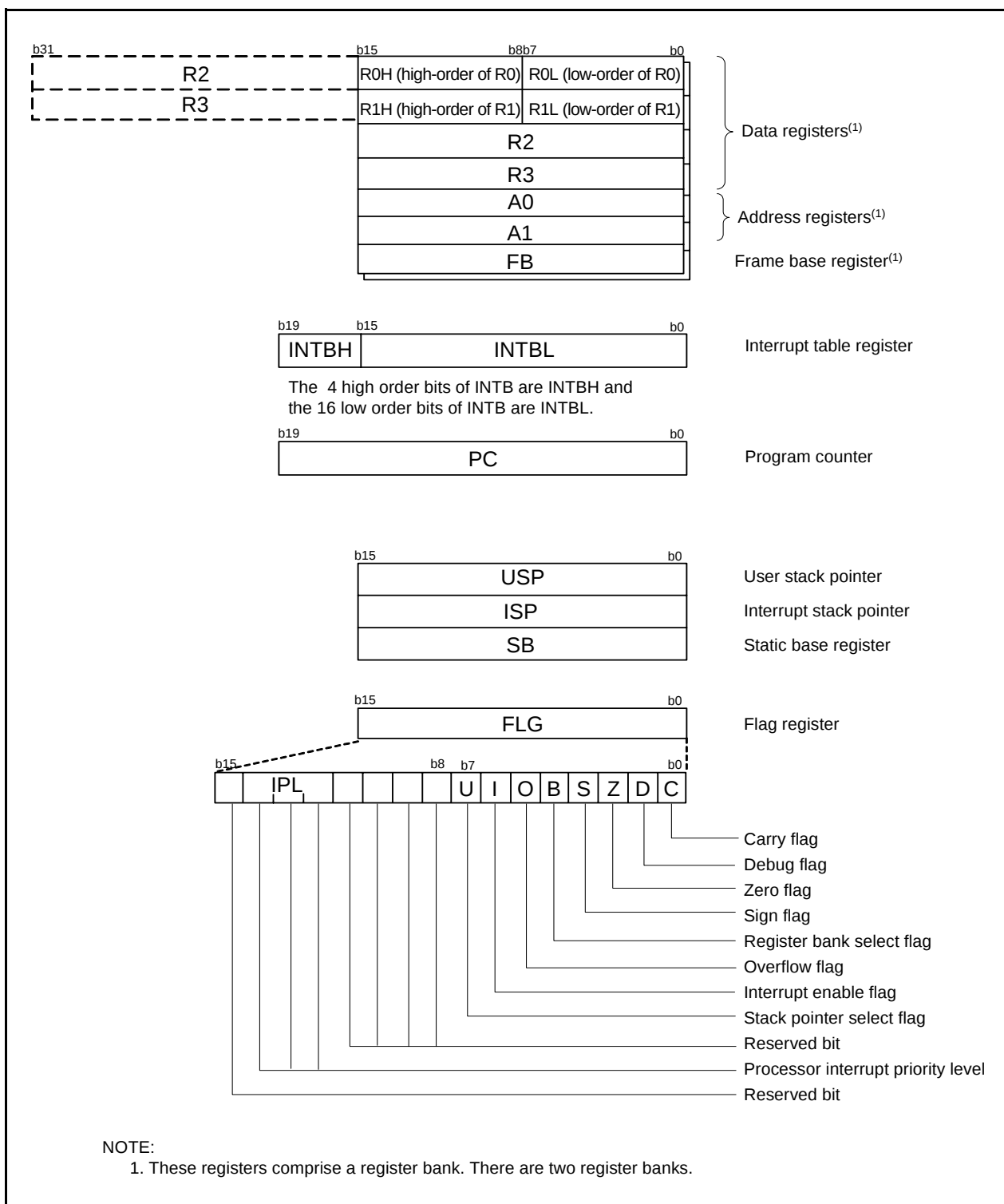


Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h	D/A Register 0	DA0	00h
00D9h			
00DAh	D/A Register 1	DA1	00h
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	000000XXb
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX000000b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11000000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART2 Transmit/Receive Mode Register	U2MR	00h
0161h	UART2 Bit Rate Register	U2BRG	XXh
0162h	UART2 Transmit Buffer Register	U2TB	XXh
0163h			XXh
0164h	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
0166h	UART2 Receive Buffer Register	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)⁽¹⁾

Address	Register	Symbol	After reset
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h			
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture / Compare 0 Register	TRFM0	0000h ⁽²⁾
029Dh			FFFFh ⁽³⁾
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 5.3 A/D Converter Characteristics⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bit
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency	Without sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	0.25	—	10	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$	1	—	10	MHz
		Without sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	0.25	—	5	MHz
		With sample and hold	$V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$	1	—	5	MHz

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	8	Bit
—	Absolute accuracy			—	—	1.0	%
t_{su}	Setup time			—	—	3	μs
R_o	Output resistor			4	10	20	$k\Omega$
I_{vref}	Reference power input current		(NOTE 2)	—	—	1.5	mA

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DAi register ($i = 0 \text{ or } 1$) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (V_{REF} not connected), I_{vref} flows into the D/A converters.

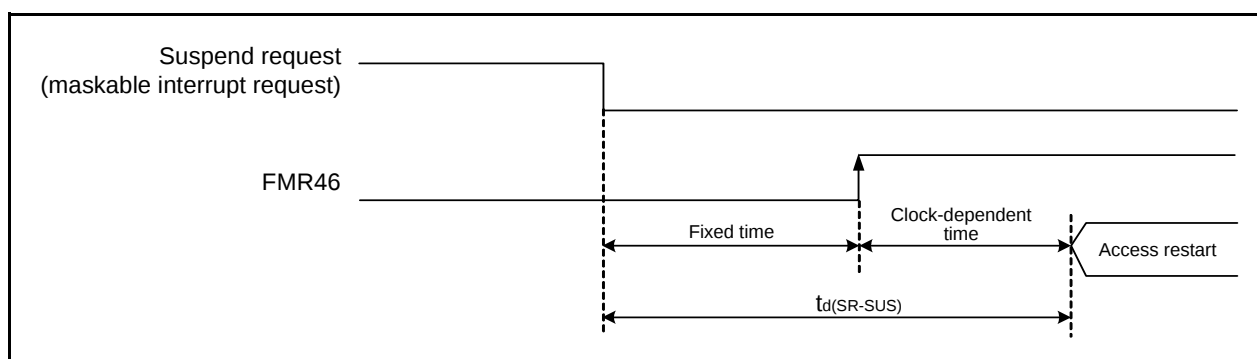


Figure 5.2 Time delay until Suspend

Table 5.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	0.9	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	300	μs
Vccmin	MCU operating voltage minimum value		2.2	—	—	V

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 2.7 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾	39.0	40	41.0	MHz
		V _{CC} = 2.2 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾	35.2	40	44.8	MHz
		V _{CC} = 2.2 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	V _{CC} = 5.0 V, T _{opr} = 25°C	–	36.864	–	MHz
		V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	550	–	μA

NOTES:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	10	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

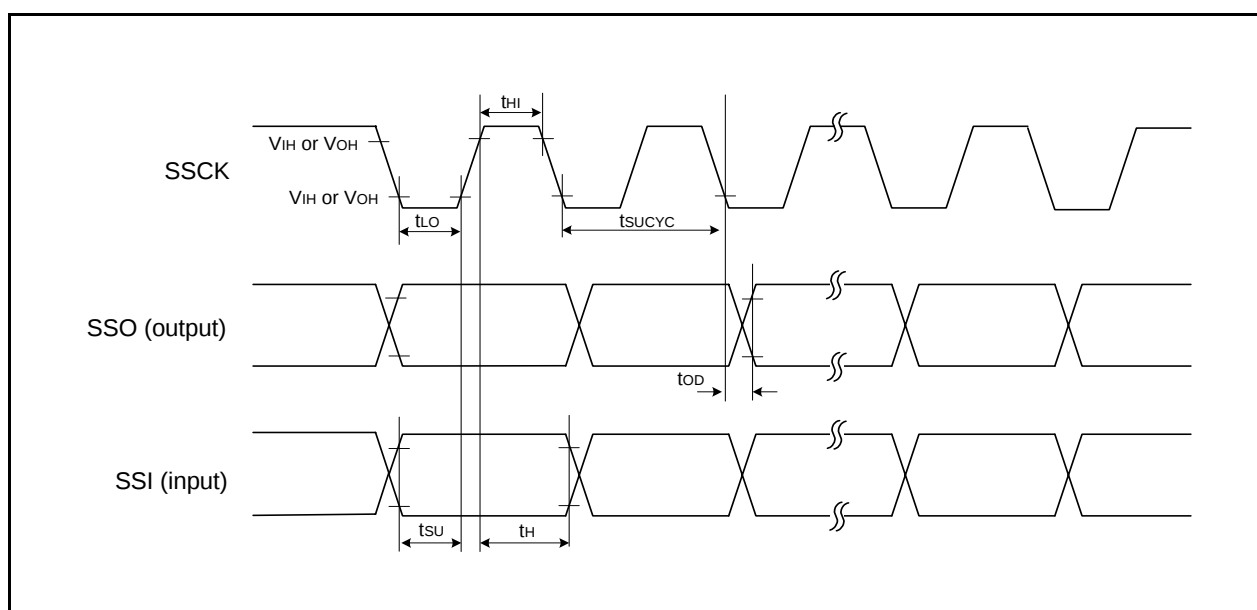


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{IXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

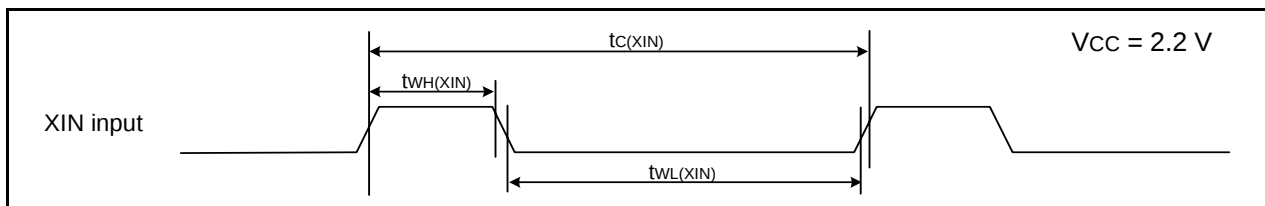
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	5.5	—	mA
				2	—	
		High-speed on-chip oscillator mode	—	5.5	11	mA
				2.2	—	
		Low-speed on-chip oscillator mode	—	145	400	μA
				145	400	
		Low-speed clock mode	—	30	—	μA
				—	—	
		Wait mode	—	28	85	μA
				17	50	
				3.3	—	
				2.1	—	
		Stop mode	—	0.65	3.0	μA
				1.65	—	

**Table 5.31 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

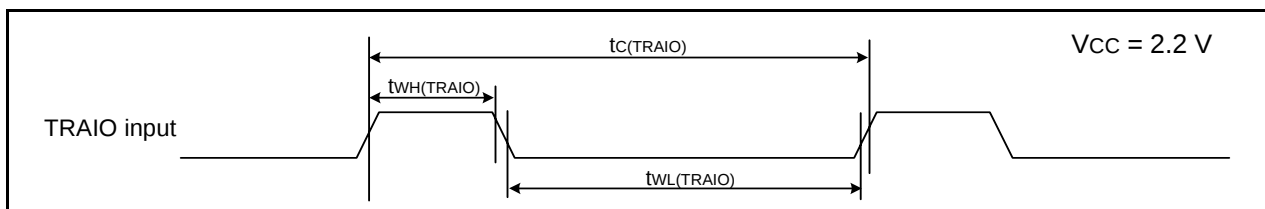
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	2.5	—	mA
				1		
		High-speed on-chip oscillator mode	—	4	—	mA
				1.7		
		Low-speed on- chip oscillator mode	—	110	300	μA
				125	350	
		Low-speed clock mode	—	27	—	μA
				20	60	
		Wait mode	—	12	40	μA
				2.8	—	
				1.9	—	
				0.6	3.0	
		Stop mode	—	1.60	—	μA
				—	—	

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.32 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.18 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input**

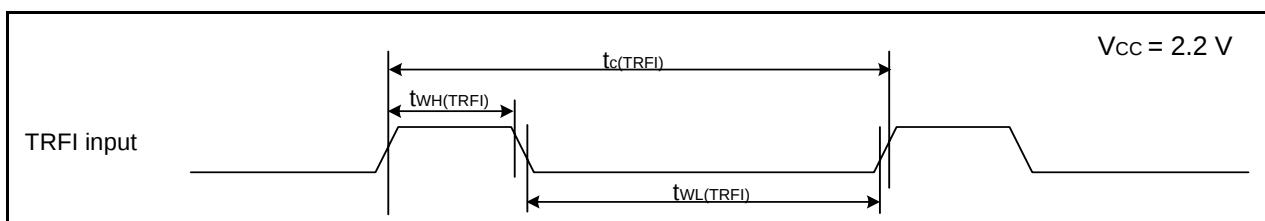
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	TBD	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	TBD	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	TBD	–	ns

**Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.34 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	2000 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	1000 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	1000 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

**Figure 5.20 TRFI Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

REVISION HISTORY	R8C/2A Group, R8C/2B Group Datasheet
------------------	--------------------------------------

Rev.	Date	Description	
		Page	Summary
0.30	Dec 22, 2006	19	Table 4.1; • 000Ah: "00XX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "0001111b" → "00X1111b" revised
		37	Table 5.11 revised
1.00	Feb 09, 2007	All pages	"Preliminary" deleted
		3	Table 1.2 revised
		5	Table 1.4 revised
		6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XX000b" → "00h" revised • 000Fh: "0001111b" → "00X1111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added
		23	Table 4.5; 0105h: "LIN Control Register 2" register name revised
		31	Table 5.2 revised
		32	Table 5.3 and Table 5.4; NOTE1 revised
		37	Table 5.11 revised
		44	Table 5.17 revised
		46	Table 5.21 and Figure 5.11; "i = 0 to 2" revised
		48	Table 5.24 revised
		50	Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised
		52	Table 5.31 revised
		53	Table 5.34 revised
		54	Table 5.35 and Figure 5.21; "i = 0 to 2" revised
2.00	Oct 17, 2007	All pages	"PTLG0064JA-A (64F0G) package" added
		3, 5	Table 1.2 and Table 1.4; • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added
		6 to 7	Table 1.5 and Figure 1.1 revised
		8	Table 1.6 and Figure 1.2 revised
		10	Figure 1.4 "64-pin LQFP Package" added
		11	Figure 1.5 added
		19 to 20	Figure 3.1 and Figure 3.2 revised
		24	Table 4.4; 00F5h: "00h" → "000000XXb" revised